3-Channel, Isolated, Sigma Delta ADC with SPI

Preliminary Technical Data

ADE7913/ADE7912

FEATURES

- Three 24-bit isolated A/D converters: one current channel and two voltage channels
- On-chip temperature sensor muxed with second voltage channel
- Integrated *iso*Power®, isolated dc-to-dc converter
- 4 wire SPI serial interface
- Up to four ADE7913s clocked from a single crystal or an external clock
- Synchronization between multiple ADE7913s
- +/-31.25mV input range for current channel
- +/-500mV input range for voltage channels
- Reference drift: 10 ppm/°C typical
- Single 3.3 V supply
- 20-lead wide body SOIC package with increased clearance and creepage
- Operating temperature: –40° to +85°C
- Safety and regulatory approvals (pending)
  - UL recognition
    - 5000V rms for 1 minute per UL1577
  - CSA Component Acceptance Notice #5A
    - IEC 61010-1: 400V rms

APPLICATIONS

- Shunt based polyphase meters
- Power quality monitoring
- Solar inverters
- Process monitoring
- Protective devices

GENERAL DESCRIPTION

The ADE7913/ADE7912 are isolated three-input channel, analog to digital converter (ADC) for polyphase energy metering applications using shunt current sensors. It features three 24-bit analog to digital converters, each of which provides 70dB signal to noise ratio over a 3 kHz signal bandwidth. One channel is dedicated to measuring the voltage across a shunt when the shunt is used for current sensing. Two additional channels are dedicated to measuring voltages, which are usually sensed using resistor dividers. One of these channels may be used to measure the temperature measurement of the die, using an internal sensor. The ADE7913 includes all the current, voltage and temperature measurements. The ADE7912 is the same as the ADE7913 but it does not include the second voltage measurement.

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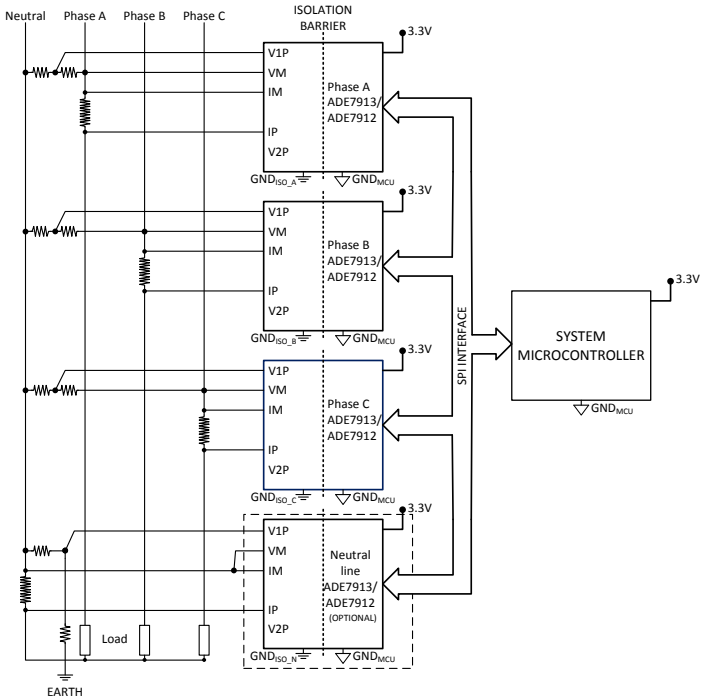

Figure 1. 3 Phase 4 Wire Meter with Four ADE7913/ADE7912s and One Microcontroller

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The ADE7913/ADE7912 include *iso*Power®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides the regulated power required by the first stage of the ADCs at 3.3V input supply. This device eliminates the need for an external dc-to-dc isolation block. The *i*Coupler chip scale transformer technology is also used to isolate the logic signals between the first and second stages of the ADC. The result is a small form factor, total isolation solution.

The ADE7913/ADE7912 contain a bidirectional SPI serial port interface. It provides access to the ADC outputs, configuration and status registers for easy interfacing with microcontrollers.

The ADE7913/ADE7912 can be clocked from a crystal or an external clock signal. To minimize the system's bill of materials, the master ADE7913/ADE7912 can drive clocks of up to three additional ADE7913/ADE7912s.

Multiple ADE7913/ADE7912s may be synchronized to sample in the same moment and provide coherent outputs.

The ADE7913/ADE7912 is available in the 20-lead wide body SOIC Pb-free package with increased creepage.

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FUNCTIONAL BLOCK DIAGRAMS

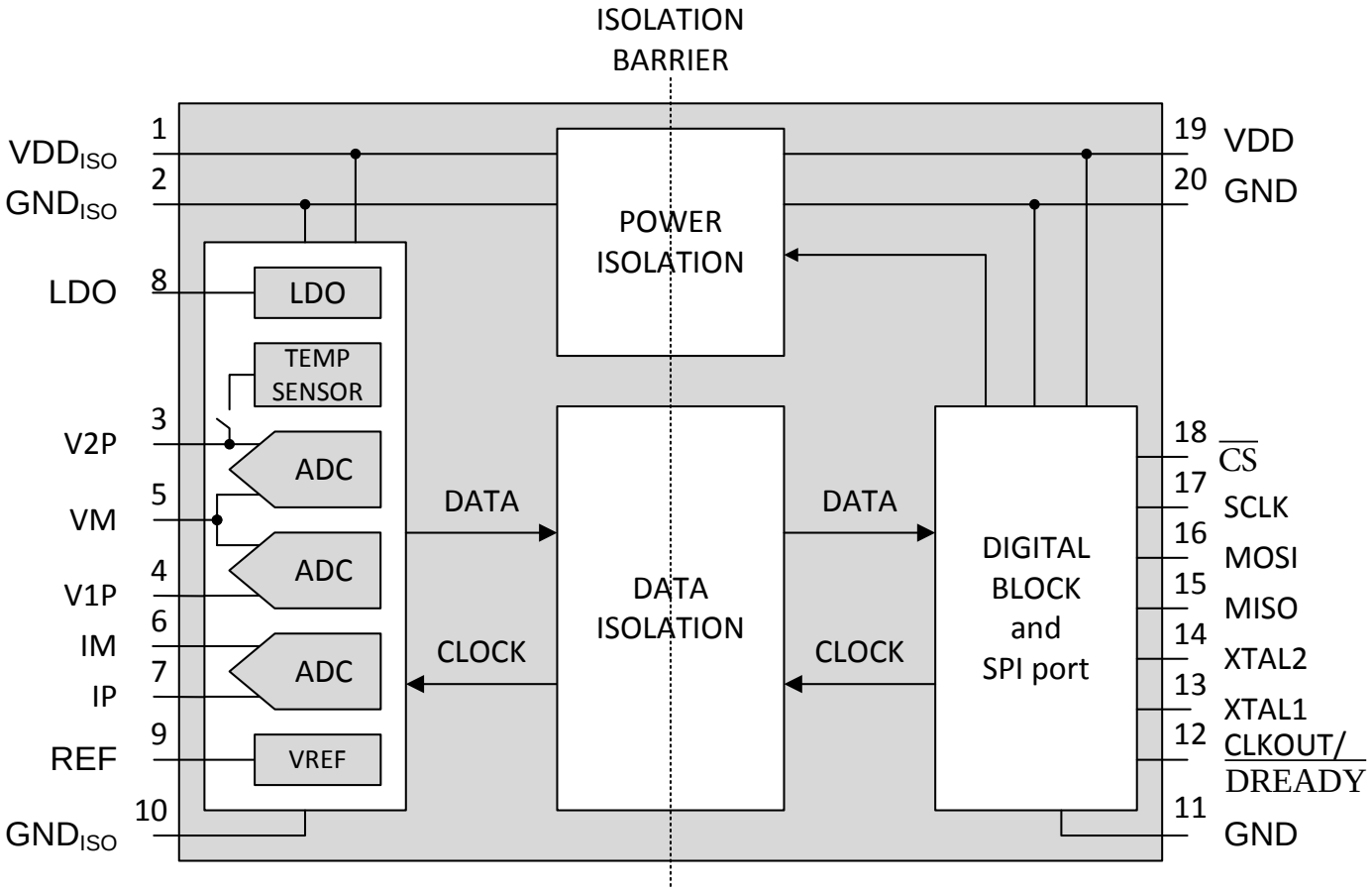

Figure 2. ADE7913 Functional Block Diagram

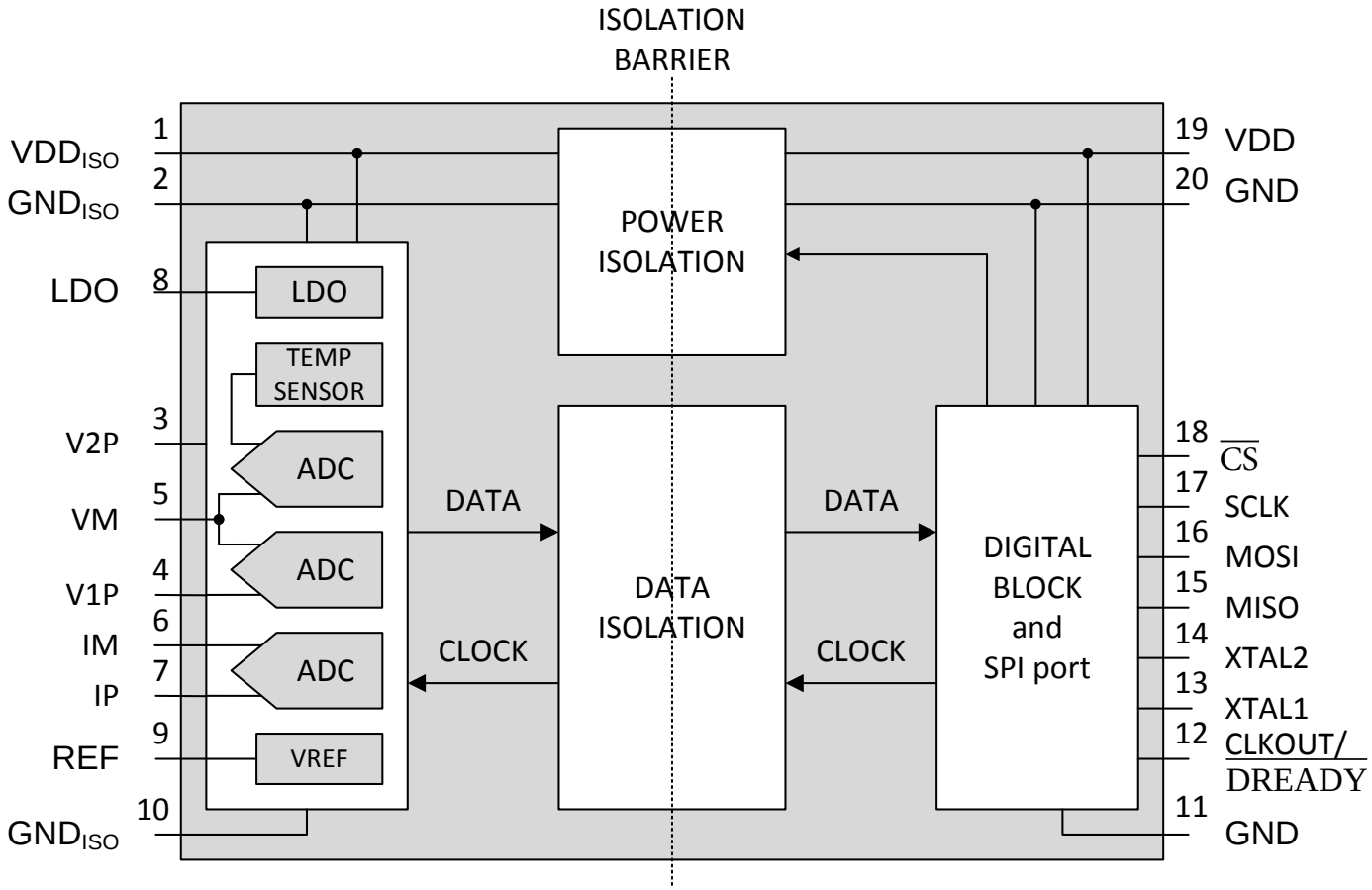

Figure 3. ADE7912 Functional Block Diagram

SPECIFICATIONS

V_{DD} = 3.3 V ± 10%, GND = 0 V, on-chip reference, XTAL1 = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP}= 25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS					
Pseudo Differential Signal at IP pin with regard to IM pin	-31.25		+31.25	mV peak	IM pin is connected to GND_{ISO}.
Pseudo Differential Signal at V1P and V2P pins with regard to VM pin	-500		+500	mV peak	Pseudo differential inputs between V1P and VM pins and between V2P and VM pins. VM pin is connected to GND_{ISO}.
Maximum common-mode voltage	-25		+25	mV	
Integral Nonlinearity	-TBD	±TBD	+TBD	LSB	
Crosstalk		TBD	TBD	dB	IM and IP inputs set to GND_{ISO}, V1P and V2P inputs at full scale
		TBD	TBD	dB	V2P and VM inputs set to GND_{ISO}, V1P and IP inputs at full scale
Input Impedance (DC)					
IP, IM, V1P, and V2P Pins	TBD			kΩ	
VM Pin	TBD			kΩ	
ADC Offset Error		TBD		mV	
ADC Offset Drift over temperature	-TBD		+TBD	nV/°C	
Gain Error	-TBD		+TBD	%	
Gain Drift over temperature	-TBD		+TBD	ppm of FS/°C	
AC Power Supply Rejection	TBD	TBD		dB	VDD = 3.3 V + 120 mV rms/50 Hz/100 Hz, IP = ±6.25mV rms, V1P = V2P = ± 100mV rms
DC Power Supply Rejection	TBD	TBD		dB	VDD=3.3 V ± 330 mV dc, IP = ±6.25mV rms, V1P = V2P = ± 100mV rms
TEMPERATURE SENSOR					
Accuracy		±5		°C	
WAVEFORM SAMPLING					
Current and Voltage Channels					
Signal-to-Noise Ratio, SNR		TBD		dB	ADC_FREQ =8kHz, BW=3300 kHz
		TBD		dB	ADC_FREQ =8kHz, BW=2000 kHz
		TBD		dB	ADC_FREQ =4kHz, BW=1650 kHz
		TBD		dB	ADC_FREQ =4kHz, BW=1000 kHz
		TBD		dB	ADC_FREQ =2kHz, BW=825 Hz
		TBD		dB	ADC_FREQ =2kHz, BW=500 Hz
		TBD		dB	ADC_FREQ =1kHz, BW=412 Hz
		TBD		dB	ADC_FREQ =1kHz, BW=250 Hz
Signal-to-Noise-and-Distortion Ratio, SINAD		TBD		dB	ADC_FREQ =8kHz, BW=3300 kHz
		TBD		dB	ADC_FREQ =8kHz, BW=2000 kHz
		TBD		dB	ADC_FREQ =4kHz, BW=1650 kHz
		TBD		dB	ADC_FREQ =4kHz, BW=1000 kHz
		TBD		dB	ADC_FREQ =2kHz, BW=825 Hz
		TBD		dB	ADC_FREQ =2kHz, BW=500 Hz
		TBD		dB	ADC_FREQ =1kHz, BW=412 Hz
		TBD		dB	ADC_FREQ =1kHz, BW=250 Hz
Total Harmonic Distortion, THD	TBD	TBD		dB	ADC_FREQ =8kHz, BW=3300 kHz
	TBD	TBD		dB	ADC_FREQ =8kHz, BW=2000 kHz
	TBD	TBD		dB	ADC_FREQ =4kHz, BW=1650 kHz
	TBD	TBD		dB	ADC_FREQ =4kHz, BW=1000 kHz
	TBD	TBD		dB	ADC_FREQ =2kHz, BW=825 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
	TBD	TBD		dB	ADC_FREQ =2kHz, BW=500 Hz
	TBD	TBD		dB	ADC_FREQ =1kHz, BW=412 Hz
	TBD	TBD		dB	ADC_FREQ =1kHz, BW=250 Hz
Spurious Free Dynamic Range, SFDR		TBD		dBFS	ADC_FREQ =8kHz, BW=3300 kHz
		TBD		dBFS	ADC_FREQ =8kHz, BW=2000 kHz
		TBD		dBFS	ADC_FREQ =4kHz, BW=1650 kHz
		TBD		dBFS	ADC_FREQ =4kHz, BW=1000 kHz
		TBD		dBFS	ADC_FREQ =2kHz, BW=825 Hz
		TBD		dBFS	ADC_FREQ =2kHz, BW=500 Hz
		TBD		dBFS	ADC_FREQ =1kHz, BW=412 Hz
		TBD		dBFS	ADC_FREQ =1kHz, BW=250 Hz
ON-CHIP REFERENCE					
Voltage Range	1.1	1.2	1.3	V	
Output Impedance	1.2			kΩ min	
Temperature Coefficient		10	50	ppm/°C	
CLKIN					All specifications for CLKIN = 4.096 MHz
Input Clock Frequency CLKIN	3.6	4.096	4.21	MHz	
CLKIN Duty Cycle	45	50	55	%	
XTAL1 logic inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
Crystal Equivalent Series Resistance			200	Ω	
XTAL1 Load Capacitor			40	pF	
XTAL2 Load Capacitor			40	pF	
CLKOUT delay from XTAL1			50	nsec	
LOGIC INPUTS—MOSI, SCLK, $\overline{CS}$					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}			±3	µA	Typical 10nA, V_{IN}=0V to VDD
Input Capacitance, C_{IN}			10	pF	

Notes:

See the Terminology section for a definition of the parameters.

XTAL1/XTAL2 load capacitors refer to the capacitors that are mounted between the XTAL1 and XTAL2 pins of the ADE7913/ADE7912 and GND. Chose these capacitors based on crystal manufacturer data sheet specification for the load capacitance. They must not have more than the max value specified in the table. For example, crystals with 20 pF load capacitance require using 40 pF capacitors on XTAL1 and XTAL2 pins.

CLKOUT delay from XTAL1 shows the delay that occurs from a high to low transition at XTAL1 pin to a synchronous high to low transition at CLKOUT/$\overline{DREADY}$ pin when CLKOUT functionality is enabled.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS— CLKOUT/$\overline{DREADY}$ AND MISO					VDD = 3.3 V
Output High Voltage, V_{OH}	3.0			V	I_{SOURCE}=800µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK}=2mA
POWER SUPPLY					For specified performance
V_{DD} Pin	2.97		3.63	V	Minimum = 3.3 V – 10%; maximum = 3.3 V + 10%
I_{DD}		TBD	TBD	mA	Bit 2 (PWRDW_EN) in CONFIG register cleared to 0.
		TBD	TBD	mA	Bit 2 (PWRDW_EN) in CONFIG register set to

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
		TBD	TBD	µA	1. Bit 2 (PWRDW_EN) in CONFIG register set to 1 and no CLKIN signal at XTAL1 pin.

REGULATORY INFORMATION

The ADE7913/ADE7912 are approved by the organizations listed in **Table 3**. Refer to **Table 9** for details regarding the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 3. Regulatory Approvals

UL Pending	CSA	VDE (Pending)
Recognized under 1577 component recognition program	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN VDE V 0884-10 (VDE V 0884-10):2006-12
Single Protection 5000 V rms isolation voltage	Basic insulation per IEC 61010-1, 400 V rms (564 V peak) maximum working voltage	Reinforced insulation, 846 V peak
File TBD	File TBD	File TBD

Notes:

In accordance with UL 1577, each ADE7913/ADE7912 is proof tested by applying an insulation test voltage ≥ 6000V rms for 1 second (current leakage detection limit = 10µA).

In accordance with DIN V VDE V 0884-10, each ADE7913/ADE7912 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5pC).

INSULATION AND SAFETY

Table 4. Critical Safety-Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(l01)	8.3	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout
Minimum External Tracking (Creepage)	L(l02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking resistance (Comparative Tracking index)	CTI	>600	V	IEC 60112
Isolation Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

The ADE7913/ADE7912 is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits.

Table 5. VDE Characteristics

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				

Description	Conditions	Symbol	Characteristic	Unit
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method B1	V_{IORM} x 1.875=$V_{pd(m)}$, 100% production test, t_{ini}=t_m=1 sec, partial discharge < 5pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A	V_{IORM} x 1.5=$V_{pd(m)}$, t_{ini}=60 sec, t_m=10 sec, partial discharge <5pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			1273	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} x 1.2=$V_{pd(m)}$, t_{ini}=60 sec, t_m=10 sec, partial discharge < 5pC		1018	V peak
Highest allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	V_{PEAK}=10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	Vpeak
Safety limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation @ 25C		P_S	2.78	W
Insulation Resistance at Ts	V_{IO}=500V	R_S	$>10^9$	Ω

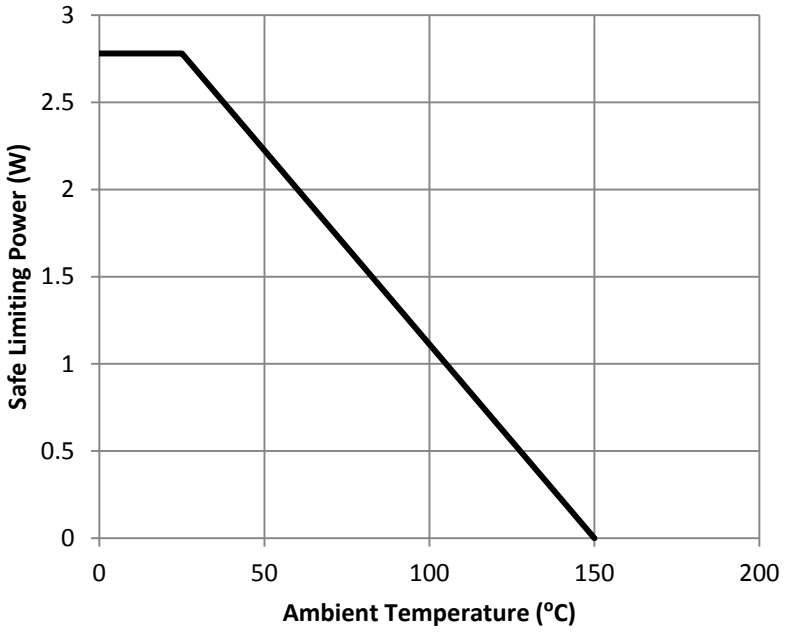

Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, CLKIN = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 6. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{CS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Frequency		250	5.6	MHz
SCLK Low Pulse Width	t_{SL}	80		ns
SCLK High Pulse Width	t_{SH}	80		ns
Data Output Valid After SCLK Edge	t_{DAV}		80	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	70		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}	5	40	ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}	0		ns

Note:

SCLK Period min and max are guaranteed by design

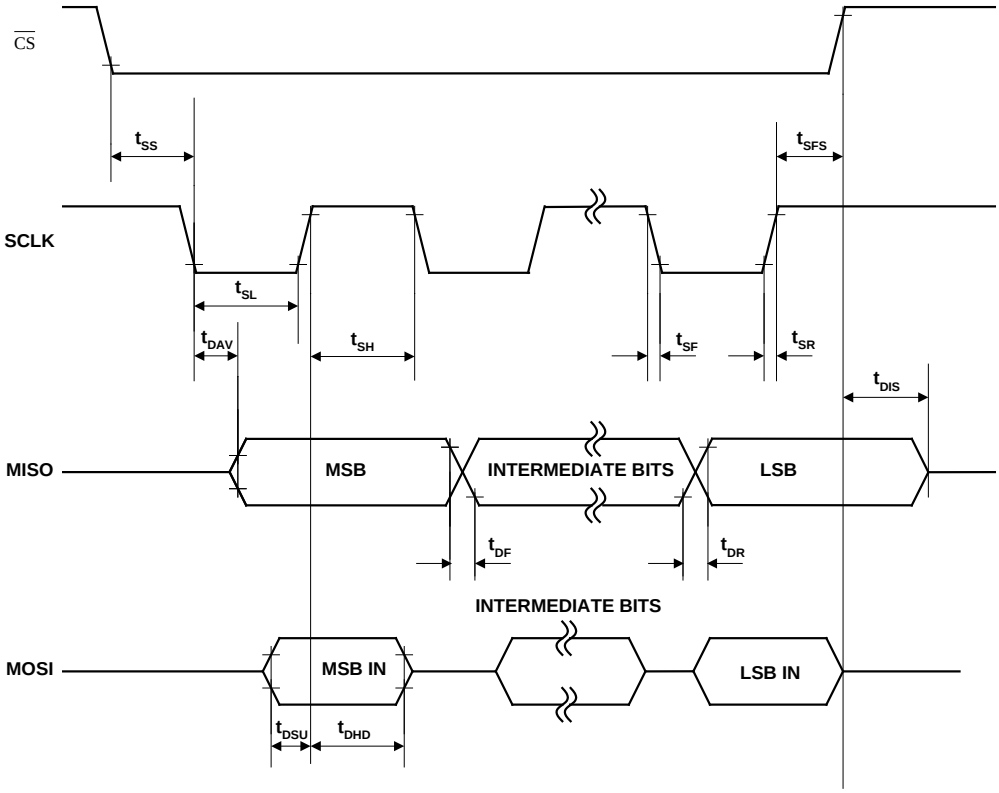

Figure 5. SPI Interface Timing

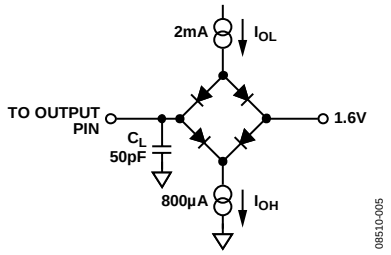

Figure 6. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to GND	−0.3 V to +3.7 V
Analog Input Voltage to GND_{ISO}, IP, IM, V1P, V2P, VM	−2 V to +2 V
Reference Input Voltage to GND_{ISO}	−0.3 V to VDD + 0.3 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Common-Mode Transients	-100 kV/µs to +100 kV/µs
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C

Note: Regarding the temperature profile used in soldering RoHS Compliant Parts : Analog Devices advises reflow profiles should conform to J-STD 20 from JEDEC. Refer to www.jedec.org for latest revision.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified equal to 48.0°C/W; θ_{JC} is specified equal to 6.2°C/W.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead SOIC_W	48.0	6.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	564	V peak	All certifications, 50-year operation
DC Voltage			
Basic Insulation	600	V peak	

[1]Refers to the continuous voltage magnitude imposed across the isolation barrier. See Insulation Lifetime section for more details

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

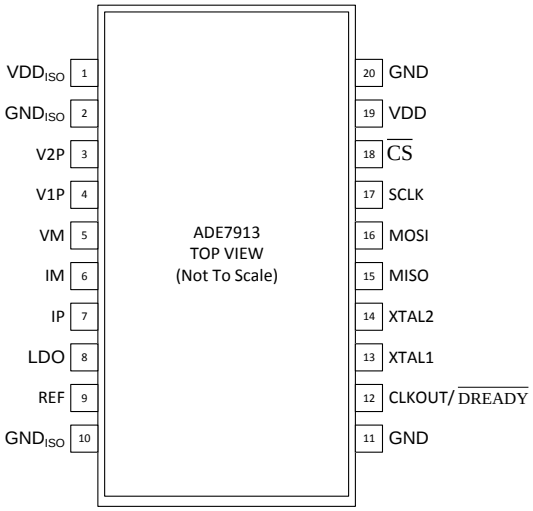

Figure 7. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD_{ISO}	This pin provides access to the 3.3V on-chip isolated power supply. Do not connect external active circuitry to this pin. Decouple this pin with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor using GND_{ISO} pin 2.
2,10	GND_{ISO}	Ground Reference of the isolated secondary side. This pin provides the ground reference for the analog circuitry. Use this quiet ground reference for all analog circuitry.
3,4,5	V2P, V1P, VM	Analog Inputs for the Voltage Channels. These channels are used with the voltage transducers and are referenced as the Voltage Channels in this document. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VM for specified operation. Connect VM pin to GND_{ISO}. If not used, connect V1P or V2P pins to VM pin. On the ADE7912, connect V2P pin to VM pin as V2P voltage channel is not available.
6,7	IM, IP	Analog Inputs for Current Channel. This channel is used with shunts and is referenced in this document as Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±31.25 mV. IM pin determines the ground of the isolated side and should be connected to GND_{ISO}.
8	LDO	2.5V output of the analog low dropout regulator (LDO). Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 100n F capacitor using GND_{ISO} pin 10. Do not connect external active circuitry to this pin.
9	REF	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. Decouple this pin to GND_{ISO} with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor using GND_{ISO} pin 10.
11,20	GND	Primary ground reference.
12	CLKOUT/$\overline{DREADY}$	When CLKOUT functionality is selected (see Synchronizing Multiple ADE7913/ADE7912 Devices section for details), the ADE7913/ADE7912 generate a digital signal synchronous to the master clock at XTAL1 pin. Use CLKOUT to provide clock to other ADE7913/ADE7912s on the board. When $\overline{DREADY}$ functionality is selected (see Synchronizing Multiple ADE7913/ADE7912 Devices section for details), the ADE7913/ADE7912 generate a low active signal synchronous to the ADC output frequency. Use this signal to start reading the ADC outputs of the ADE7913/ADE7912.
13	XTAL1	Master Clock Input. An external clock can be provided at this logic input. CLKOUT/$\overline{DREADY}$ signal of another ADE7913/ADE7912 appropriately configured (see Synchronizing Multiple ADE7913/ADE7912 Devices section for details) can be provided at this pin. Alternatively, a crystal can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7913/ADE7912. The clock frequency for specified operation is 4.096 MHz, but lower frequencies down to 3.6 MHz may be used. Use ceramic load capacitors of a few tens of picofarad with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for load capacitance requirements.
14	XTAL2	A crystal can be connected across this pin and XTAL1 (as previously described with Pin 13 in this table) to provide a clock source for the ADE7913/ADE7912.
15	MISO	Data Out for SPI Port. Pull up this pin with 10 kΩ resistor (See SPI – Compatible Interface for details).

Pin No.	Mnemonic	Description
16	MOSI	Data In for SPI Port.
17	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock (see the SPI – Compatible Interface section).
18	$\overline{CS}$	Chip Select for SPI Port.
19	V_{DD}	Primary Supply Voltage. This pin provides the supply voltage of the ADE7913/ADE7912. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple this pin to GND with a 10 µF capacitor in parallel with a ceramic 1 nF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

TEST CIRCUIT

TBD

Figure 8. Test Circuit.

TERMINOLOGY

Pseudo Differential Signal Voltage Range between the pins IP and IM, V1P and VM and V2P and VM pins

The range represents the peak-to-peak pseudo differential voltage that must be applied to the ADCs to generate a full scale response when the IM and VM pins are connected to GND_{ISO} pin 2 (Figure 9 illustrates the IP and IM case, Figure 10 illustrates the V1P, V2P and VM case).

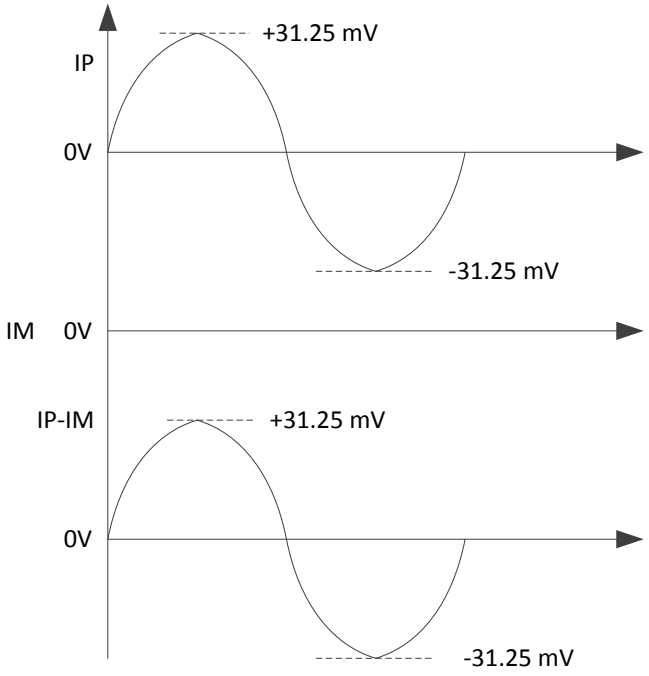

Figure 9. Pseudo Differential Input Voltage Range between IP and IM Pins

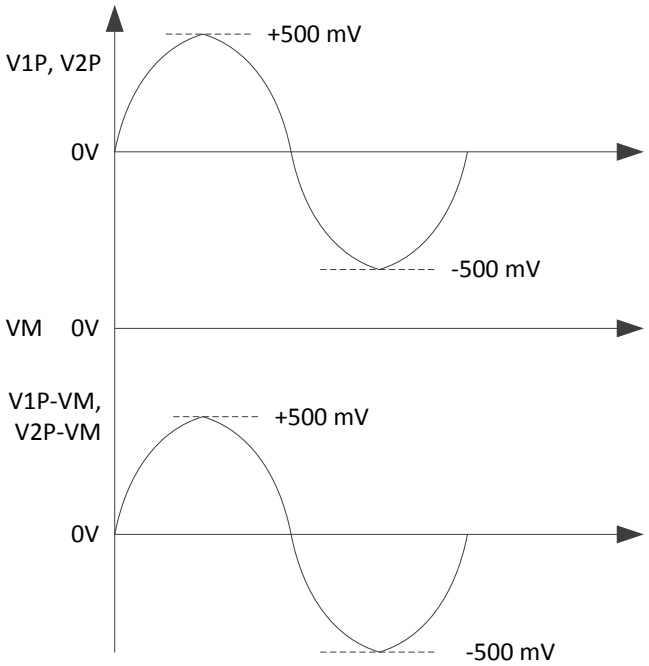

Figure 10. Pseudo Differential Input Voltage Range betweenV1P and VM and Between V2P and VM

Common-Mode Voltage Range

The common mode voltage is a voltage that appears in common at IP and IM pins of the current channel, and at V1P, V2P and VM pins of the voltage channels, with respect to ground. The range represents the maximum allowed common mode voltage.

Integral Nonlinearity (INL)

INL refers to the maximum deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. The deviation is measured from the middle of each code to the true straight line.

Crosstalk

Crosstalk represents leakage of signals, usually via capacitance between circuits. It is measured in the current channel by setting the IP and IM pins to GND_{ISO} pin 2, supplying a full scale alternate differential voltage at the V1P and V2P pins of the voltage channel and measuring the output of the current channel. It is measured in the voltage channel by setting the V2P and VM pins to GND_{ISO} pin 2, supplying a full scale alternate differential voltage at the V1P pin and measuring the output of the V2P channel. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full scale output value. The ADC outputs are acquired over 2 s. It is expressed in decibels.

Input Impedance (DC)

The input impedance represents the impedance measured at each ADC input pin: IP, IM, V1P, V2P, and VM.

ADC Offset Error

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to GND_{ISO}, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the input range of each channel.

ADC Offset Drift over temperature

The ADC offset is measured at -40°C, +25°C and +85°C and then the drift over temperature is computed in the following way:

$$Drift = \max\left[\left|\frac{Offset(-40)-Offset(25)}{Offset(25)}\right|,\left|\frac{Offset(85)-Offset(25)}{Offset(25)}\right|\right]$$

It is expressed in nV/°C.

Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code (see Analog-to-Digital Conversion section). The difference is expressed as a percentage of the ideal code.

ADC Gain Drift over temperature

This temperature coefficient includes the temperature variation of the ADC gain and of the internal voltage reference. It

represents the overall temperature coefficient of one current or voltage channel. With the internal voltage reference in use, the ADC gain is measured at -40°C, +25°C and +85°C. Then the temperature coefficient is computed as follows:

$$Drift = \max\left[\left|\frac{Gain(-40) - Gain(25)}{Gain(25)}\right|, \left|\frac{Gain(85) - Gain(25)}{Gain(25)}\right|\right]$$

It is measured in ppm of FS/°C.

Power Supply Rejection (PSR)
This quantifies the measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 50 Hz or 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (Power Supply Rejection Ratio, PSRR). Then PSR= 20 $\log_{10}$ (PSRR).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading (PSRR). Then PSR= 20 $\log_{10}$ (PSRR).

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The spectral components are calculated over a 2s window. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The spectral components are calculated over a 2s window. The value for SINAD is expressed in decibels.

Total Harmonic Distortion, THD

THD is the ratio of the rms sum of all harmonics (neglecting the noise components) to the rms value of the fundamental. The spectral components are calculated over a 2s window. The value for THD is expressed in decibels.

Spurious Free Dynamic Range, SFDR

SFDR is the ratio of the rms value of the actual input signal to the rms value of the peak spurious component over the waveform samples measurement bandwidth. The spectral components are calculated over a 2s window. The value of SFDR is expressed in decibel relative to full scale, dBFS.

On-chip Reference Temperature Coefficient

The voltage of the on-chip reference is measured at -40°C, +25°C and +85°C and then the drift over temperature is computed in the following way:

$$Drift = \max\left[\left|\frac{REF(-40) - REF(25)}{REF(25)}\right|, \left|\frac{REF(85) - REF(25)}{REF(25)}\right|\right]$$

APPLICATION INFORMATION

ADE7913/ADE7912 IN POLY-PHASE ENERGY METERS

The ADE7913/ADE7912 have been designed to be used in three phase energy metering systems in which two, three or four ADE7913/ADE7912s are managed by a master device containing an SPI interface, usually a microcontroller.

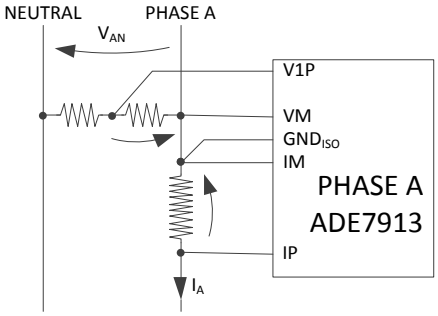

Figure 11. Phase A ADE7913/ADE7912 current and voltage sensing

Figure 9 presents the phase A of a three phase energy meter. The phase A current, I_A, is sensed with a shunt. A pole of the shunt is connected to IM pin of the ADE7913/ADE7912 and becomes the ground of the isolated side of the ADE7913/ADE7912, GND_{ISO}. The phase A to neutral voltage V_{AN} is sensed with a resistor divider and VM pin is also connected to IM and GND_{ISO} pins. Note that the voltages measured by the ADCs of the ADE7913/ADE7912 are opposite to V_{AN} and I_A, a classic approach of single phase metering. The other ADE7913/ADE7912s that monitor phases B and C are connected in a similar way.

The voltage channel, V2P, is intended to measure an auxiliary voltage and it is available only on the ADE7913. If V2P is not used, as is the case of the ADE7912, connect V2P to VM.

Figure 10 presents a block diagram of a three phase energy meter that uses three ADE7913/ADE7912s and a microcontroller. The neutral current is not monitored in this case. To simplify the drawing, the shunts and the voltage dividers have not been shown as the structure presented in Figure 9 is present on all phases. There is only one 4.096MHz crystal providing the clock to the ADE7913/ADE7912 that senses the phase A current and voltage. The ADE7913/ADE7912s that sense the phases B and C currents and voltages are clocked by a signal generated at CLKOUT pin of the ADE7913/ADE7912 placed to sense the phase A current and voltage. As an alternative configuration, the microcontroller may generate a 4.096MHz clock to all ADE7913/ADE7912s at the XTAL1 pin (see Figure 11). Note that XTAL1 pin may receive a clock with the frequency within the 3.6 MHz to 4.21 MHz range, as specified in Table 1.

The microcontroller uses the SPI port to communicate with the ADE7913/ADE7912s. Three of its I/O pins, CS_A, CS_B and CS_C are used to generate the SPI $\overline{CS}$ signals. The SCLK, MOSI and MISO pins of the microcontroller are directly connected to the correspondent pins SCLK, MOSI and MISO of each ADE7913/ADE7912 (Figure 14). To simplify Figure 10 and successive figures, these connections have not been shown.

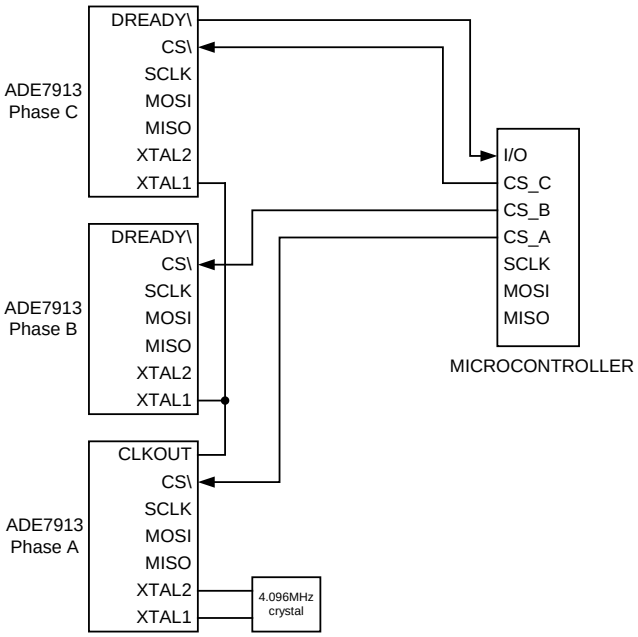

Figure 12. Three phase energy meter using three ADE7913/ADE7912s

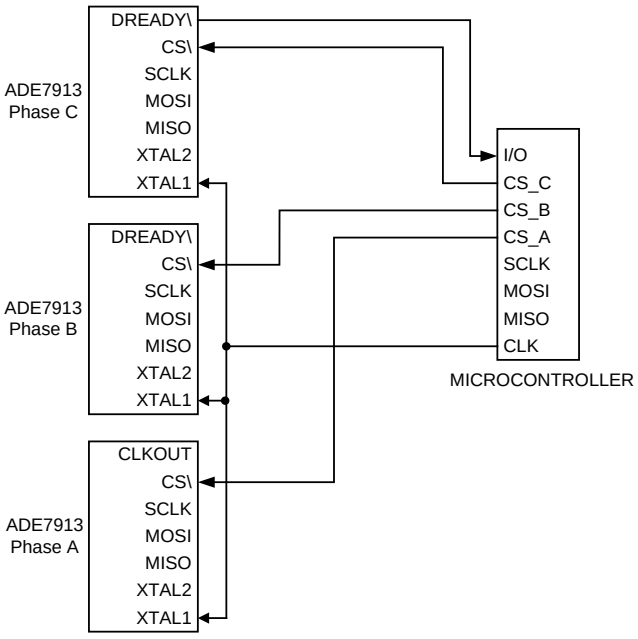

Figure 13. Microcontroller generating clock to three ADE7913/ADE7912s

The CLKOUT/ $\overline{DREADY}$ pin of the ADE7913/ADE7912 used to sense the phase C current and voltage is connected to an I/O pin of the microcontroller. It provides an active low pulse for 64 CLKIN cycles (15.625 μsec at CLKIN=4.096MHz) when the ADC conversion data is available. It signals when the ADC outputs of all ADE7913/ADE7912s become available and when the microcontroller starts to read them. See Synchronizing

Multiple ADE7913 Devices for more details on the method to synchronizing multiple ADE7913/ADE7912s.

At power up, or after a hardware or software reset, the procedure presented in Power – up procedure section must be followed to make the ADE7913/ADE7912s function appropriately.

The case of the energy meter using four ADE7913/ADE7912s is similar and it is presented in Figure 12. The microcontroller uses an additional I/O pin, CS_N, to generate the SPI $\overline{CS}$ signal to the ADE7913/ADE7912 monitoring the neutral current.

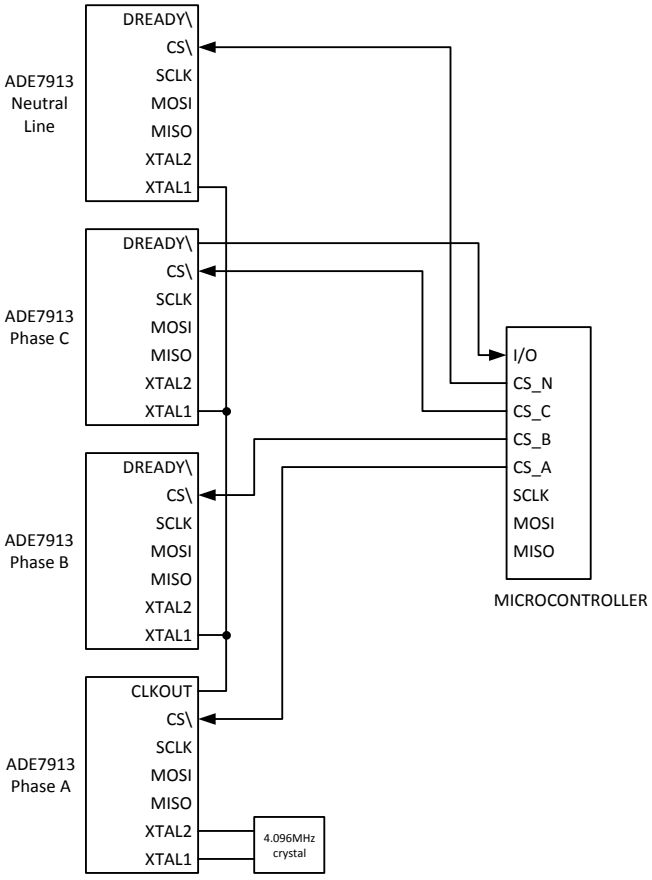

Figure 14. Three phase energy meter using four ADE7913/ADE7912s

The case of the energy meter using two ADE7913/ADE7912s in a delta configuration is shown in Figure 13. The meter ground is on phase B line. One ADE7913/ADE7912 measures phase A current and phase A to phase B voltage. Second ADE7913/ADE7912 measures phase C current and phase C to phase B voltage. Phase B current and phase A to phase C voltage are computed by the system's microcontroller.

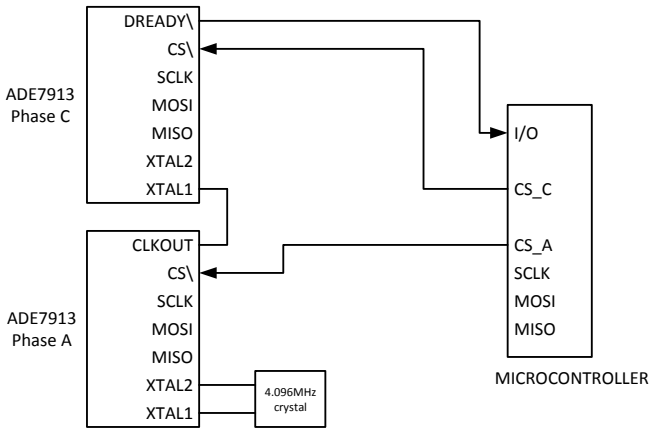

Figure 15. Three Phase Meter using two ADE7913/ADE7912s for Delta Configuration

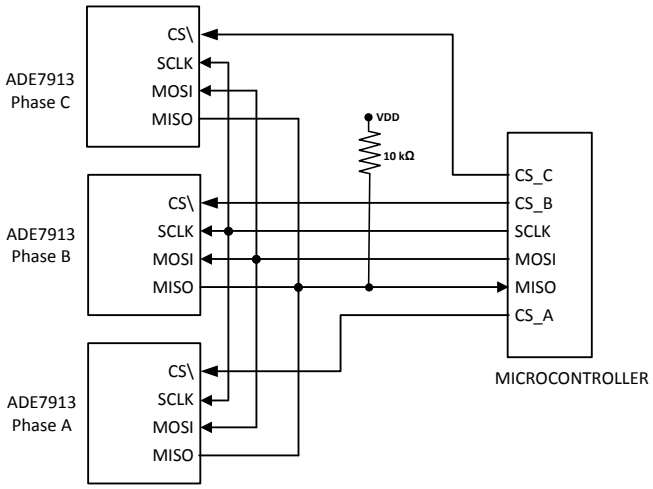

Figure 16. SPI connections between three ADE7913/ADE7912s and a microcontroller

SPI – COMPATIBLE INTERFACE

The SPI of the ADE7913/ADE7912 is the slave of the communication and consists of four pins: SCLK, MOSI, MISO, and $\overline{CS}$. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. Data shifts into the ADE7913/ADE7912 at the MOSI logic input on the falling edge of SCLK and the ADE7913/ADE7912 samples it on the rising edge of SCLK. Data shifts out of the ADE7913/ADE7912 at the MISO logic output on a falling edge of SCLK and can be sampled by the master device on the raising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum and minimum serial clock frequencies supported by this interface are 5.6 MHz and 250 Hz, respectively. MISO stays in high impedance when no data is transmitted from the ADE7913/ADE7912. At power up, or during hardware or software reset, the microcontroller reads STATUS0 register to detect when bit 0 (RESET_ON) clears to 0. To allow reading this bit as 1 during this period, a 10kΩ pull up resistor is recommended on this pin. See Figure 14 for details of the

connection between the SPI ports of three ADE7913/ADE7912s and a microcontroller containing an SPI interface.

The $\overline{CS}$ logic input is the chip select input. Drive the $\overline{CS}$ input low for the entire data transfer operation. Bringing $\overline{CS}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{CS}$ logic input to low. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, every time a register is written, its value should be verified by reading it back.

SPI Read Operation

The read operation using the ADE7913/ADE7912 SPI interface initiates when the master sets the $\overline{CS}$ pin low and begins sending one command byte on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK.

The bit composition of the command byte is presented in **Table 11**. Bits 1:0 are reserved and they can have any value. The examples presented throughout this section use them set to 00. Bit 2 (Read_En) determines the type of the operation. If it is a read, then Read_En must be set to 1. If it is a write, Read_En must be cleared to 0. Bits 7:3 (ADDR) represent the address of the register to be read or written.

Table 11. Command byte for SPI read/write operations

Bit Location	Bit Mnemonic	Description
1:0	Reserved	These bits can have any value.
2	Read_En	Set this bit to 1 if a SPI read operation is executed. Clear this bit to 0 if a SPI write operation is executed.
7:3	ADDR	Address of the register to be read or written.

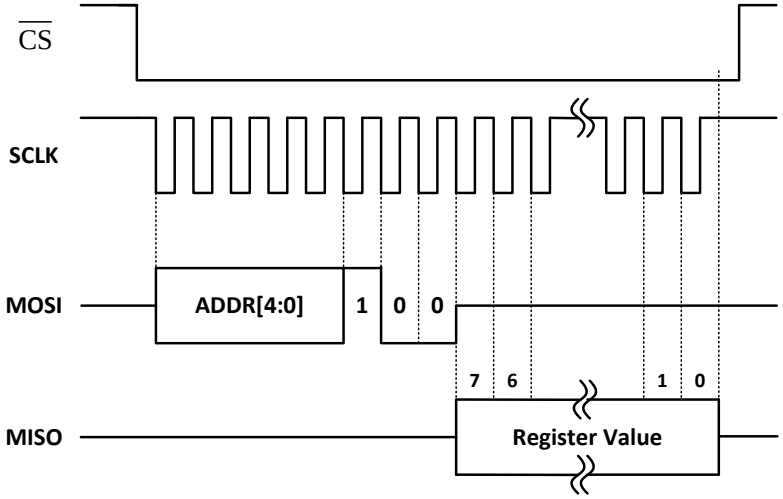

Figure 17. SPI Read Operation of an 8-bit Register

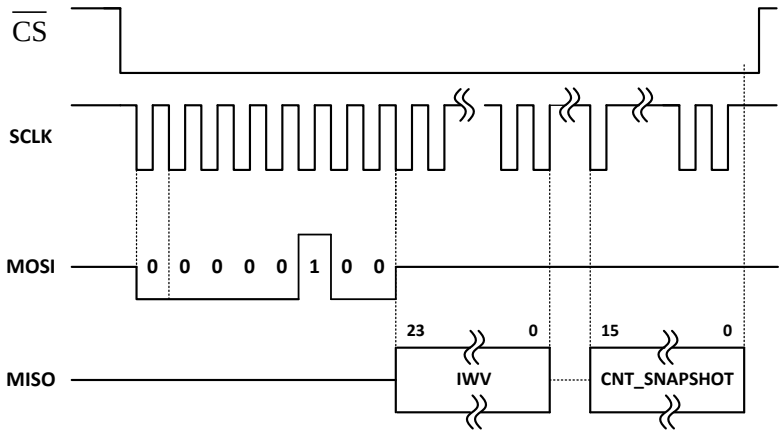

Figure 18. SPI Read Operation in Burst Mode

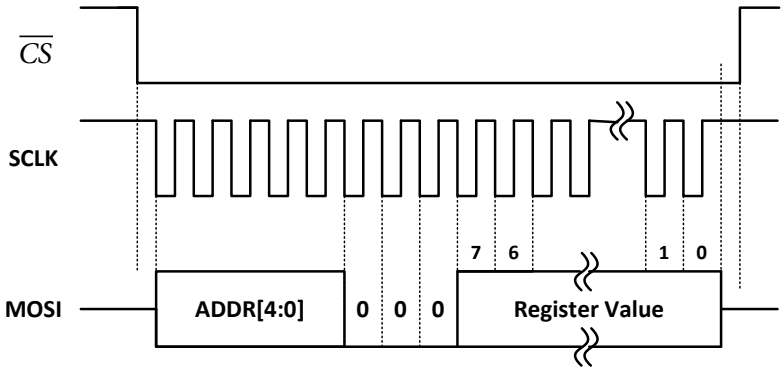

Figure 19. SPI Write Operation

The ADE7913/ADE7912 SPI samples data on the low-to-high transitions of SCLK. After the ADE7913/ADE7912 receives the last bit of the command byte on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit, it sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. Figure 15 presents the details of an 8-bit register read operation. 16-bit and 32-bit registers are read in the same manner.

SPI Read Operation in Burst Mode

All ADE7913/ADE7912 output registers, IWV, V1WV, V2WV, ADC_CRC, STATUS0 and CNT_SNAPSHOT can be read in two ways. First is the regular way, one register at a time (see SPI Read Operation section for details). The second way is reading multiple consecutive registers at a time in a burst mode. The burst mode initiates when the master sets the $\overline{CS}$ pin low and begins sending the command byte (see **Table 11**) on the MOSI line with bits 7:3 (ADDR) set to IWV register address, 00000. This means a command byte set to 0x04. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7913/ADE7912 samples data on the low-to-high transitions of SCLK. After the ADE7913/ADE7912 receives the last bit of the command byte on a low-to-high transition of SCLK, it begins to transmit the 24-bit IWV register on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit of IWV, the ADE7913/ADE7912 sends V1WV that is placed at the next location and so forth until the master sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO go into high impedance state. See Figure 16 for details of the SPI read operation in burst mode.

If, for example, 16-bit CNT_SNAPSHOT register does not need to be read, the master sets the $\overline{CS}$ and SCLK lines high after STATUS0 register has been received.

If, for example, IVW register is not required, but V1WV is, then set ADDR bits to the V1WV address, 00001, in the command byte and execute the SPI in burst mode operation.

SPI Write Operation

The SPI write operation initiates when the master sets the $\overline{CS}$ pin low and begins sending one command byte (see **Table 11**). Bit 2 (Read_En) has to be cleared to 0. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7913/ADE7912 samples data on the low-to-high transitions of SCLK. Next, the master sends the 8-bit value of the register without losing any SCLK cycle. After the last bit is transmitted, at the end of SCLK cycle, the master sets the $\overline{CS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 17 for details of the SPI write operation.

Note that the SPI write operation can execute only 8-bit writings. The 16-bit COUNTER register is written executing the write operation twice: the less significant byte is written first followed by the most significant byte. See Synchronizing Multiple ADE7913/ADE7912 Devices section for details on the functionality controlled by COUNTER register.

As the ADE7913/ADE7912 does not need to acknowledge a write command in any way, this operation can be broadcast to multiple ADE7913/ADE7912s when the same register has to be initialized with the same value.

SYNCHRONIZING MULTIPLE ADE7913/ADE7912 DEVICES

In polyphase metering systems, it is highly desired to sample all currents and voltages in the same exact moment and to provide coherent ADC output samples. Additionally, to use the EMI reduction scheme managed by EMI_CTRL register (see DC-TO-DC Converter section for details), the ADE7913/ADE7912s of the system must provide coherent samples.

Section "ADE7913/ADE7912 in Poly-Phase Energy Meters" presented how a polyphase energy meter containing multiple ADE7913/ADE7912s may use one crystal to clock all the ADE7913/ADE7912s. At power up, only one ADE7913/ADE7912 is clocked from the crystal as the others are set to receive clock from CLKOUT/ $\overline{DREADY}$ pin of the first

ADE7913/ADE7912. Additionally, this pin has $\overline{\text{DREADY}}$ functionality enabled by default. In Figure 10, Figure 12, and Figure 13, the ADE7913/ADE7912 on phase A is clocked from the crystal and the other ADE7913/ADE7912s are in standby as there is no clock signal coming into their XTAL1 pin. The microcontroller enables CLKOUT functionality by setting bit 0 (CLKOUT_EN) to 1 in CONFIG register. This ensures the other ADE7913/ADE7912s in the system receive the same clock as the ADE7913/ADE7912 on phase A. This operation ensures that all ADCs within all ADE7913/ADE7912s in the system sample data in the same exact moment.

As an alternative to using one single crystal, the microcontroller may generate a clock signal to the XTAL1 pins of every ADE7913/ADE7912, ensuring the precise ADC sampling synchronization (see Figure 11).

To configure all ADE7913/ADE7912s in an energy meter to provide coherent ADC output samples, that is samples obtained in the same output cycle, all ADE7913/ADE7912s must have the same ADC output frequency and the outputs must be synchronized. The bits 5, 4 (ADC_FREQ) in CONFIG register select the ADC output frequency, so they must be initialized to the same value (see ADC Output Values section for more details). To synchronize the ADC outputs, that is to set all ADE7913/ADE7912s to generate ADC outputs in the same exact moment, after power up, the microcontroller has to broadcast a write to the 8-bit SYNC_SNAP register with the value 0x01. All ADE7913/ADE7912s then start a new ADC output period simultaneously when the bit0 (SYNC) of SYNC_SNAP register has been written. SYNC bit clears itself back to 0 after one CLKIN cycle.

As presented in Figure 10, Figure 12, and Figure 13, the pin CLKOUT/ $\overline{\text{DREADY}}$ of one ADE7913/ADE7912 is connected to an I/O input of the microcontroller. This ADE7913/ADE7912 has bit 0 (CLKOUT_EN) in CONFIG register set at the default value, 0, to enable the $\overline{\text{DREADY}}$ functionality. When the ADC output period starts, $\overline{\text{DREADY}}$ pin goes low for 64 CLKIN cycles (15.625 µsec when CLKIN=4.096 MHz), signaling that all ADC outputs from all ADE7913/ADE7912s are available and the microcontroller must start reading them. It is recommended to use the SPI read burst mode, as this ensures all data is read in the shortest amount of time.

The ADE7913/ADE7912 contains an internal 12-bit counter that functions at CLKIN frequency. It is synchronized with the ADC output period and $\overline{\text{DREADY}}$ pin. When a new output period starts, the counter starts decreasing from a value determined by bits 5,4 (ADC_FREQ) in CONFIG register. Table 12 presents these values.

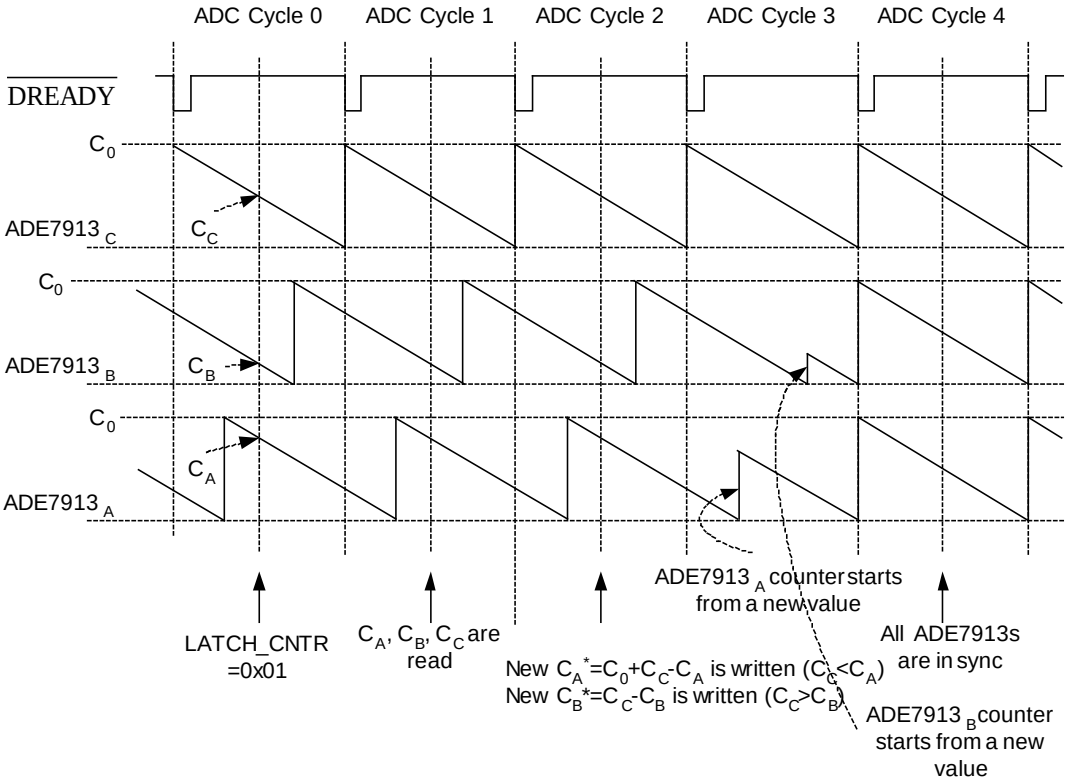

Figure 20. Synchronizing Phase A and B ADE7913/ADE7912s With Phase C ADE7913/ADE7912

Table 12. Counter initial values function of ADC_FREQ bits

Bits 5,4 (ADC_FREQ) in CONFIG register	ADC output frequency	Counter C_0 initial value (CLKIN=4.096 MHz)	Counter C_0 initial value function of CLKIN
00	8KHz	511	$\frac{CLKIN}{8000}-1$
01	4KHz	1023	$\frac{CLKIN}{4000}-1$
10	2KHz	2047	$\frac{CLKIN}{2000}-1$
11	1KHz	4095	$\frac{CLKIN}{1000}-1$

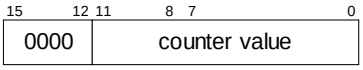

Figure 21. CNT_SNAPSHOT Register

The 8-bit register SYNC_SNAP latches the value of the counter when it is written with 0x02, which means bit 1 (SNAP) set to 1. A broadcast write to all ADE7913/ADE7912s ensures all the counters of every ADE7913/ADE7912 are latched in the same moment. The bit SNAP clears itself back to 0 after one CLKIN cycle. The values of the counters offer a measure of the ADC outputs synchronization across all ADE7913/ADE7912s. Ideally, the values should be perfectly equal, showing all ADE7913/ADE7912s are fully synchronized. In reality, due to the uncertainty between the SPI clock generated by the microcontroller and the ADE7913/ADE7912 CLKIN, a ±1 count difference between counters is acceptable. The 12-bit counter is accessed as 16-bit CNT_SNAPSHOT register (see Figure 19).

If the internal counter of one ADE7913/ADE7912 does not have a value correlated with the values of the other ADE7913/ADE7912s counters, this means the ADC outputs of one phase are no longer synchronized with the ADC outputs from the other phases. The ADE7913/ADE7912 provides two options: one is to broadcast a write to the 8-bit SYNC_SNAP register with the value 0x01. This immediately forces all ADE7913/ADE7912s to start an ADC output cycle simultaneously. However, all phases would present ADC output distortions of various degrees function of when SYNC_SNAP=0x01 writing is executed within the current output period. Therefore, this command is better to be executed at power up or after a hardware or software reset.

The other option is to compute a new starting value for the internal counter of the particular ADE7913/ADE7912 that is out of sync. This value forces the internal counter to start a new ADC output cycle counting down from it and end simultaneously with the other counters of the other ADE7913/ADE7912s. The 12-bit value is stored into two 8-bit COUNTER1 and COUNTER0 registers (see Figure 20). COUNTER0 contains the less significant 8 bits and must be written first. COUNTER1 contains the 4 most significant bits and must be written after COUNTER0. The advantage relative to using SYNC_SNAP=0x01 is that only the ADC outputs of phase out of sync are affected. The other phases already in sync remain untouched. As a general rule, it is recommended to verify the synchronization of the ADE7913/ADE7912s every couple of seconds.

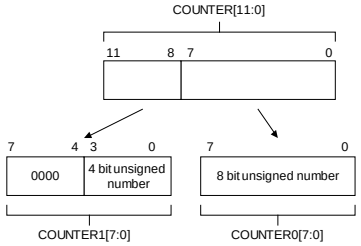

Figure 22. Counter start value is communicated using two 8-bit registers

Consider the case presented in Figure 18: Phase A, B and C counters of three ADE7913/ADE7912s are shown for the meter presented in Figure 10. All of them are out of synchronization. It is desired to synchronize phase A and phase B ADE7913/ADE7912s with the phase C ADE7913/ADE7912 which is considered as reference because it generates $\overline{\text{DREADY}}$. The following steps are executed immediately after the output registers IWV, V1WV, V2WV, ADC_CRC and STATUS0 have been read when $\overline{\text{DREADY}}$ low active pulses have been generated:

-ADC cycle 0:

Disable the configuration registers protection by setting Lock register to 0x9C (See Protecting the integrity of configuration registers section for details). Set the 8-bit register SYNC_SNAP to 0x02 using a write broadcast command. The values C_A, C_B and C_C of the three counters are latched and stored into the CNT_SNAPSHOT registers.

-ADC cycle 1:

ADE7913/ADE7912s counters C_A, C_B and C_C latched at cycle 0 are read in burst mode together with IWV, V1WV, V2WV, ADC_CRC and Status registers .

-ADC cycle 2:

Because C_A>C_C, the following equation can be written:

$C_C + C_0 = C_A + C_A^*$, where C_A^* is the new value that must be determined. New initial counter value $C_A^* = C_C + C_0 - C_A$ is written into phase A ADE7913/ADE7912 in two consecutive 8-bit writes to COUNTER0 and COUNTER1 registers. Phase A ADE7913/ADE7912 will be in sync with phase C ADE7913/ADE7912 starting with ADC cycle 4.

Because C_B<C_C, the following equation can be written:

$C_C = C_B + C_B^*$, where C_B^* is the new value that must be determined. New initial counter value $C_B^* = C_C - C_B$ is written into phase B ADE7913/ADE7912 in two consecutive 8-bit writes to COUNTER0 and COUNTER1 registers. Phase B ADE7913/ADE7912 will be in sync with phase C ADE7913/ADE7912 starting with ADC cycle 4.

As demonstrated above, if the latched value of the counter on the reference phase X is C_X and the initial value of the counter is C_0 (see Table 11), the new value of the counter on phase Y required to bring phase Y in synchronization to phase X is:

If $C_Y > C_X$, then $C_Y^* = C_X + C_0 - C_Y$. (1)

If $C_Y \leq C_X$, then $C_Y^* = C_X - C_Y$. (2)

-ADC cycle 3:

The phases A and B ADE7913/ADE7912s counters start counting down based on the COUNTER1 and COUNTER0 values written during ADC cycle 2.

-ADC cycle 4:

All ADE7913/ADE7912s generate ADC outputs synchronously. To verify this, as a good programming practice, the counters should be read again, so SYNC_SNAP=0x02 command is executed one more time.

-ADC cycle 5:

ADE7913/ADE7912s counters C_A, C_B and C_C latched after SYNC_SNAP= 0x2 command are stored into the CNT_SNAPSHOT register and are read in burst mode. They should show the same value plus or minus 1LSB, which means plus or minus one CLKIN cycle (±244nsec for CLKIN=4.096MHz):

$C_C = C_A \pm 1 = C_B \pm 1$.

Enable back the configuration registers protection by setting Lock register to 0xCA (See Protecting the integrity of configuration registers section for details).

The ±1 LSB error may appear because CLKIN, the internal clock of the ADE7913/ADE7912 is asynchronous to the serial port clock generated by the microcontroller and used to write the COUNTER1 and COUNTER0 values during ADC cycle 2.

The EMI reduction scheme managed by EMI_CTRL register (see DC-TO-DC Converter section for details) requires the ADE7913/ADE7912s of the system to provide coherent samples. This ensures no ADE7913/ADE7912 of the system generates the PWM signals required to manage the dc-to-dc converter in the same moment with another ADE7913/ADE7912. The ±1 LSB error in the counter synchronization means at least two ADE7913/ADE7912s generate PWM signals simultaneously for one CLKIN cycle and the EMI reduction scheme may be impacted. While there are no guarantees, both synchronization procedures outlined in this section may be repeated until $C_C = C_A = C_B$.

POWER MANAGEMENT

DC-TO-DC CONVERTER

The dc-to-dc converter section of the ADE7913/ADE7912 works on the principles that are common to most modern power supply designs. V_{DD} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power is transferred to the secondary side where it is rectified to a high dc voltage. The power is then linearly regulated down to about 3.3V and supplied to the ADC side section through a 2.5V LDO regulator.

The ADE7913/ADE7912's internal dc-to-dc converter state is controlled by the input V_{DD}. In normal operation mode, V_{DD} should be maintained between 2.97V and 3.63V.

The block diagram of the isolated dc-to-dc converter is presented in Figure 21. The ADE7913/ADE7912 primary supply voltage VDD input supplies an alternative current (ac) source. The ac signal passes through a chip-scale air core transformer and it is transferred to the secondary side. A rectifier then produces the isolated power supply VDD_{ISO}. Using another chip-scale air core transformer, a feedback circuit measures VDD_{ISO} and passes the information back into the VDD domain where a PWM control block controls the ac source to maintain VDD_{ISO} at 3.3V.

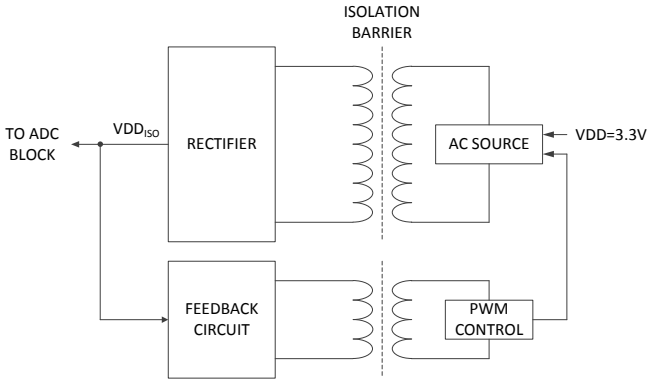

Figure 23. Isolated dc-to-dc Converter Block Diagram

The PWM control block works at CLKIN/4 (1.024 MHz) clock and every half period generates a PWM pulse to the ac source (Figure 22).

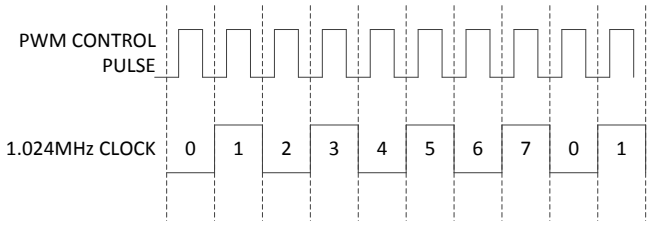

Figure 24. PWM Control Block Generates Pulses Based on 1MHz Clock

Every time a PWM pulse is generated, the ac source transmits very high frequency signals across the isolation barrier to allow efficient power transfer through the small chip-scale transformers. This creates high frequency currents that can propagate in the circuit board ground and the power planes, causing edge and dipole radiation. The PCB Board Layout section presents the best PCB layout approach to deal with the electromagnetic interference (EMI) issues. In addition to the layout approach, the EMI_CTRL 8-bit register helps in reducing the emissions generated by the ADE7913/ADE7912 dc-to-dc converter.

The clock that manages the PWM Control block is divided in 8 periodical slots, 0 to 7, as presented in Figure 22. Every bit of EMI_CTRL register controls one slot: bit 0 controls slot 0, bit 1 controls slot 1, …, bit 7 controls slot 7. When the bit is 1, the default value, the PWM Control block generates a pulse, when the bit is 0, the PWM Control block does not generate any pulse. The recommendation is to have only four of these bits set to 1 for every ADE7913/ADE7912 used in the system to further reduce the emissions generated by the ADE7913/ADE7912 dc-to-dc converter.

If the three-phase energy meter contains four ADE7913/ADE7912s, then first the ADE7913/ADE7912s have to be synchronized (see Synchronizing Multiple ADE7913/ADE7912 Devices). Then every EMI_CTRL register should be initialized. The dc-to-dc converters of only two ADE7913/ADE7912s generate EMI in the same moment, lowering the overall EMI level of the meter. Initialize EMI_CTRL register of phase A ADE7913/ADE7912 (EMI_CTRL_A) to 0x55, EMI_CTRL_B to 0xAA, EMI_CTRL_C to 0x55, and EMI_CTRL_N to 0xAA (Figure 23).

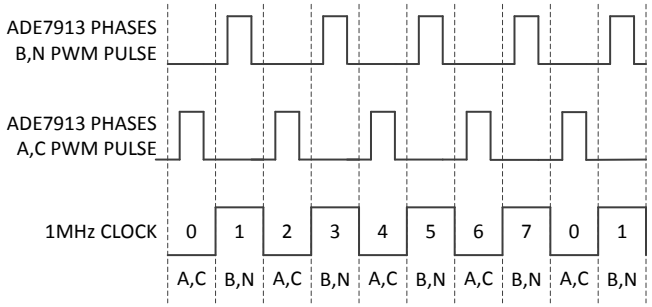

Figure 25. EMI Management at a Three Phase Meter with Four ADE7913/ADE7912s

If the board contains one, two or three ADE7913/ADE7912s, set four bits in the EMI_CTRL register according to the approach presented in Figure 23 while leaving slots unused.

MAGNETIC FIELD IMMUNITY

The ADE7913/ADE7912 is immune to dc magnetic fields because it uses air core transformers. The limitation on the ADE7913/ADE7912's ac magnetic field immunity is set by the condition in which the induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3.3V operating condition is examined because it is the nominal supply of the ADE7913/ADE7912.

The pulses at the transformer output have amplitude greater than 1.0V. The decoder has a sensing threshold at about 0.5V, thus establishing a 0.5V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = \left(-\frac{d\beta}{dt} \right) \sum_{n=1}^{N} \pi r_n^2 \quad (3)$$

where:

β is the ac magnetic field: $\beta(t) = B \times \sin(\omega t)$

N is the number of turns in the receiving coil.

R_n is the radius of the n^{th} turn in the receiving coil.

Given the geometry of the receiving coil in the ADE7913/ADE7912 and an imposed requirement that the induced voltage V_{THR} be, at most, 50% of the 0.5V margin at the decoder, a maximum allowable magnetic field B is calculated, as shown in Figure 24.

$$B = \frac{V_{THR}}{2\pi f \times \sum_{n=1}^{N} \pi r_n^2} \quad (4)$$

where f is the frequency of the magnetic field and B is the amplitude of the ac magnetic field.

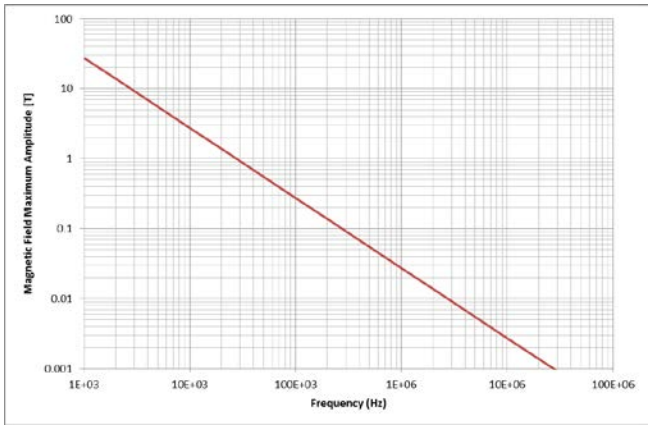

Figure 26. Maximum allowable external magnetic field

For example, at a magnetic field frequency of 10 kHz, the maximum allowable magnetic field of 2.8 T induces a voltage of 0.25V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from more than 1.0V to 0.75V, still well above the 0.5Vsensing threshold of the decoder.

The preceding magnetic field values correspond to specific current magnitudes at given distances from the ADE7913/ADE7912 transformers.

$$I = \frac{B}{\mu_0} \times 2\pi d = \frac{V \times d}{\mu_0 \times f \times \sum_{n=1}^{N} \pi r_n^2} \quad (5)$$

where μ_0 is $4\pi \times 10^{-7}$ H/m , the magnetic permeability of the air.

Figure 25 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADE7913/ADE7912 is extremely immune and can be affected only be extremely large currents operated at high frequency very close to the component. For the 10 kHz example noted, one would have to place 5mm away from the ADE7913/ADE7912 a current with an amplitude of 69 kA to affect the component's operation.

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility (see PCB Board Layout section).

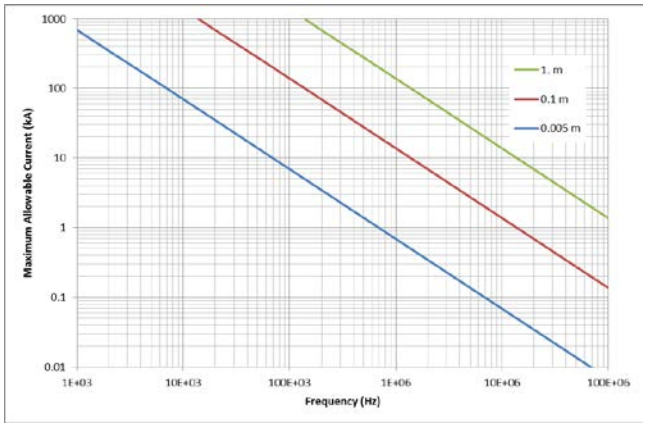

Figure 27. Maximum allowable current for various current-to-ADE7913/ADE7912 spacings

PCB BOARD LAYOUT

TBD

POWER – UP AND INITIALIZATION PROCEDURES

At power up, or after a hardware or software reset, the microcontroller managing a system formed by one or multiple ADE7913/ADE7912s must execute the following steps to manage the ADE7913/ADE7912s.

Power – up procedure for systems with one single ADE7913/ADE7912

For one standalone ADE7913/ADE7912 managed by a microcontroller, the power up procedure is (see also Figure 26):

-connect a crystal between XTAL1 and xTAL2 pins.

-supply VDD to the ADE7913/ADE7912. To ensure the ADE7913/ADE7912 starts functioning correctly, the supply must reach 3.3V-10% in less than 23 msec from approximately 2.0V level. The ADE7913/ADE7912 starts to function.

- The dc-to-dc converter takes then approximately 30msec to power up and supply the isolated side of the

ADE7913/ADE7912. After this time, the isolated side of the ADE7913/ADE7912 is fully functional.

-To determine when the ADE7913/ADE7912 is ready to accept commands, read STATUS0 register until its bit 0 (RESET_ON) is cleared to 0. This happens approximately 20 msec after the ADE7913/ADE7912 started to function and indicates the non-isolated side of the ADE7913/ADE7912 is fully functional using the default settings.

-initialize CONFIG, the configuration register and EMI_CTRL, the emissions control register.

-protect the configuration registers by setting LOCK register to 0xCA. See Protecting the integrity of configuration registers section for details.

-the ADE7913/ADE7912 begins generating at CLKOUT/ $\overline{\text{DREADY}}$ pin a signal that is active low for 64 CLKIN cycles (15.625µsec for CLKIN=4.096MHz) when ADC conversion data is available.

$\overline{\text{DREADY}}$ functionality is enabled by default at CLKOUT/ $\overline{\text{DREADY}}$ pin.

-the microcontroller reads in SPI burst mode IWV, V1WV, V2WV, ADC_CRC and STATUS0 registers (see SPI Read operation in burst mode section for more details).

Note that this power up procedure applies in the same way to systems that have multiple ADE7913/ADE7912s, each clocked from its own crystal. Every ADE7913/ADE7912 is powered up and started independently.

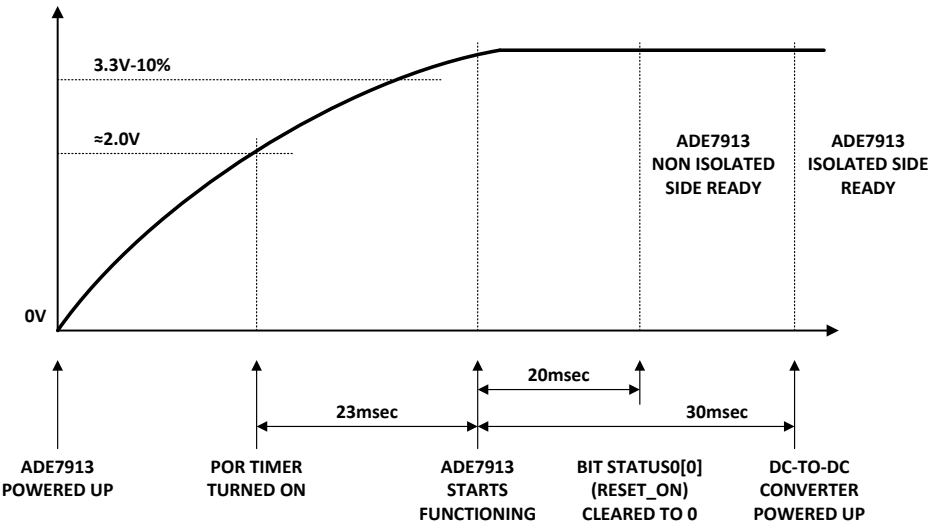

Figure 28. Power Up Procedure for Systems with One or Multiple ADE7913/ADE7912s, each Clocked from its own Crystal

Power – up procedure for systems that use one single crystal

For poly phase energy meters presented in Figure 10, Figure 12 and Figure 13in which one single crystal is used, the power up procedure is (see also Figure 27):

-supply VDD to the ADE7913/ADE7912s. To ensure the Phase A ADE7913/ADE7912 (ADE7913/ADE7912$_A$) starts functioning correctly, the supply must reach 3.3V-10% in less than 23 msec from approximately 2.0V level. The ADE7913/ADE7912$_A$ is clocked by the 4.096MHz crystal and starts functioning. The other ADE7913/ADE7912s are not clocked yet.

-The dc-to-dc converter takes then approximately 30msec to power up and supply the isolated side of the ADE7913/ADE7912$_A$. After this time, the isolated side of the ADE7913/ADE7912$_A$ is fully functional.

-To determine when the ADE7913/ADE7912$_A$ is ready to accept commands, STATUS0 register is read until its bit 0 (RESET_ON) is set to 0. This happens approximately 20 msec after the ADE7913/ADE7912 started to function and indicates the non-isolated side of the ADE7913/ADE7912$_A$ is fully functional using the default settings.

-initialize configuration register CONFIG of the ADE7913/ADE7912$_A$ with bit 0 (CLKOUT_EN) set to 1. CLKOUT signal is provided at CLKOUT/ $\overline{\text{DREADY}}$ pin and the ADE7913/ADE7912s on the other phases are now clocked.

-initialize EMI_CTRL, the emissions control register of the ADE7913/ADE7912$_A$.

-the dc-to-dc converters of the other ADE7913/ADE7912s power up approximately 30msec after the clock was provided. The isolated sides of the ADE7913/ADE7912s are now fully functional.

-read STATUS0 registers of the other ADE7913/ADE7912s until bit 0 (RESET_ON) is set to 0, indicating their non-isolated sides are fully functional with default settings. It happens approximately 20 msec after the clock signal was provided.

-initialize CONFIG register of all remaining ADE7913/ADE7912s. Select one ADE7913/ADE7912 (ADE7913/ADE7912$_C$ in Figure 10, Figure 12 and Figure 13 examples) and connect its CLKOUT/ $\overline{\text{DREADY}}$ pin to an

external interrupt I/O pin of the microcontroller. The ADE7913/ADE7912C must have bit 0 (CLKOUT_EN) in CONFIG register left to the default value of 0 as it uses $\overline{\text{DREADY}}$ functionality at CLKOUT/ $\overline{\text{DREADY}}$ pin.

-initialize EMI_CTRL, the emissions control register of all remaining ADE7913/ADE7912s.

-execute SYNC_SNAP=0x01 write broadcast to synchronize all the ADE7913/ADE7912s of the meter (see Synchronizing Multiple ADE7913/ADE7912 Devices sections for details).

-execute LOCK=0xCA write broadcast to protect the configuration registers of all ADE7913/ADE7912s. See Protecting the integrity of configuration registers section for details.

-periodically, every couple of seconds, disable the registers protection, execute a SYNC_SNAP=0x02 write broadcast to read CNT_SNAPSHOT register of every ADE7913/ADE7912 and see if resynchronization is necessary. Resynchronize the ADE7913/ADE7912s out of sync (see Synchronizing Multiple ADE7913/ADE7912 Devices sections for details) and then enable back the registers protection.

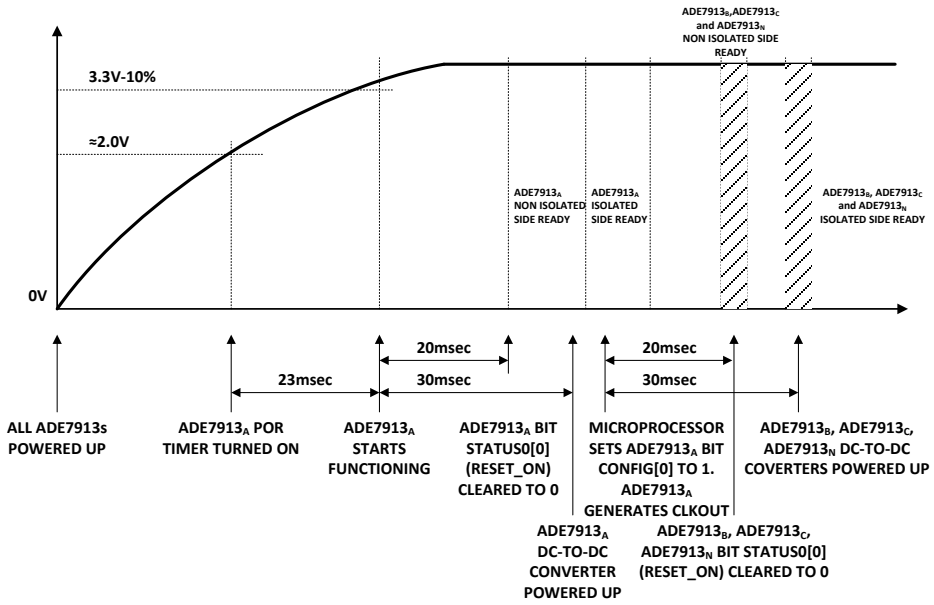

Figure 29. Power Up Procedure for Systems with Multiple ADE7913/ADE7912s.Only Phase A ADE7913/ADE7912 is Clocked from a Crystal

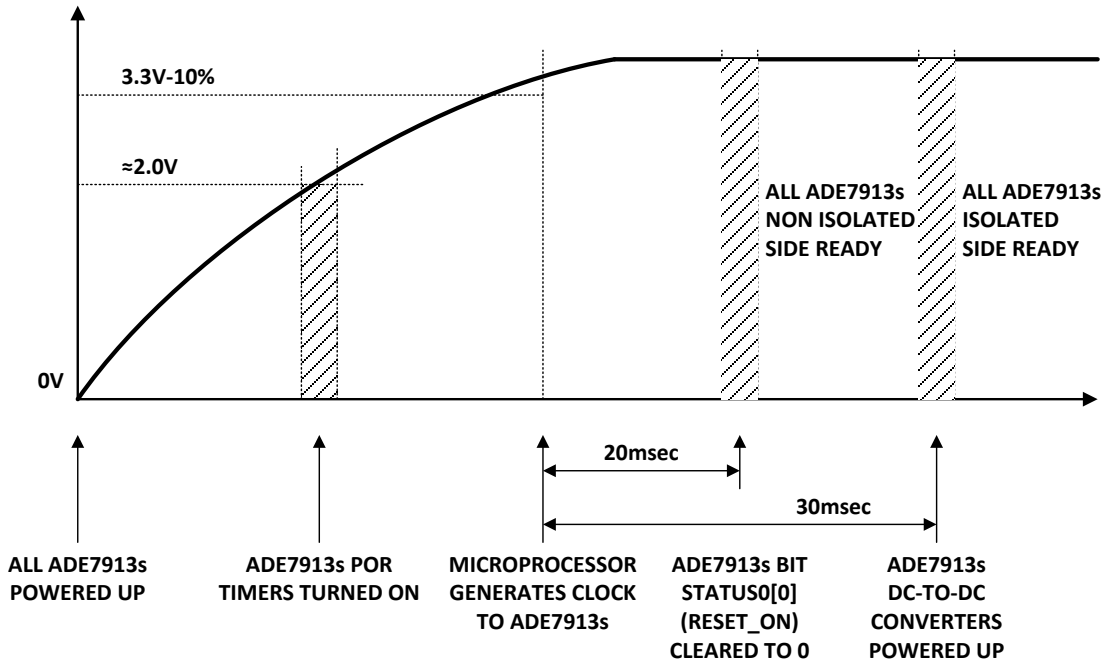

Figure 30. Power-Up Procedure for Systems with Multiple ADE7913/ADE7912 Clocked from a Microprocessor

Power – up procedure for systems that use clock generated from microcontroller

For poly phase energy meters presented in Figure 11 in which the microcontroller generates the clock signal used by all ADE7913/ADE7912s, the power-up procedure is:

-supply VDD to the ADE7913/ADE7912s. To ensure the ADE7913/ADE7912s start functioning correctly, the supply must reach 3.3V-10% in less than 23 msec from 2.0V±10% level.

-generate the clock signal from the microcontroller to all ADE7913/ADE7912s.

-The dc-to-dc converters take then approximately 30msec to power up and supply the isolated side of the ADE7913/ADE7912s. After this time, the isolated side of the ADE7913/ADE7912s is fully functional.

-read STATUS0 registers of the ADE7913/ADE7912s until bit 0 (RESET_ON) is set to 0, indicating the non-isolated side of the ADE7913/ADE7912s is fully functional with default settings. It happens approximately 20 msec after the clock signal was provided.

-initialize configuration register CONFIG of the ADE7913/ADE7912s with bit 0 (CLKOUT_EN) cleared to 0 to avoid generating an unnecessary clock at CLKOUT/ $\overline{\text{DREADY}}$ pins. Select one ADE7913/ADE7912 (ADE7913/ADE7912$_C$ in Figure 11 example) and connect its CLKOUT/ $\overline{\text{DREADY}}$ pin to an external interrupt I/O pin of the microcontroller.

-initialize EMI_CTRL, the emissions control register of all ADE7913/ADE7912s.

-execute a SYNC_SNAP=0x01 write broadcast to synchronize all the ADE7913/ADE7912s of the meter (see Synchronizing Multiple ADE7913/ADE7912 Devices sections for details).

-execute LOCK=0xCA write broadcast to protect the configuration register of all ADE7913/ADE7912s. See Protecting the integrity of configuration registers section for details.

-periodically, every couple of seconds, disable the registers protection, execute a SYNC_SNAP=0x02 write broadcast to read COUNTER1 and COUNTER0 registers of every ADE7913/ADE7912 and see if resynchronization is necessary. Resynchronize the ADE7913/ADE7912s that drift out of sync (see Synchronizing Multiple ADE7913/ADE7912 Devices sections for details) and then enable back the registers protection.

HARDWARE RESET

The ADE7913/ADE7912 does not have a dedicated $\overline{\text{RESET}}$ pin. Instead, if $\overline{\text{CS}}$ and MOSI pins are both kept low simultaneously for 64 SCLK cycles, then the ADE7913/ADE7912 enters the hardware reset state.

If $\overline{\text{CS}}$ and MOSI pins are kept low for 64 SCLK cycles, all the registers are set to their default values and the dc-to-dc converter is shut down. The procedure can be done simultaneously for all ADE7913/ADE7912s in a poly phase energy meter. At the end of the reset period, the ADE7913/ADE7912 sets bit 0 (RESET_ON) to 0 in STATUS0 register. At this point, one of the procedures presented in the Power – up and initialization section must be followed to initialize correctly the ADE7913/ADE7912s .

Keeping low $\overline{\text{CS}}$ and MOSI pins can be accomplished by executing a SPI broadcast write operation in which the lines are kept low for 64 SCLK cycles. This is equivalent to sending 8 bytes equal to 0x00 to the ADE7913/ADE7912 to accomplish the hardware reset.

SOFTWARE RESET

Bit 6 (SWRST) in the CONFIG register manages the software reset functionality. The default value of this bit is 0. If this bit is set to 1, then the ADE7913/ADE7912 enters the software reset state. In this state, all the internal registers are set to their default values. The dc-to-dc converter continues to function. When the software reset ends, Bit 6 (SWRST) in the CONFIG register clears automatically to 0 and bit 0 (RESET_ON) in STATUS0 register becomes 0. If configuration registers have been protected using a LOCK=0xCA register write, first unlock the registers by writing LOCK=0x9C and then write CONFIG register with bit 6 (SWRST) set to 1 to start a software reset. At this point, one of the procedures presented in the Power – up and initialization section must be followed to initialize correctly the ADE7913/ADE7912.

POWER DOWN MODE

There are situations in which the ADCs of the ADE7913/ADE7912 do not need to function and it is desirable to lower the current consumption of the device. Bit 2 (PWRDWN_EN) in CONFIG register, when set to 1, turns off the dc-to-dc converter and the Σ-Δ modulators are shut down. If PWRDWN_EN is cleared to 0, the default value, the dc-to-dc converter is functional and the Σ-Δ modulators are active.

If the microcontroller generates the clock to all ADE7913/ADE7912s (situation presented in Figure 11), the current consumption may be further reduced by shutting down the clock.

In systems in which CLKOUT pin of one ADE7913/ADE7912 is used to clock other ADE7913/ADE7912s (situation present in Figure 10, Figure 12 and Figure 13), lower current consumption of these ADE7913/ADE7912s may be achieved by clearing bit 0 (CLKOUT_EN) to 0 in CONFIG register.

THEORY OF OPERATION

ANALOG INPUTS

The ADE7913/ADE7912 has 3 analog inputs, one current and two voltage channels. The current channel has two fully differential voltage input pins: IP and IM that accept a maximum differential signal of ±31.25 mV.

The maximum signal level on the IP/IM with respect to GND_{ISO} is also ±31.25 mV. The maximum common-mode signal allowed on these inputs is ±25mV. Figure 29 presents a schematic of the input for the current channel and its relation to the maximum common-mode voltage.

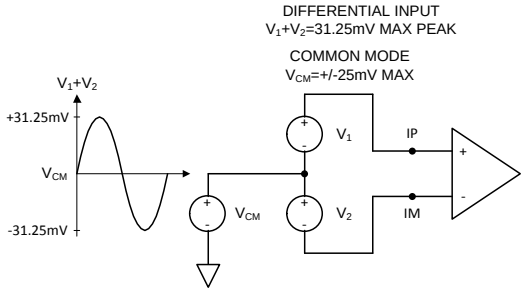

Figure 31. Maximum Input Level, Current Channels

Note that the current channel is used to sense the voltage across a shunt. In this case one pole of the shunt becomes the ground of the meter (Figure 11) and therefore the current channel is used in a pseudo differential configuration, similar to the voltage channel configuration (Figure 32).

The voltage channel has two pseudo differential, single-ended voltage input pins: V1P and V2P. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VM. The maximum signal level on analog inputs for VxP and VM is also ±0.5 V with respect to GND_{ISO}. The maximum common-mode signal allowed on the inputs is ±25mV. Figure 30 presents a schematic of the voltage channel inputs and their relation to the maximum common-mode voltage.

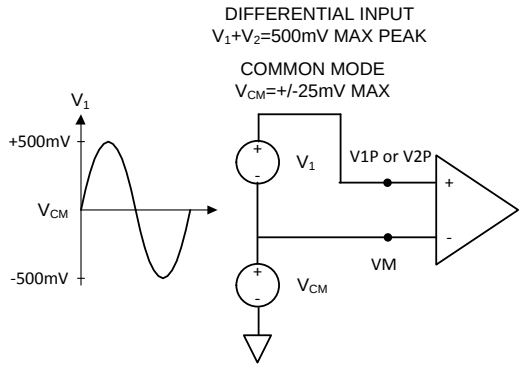

Figure 32. Maximum Input Level, Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7913/ADE7912 has three second order sigma-delta (Σ-Δ) analog-to-digital converters (ADCs). For simplicity, the block diagram in Figure 31 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter, separated by the digital isolation block.

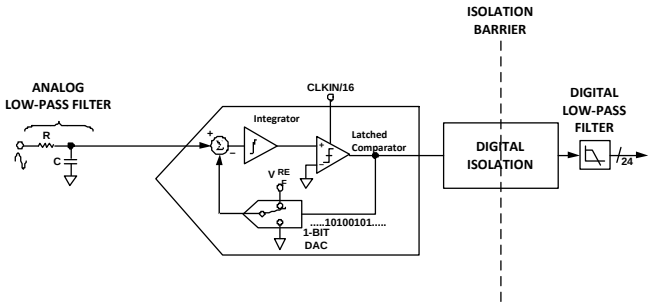

Figure 33. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7913/ADE7912, the sampling clock is equal to CLKIN/4 (1.024MHz when CLKIN=4.096 MHz). The 1-bit DAC in the feedback loop is driven by the serial stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter, after the data passed through the digital isolators. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, when CLKIN=4.096 MHz, the sampling rate in the ADE7913/ADE7912 is 1.024 MHz, while the bandwidth of interest is 40 Hz to 3.3 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered, as shown in Figure 32. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling factor of 4 is required just to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. This is the second technique used to achieve high resolution. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 32.

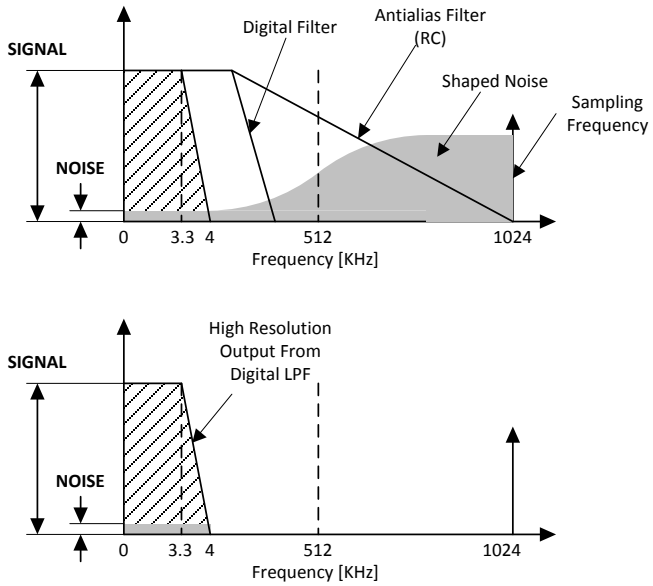

Figure 34. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

The bandwidth of interest is function of the input clock frequency, the ADC output frequency selectable by bits 5,4 (ADC_FREQ) in CONFIG register (see ADC Output Values for details) and Bit 7 (BW) of the CONFIG register. When CLKIN is 4.096 MHz and the ADC output frequency is 8 kHz: if BW is cleared to 0, the default value, the bandwidth is 3.3 kHz. If BW is set to 1, the bandwidth is 2 kHz. **Table 13** presents the ADC output frequencies and the ADC bandwidth selections function of the input clock frequency. Three cases are presented: one for CLKIN=4.096 MHz, the typical value, one for 4.21 MHz, the maximum clock input frequency, and one for 3.6 MHz, the minimum clock input frequency.

Antialiasing Filter

Figure 31 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7913/ADE7912, and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems as shown in Figure 33. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Frequency components above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, that is, 1.024MHz, move into the band of interest for metering, that is, 40Hz to 3.3 kHz or 2 kHz. To attenuate the high frequency (near 1.024MHz) noise and prevent the distortion of the band of interest, a low-pass filer (LPF) must be introduced. It is recommended to use one RC filter with a corner frequency of 5 kHz for the attenuation to be sufficiently high at the sampling frequency of 1.024MHz. The 20dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing.

Table 13. ADC Output Frequency and ADC Bandwidth Function of CLKIN Frequency

CLKIN [MHz]	Bits ADC_FREQ in CONFIG register	ADC Output Frequency [Hz]	ADC Bandwidth when bit BW in CONFIG register cleared to 0 [Hz]	ADC Bandwidth when bit BW in CONFIG register set to 1 [Hz]
4.096	00	8000	3300	2000
	01	4000	1650	1000
	10	2000	825	500
	11	1000	412	250
4.21	00	8222	3391	2055
	01	4111	1695	1027
	10	2055	847	513
	11	1027	423	256
3.6	00	7031	2900	1757
	01	3515	1450	878
	10	1757	725	439
	11	878	362	219

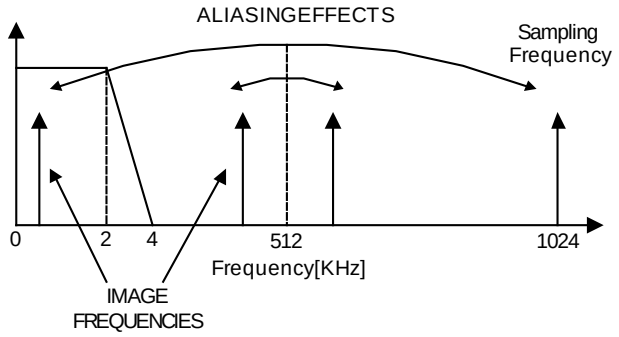

Figure 35. Antialiasing Effects

ADC Transfer Function

All ADCs in the ADE7913/ADE7912 are designed to produce the same 24-bit signed output code for the same input signal level. With a full-scale input signal of 31.25mV on the current channel and 0.5V on the voltage channels and an internal reference of 1.2V, the ADC output code is nominally 5,320,000 and usually varies for each ADE7913/ADE7912 around this value. The code from the ADC can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±49.27mV on the current channel and ±0.788 V on the voltage channels. However, for specified performance, do not exceed the nominal range of ±31.25 mV for the current channel and ±0.5 V for the voltage channels; ADC performance is guaranteed only for input signals within these limits.

ADC Output Values

The ADC output values are stored into three 24-bit signed registers, IWV, V1WV and V2WV at a rate defined by Bits 5,4 (ADC_FREQ) in the CONFIG register. The output frequency may be 8 kHz (CLKIN/512), 4 kHz (CLKIN/1024), 2 kHz (CLKIN/2048) or 1 kHz (CLKIN/4096) based on ADC_FREQ being equal to respective 00, 01, 10 or 11 when CLKIN is 4.096MHz .

The microcontroller may read the ADC output registers one at a time or in burst mode. See SPI Read Operation and SPI Read operation in burst mode sections for details.

ADC OUTPUT VALUES CRC

The ADE7913/ADE7912 computes every output cycle the cyclic redundancy check (CRC) of the ADC output values stored into IVW, V1WV and V2WV registers. The bits 5,4 (ADC_FREQ) in CONFIG register determine the ADC output frequency and therefore determine the update rate of the CRC. The CRC algorithm is based on the CRC-16-CCITT algorithm. The registers are introduced into a linear feedback shift register (LFSR) based generator as shown in Figure 34: one byte at a time, less significant byte first. Each byte is then considered with the most significant bit first. The 16-bit result is written in the ADC_CRC register.

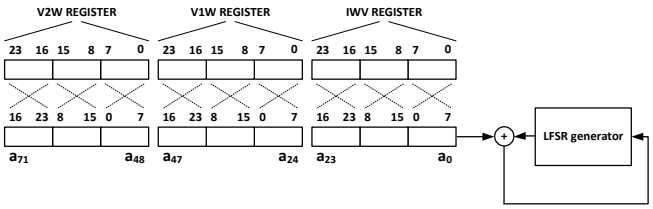

Figure 36. CRC calculation of the ADC output values

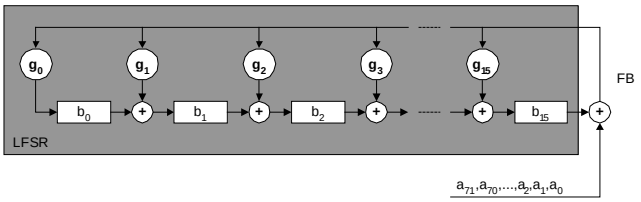

Figure 37. LFSR generator used for ADC_CRC calculation

Figure 35 shows how the LFSR works. The IWV, V1WV and V2WV registers form the bits [a_{71}, a_{70},…, a_0] used by LFSR. Bit a_0 is bit 7 of first register to enter LFSR; Bit a_{71} is the bit 16 of V2WV, the last register to enter LFSR. The formulas that govern LFSR are as follows:

$b_i(0) = 1$, i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant.

g_i, i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (6)$$

$$g_0 = g_5 = g_{12} = 1 \quad (7)$$

All of the other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (8)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (9)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, ..., 15 \quad (10)$$

Equation(10), Equation (11), and Equation (12) must be repeated for j = 1, 2, …, 72. The value written into the ADC_CRC register contains the Bit $b_i(72)$, i = 0, 1, …, 15.

The ADC_CRC register can be read executing an SPI register read access or as part of the SPI burst mode read operation. See SPI Read Operation and SPI Read operation in burst mode sections for more details.

TEMPERATURE SENSOR

The ADE7913/ADE7912 contains a temperature sensor that is multiplexed with the V2P input of the voltage channel. Bit 3 (TEMP_EN) of CONFIG register selects what the third ADC of the ADE7913 measures. If TEMP_EN bit is 0, its default value, the ADC measures the voltage between V2P and VM pins. If

TEMP_EN bit is 1, then the ADC measures the temperature sensor. In the ADE7912 case, the ADC always measures the temperature sensor and the state of bit TEMP_EN does not have any significance. In both cases, the conversion result is stored into V2WV register. The time it takes for the temperature sensor measurement to settle after the TEMP_EN bit is set to 1 is 5 ms.

The expression used to calculate the temperature in the microcontroller is:

$$\text{temp} = 8.72101\times10^{-5}\times\left(\text{V2WV}+\text{TEMPOS}\times2^{11}\right)-306.47$$

Where:

temp is the temperature value measured in Celsius degrees.

The gain used to convert the bit information provided by the ADE7913/ADE7912 into Celsius degrees has a default value of 8.72101 x 10^{-5} °C/LSB. The temperature measurement accuracy is ±5°C.

TEMPOS is a 8-bit signed read –only register in which the temperature sensor offset is stored. The offset information is calculated during the manufacturing process and it is stored with opposite sign into the ADE7913/ADE7912. One least significant bit (LSB) of TEMPOS register is equivalent to 2^{11} LSBs of V2WV register.

Instead of using the default value, the gain value may be calibrated as part of the overall meter calibration process. Just measure the temperature TEMP of every ADE7913/ADE7912, read V2WV register containing the temperature sensor reading of every ADE7913/ADE7912 and compute the gains as follows:

$$\text{Temperature gain} = \frac{TEMP}{V2WV + xTEMPOS\times2^{11}} \quad (11)$$

PROTECTING THE INTEGRITY OF CONFIGURATION REGISTERS

The configuration registers of the ADE7913/ADE7912 are of two categories: user accessible (CONFIG, EMI_CTRL, SYNC_SNAP, COUNTER0 and COUNTER1) and internal. The internal registers cannot be written and they must remain at their default values. To protect the integrity of all configuration registers, a write protection mechanism is available.

By default, the protection is disabled and the configuration registers can be written without restriction. When the protection is enabled, no writes to any configuration register is allowed. The registers can always be read, without restriction, independent of the write protection state.

To enable the protection, write 0xCA to the 8-bit Lock register. To disable the protection, write 0x9C to the 8-bit Lock register. It is recommended to enable the write protection after CONFIG and EMI_CTRL registers have been initialized. If any user accessible register has to be changed, for example during the synchronization process of multiple ADE7913/ADE7912s, simply disable the protection, change the value of the register and then re-enable the protection.

CONFIGURATION REGISTERS CRC

Every output cycle, the ADE7913/ADE7912 computes the CRC of the following registers: CONFIG, EMI_CTRL, TEMPOS, internal configuration registers, bit 2 (IC_PROT) of STATUS0 register and bit 7 of STATUS1 register. The CRC algorithm is called CRC-16-CCITT and is similar to the one presented in ADC Output Values CRC section. The 16-bit result is written in the CTRL_CRC register.

The input registers to the CRC circuit form a 64 bit array that is introduced bit by bit into a LFSR based generator, similar to Figure 34 and Figure 35: one byte at a time, least significant byte first. Each byte is then processed with the most significant bit first.

The formulas that govern LFSR are as follows:

$b_i(0) = 1$, i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant.

g_i, i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm in expressions (8) and (9).

$$FB(j) = a_{j-1} \text{ XOR } b_{31}(j-1) \quad (12)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (13)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, ..., 15 \quad (14)$$

Equation (14), Equation (15), and Equation (16) must be repeated for j = 1, 2, …, 64. The value written into the CTRL_CRC register contains the Bit $b_i(64)$, i = 0, 1, …, 15. Because each ADE7913/ADE7912 has a particular TEMPOS register value, each ADE7913/ADE7912 has a different CTRL_CRC register default value.

ADE7913/ADE7912 STATUS

The bits in STATUS0 and STATUS1 registers of the ADE7913/ADE7912 characterize the state of the device.

If the value of CTRL_CRC register changes, the bit 1 (CRC_STAT) is set to 1 in STATUS0 register. It clears to 0 when STATUS0 register is read.

After the configuration registers have been protected by writing 0xCA into LOCK register, bit 2 (IC_PROT) in STATUS0 register is set to 1. It clears to 0 when STATUS0 register is read, and it is set back to 1 at the next ADC output cycle.

At power up, or after a hardware or software reset, the ADE7913/ADE7912 signals the end of the reset period by clearing bit 0 (RESET_ON) to 0 in STATUS0 register.

If the ADC output values IWV, V1WV and V2WV are not read during an output cycle, the bit 3 (ADC_NA) in STATUS1 register becomes 1. It clears to 0 when the STATUS1 register is read.

The STATUS0 and STATUS1 registers can be read by executing an SPI register read access. STATUS0 can also be read as part of

the SPI burst mode read operation. See SPI Read Operation and SPI Read operation in burst mode sections for more details.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the life-time of the insulation structure within the ADE7913/ADE7912 devices. Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 9 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases. The insulation lifetime of the ADE7913/ADE7912 devices depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 36, Figure 37, and Figure 38 illustrate these different isolation voltage waveforms. Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 9 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 37 or Figure 38 should be treated as a bipolar ac waveform and its peak voltage limited to the 50-year lifetime voltage value listed in Table 9. The voltage presented in Figure 37 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

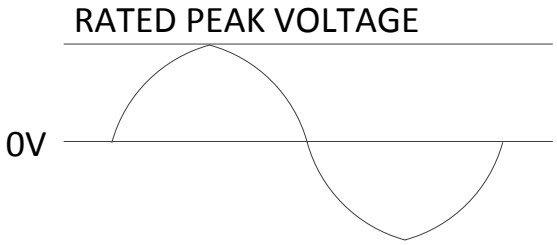

Figure 38. BipolarAC Waveform

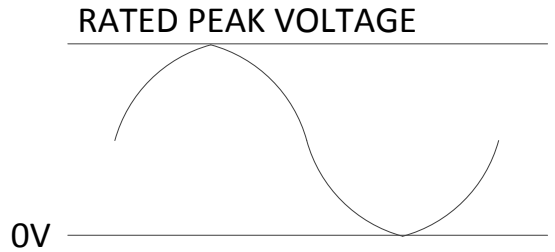

Figure 39.Unipolar AC Waveform

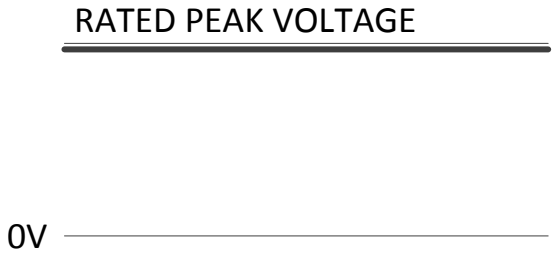

Figure 40. DC Waveform

ADE7913 EVALUATION BOARD

An evaluation board built upon the ADE7913 allows customers to quickly evaluate this IC. Visit www.analog.com/ADE7913 for details.

ADE7913/ADE7912 VERSION

The bits 2, 1, 0 (Version) in STATUS1 register identify the version of the ADE7913/ADE7912.

REGISTERS LIST

In the tables below, R means a register can be read, W means a register can be written. U means an unsigned register, and S means a signed register in twos complement format.

Table 14. Registers List

Address	Register Name	R/W	Bit Length	Type	Default Value	Description
0x0	IWV	R	24	S	0x000000	Instantaneous value of current I.
0x1	V1WV	R	24	S	0x000000	Instantaneous value of voltage V1.
0x2	V2WV	R	24	S	0x000000	Instantaneous value of voltage V2.
0x3	Reserved	R	24	S	0x000000	Reserved. This location always reads 0x000000.
0x4	ADC_CRC	R	16	U	N/A	CRC value of IWV, V1WV and V2WV registers. See ADC Output Values CRC section for details.
0x5	CTRL_CRC	R	16	U	N/A	CRC value of configuration registers. See Configuration registers CRC for details.
0x6	Reserved	R	16	S	0x0000	Reserved. This location always reads 0x0000.
0x7	CNT_SNAPSHOT	R	16	U	N/A	Snapshot value of the counter used in synchronization operation. See Synchronizing Multiple ADE7913/ADE7912 Devices section for details.
0x8	CONFIG	R/W	8	U	0	Configuration register. See Table 15 for details.
0x9	STATUS0	R	8	U	N/A	Status register. See Table 16 for details.
0xA	Lock	W	8	U	N/A	Memory protection register. See Protecting the integrity of configuration registers section and Table 17 for details.
0xB	SYNC_SNAP	W	8	U	N/A	Synchronization register. See Table 18 for details.
0xC	COUNTER0	R/W	8	U	N/A	Contains the least significant 8 bits of the internal synchronization counter.

Address	Register Name	R/W	Bit Length	Type	Default Value	Description
0xD	COUNTER1	R/W	8	U	N/A	COUNTER1[3:0] bits contain the most significant 4 bits of the synchronization counter. See Synchronizing Multiple ADE7913/ADE7912 Devices section for details.
0xE	EMI_CTRL	R/W	8	U	0xFF	EMI control register. Manages the PWM control block of the isolated dc-to-dc converter to reduce EMI emissions (see Table 19 and DC-TO-DC Converter section for details).
0xF	STATUS1	R	8	U	N/A	Status register. See Table 20 for details.
0x11,0x10	Reserved	R/W	8	U	0x00	These registers should not be written for proper operation.
0x13, 0x12	Reserved	R	8	U	0x00	Reserved registers.
0x14	Reserved					No functionality assigned at this address.
0x17, 0x16, 0x15	Reserved	R	8	U	0x00	Reserved registers.
0x18	TEMPOS	R	8	U	N/A	Temperature sensor offset

Table 15. Register CNT_SNAPSHOT (Address 0x7)

Bit Location	Bit Mnemonic	Default Value	Description
11:0	COUNTER	0x000	Snapshot value of the counter used in synchronization operation.
15:12	Reserved	0000	Reserved. These bits do not represent any functionality.

Table 16. Register CONFIG (Address 0x8)

Bit Location	Bit Mnemonic	Default Value	Description
0	CLKOUT_EN	0	Enables CLKOUT functionality at CLKOUT/ $\overline{\text{DREADY}}$ pin. When CLKOUT_EN=0, the default value, $\overline{\text{DREADY}}$ functionality is enabled. When CLKOUT_EN=1, CLKOUT functionality is enabled
1	Reserved	0	Reserved. This bit does not manage any functionality.
2	PWRDWN_EN	0	Shuts down the dc-to-dc converter. When PWRDWN_EN=0, the default value, the dc-to-dc converter is functional and the Σ-Δ modulators are active. When PWRDWN_EN=1, the dc-to-dc converter is turned off and the Σ-Δ modulators are shut down.
3	TEMP_EN	0	This bit selects the second voltage channel measurement. When this bit is 0, the default value, the voltage between pins V2P and VN is measured. When this bit is 1, the internal temperature sensor is measured (See Temperature Sensor for more details). In the ADE7912 case, the internal temperature sensor is always measured and this bit does not have any significance.
5,4	ADC_FREQ	00	These bits select the ADCs output frequency. 00=8KHz, 125µsec period. 01=4KHz, 250 µsec period.

Bit Location	Bit Mnemonic	Default Value	Description
			10=2KHz, 500 µsec period. 11=1KHz, 1msec period.
6	SWRST	0	When this bit is set to 1, a software reset is initiated. Bit clears itself to 0 after one CLKIN cycle.
7	BW	0	Selects the bandwidth of the digital low pass filter of the ADC. When BW=0, the default value, the bandwidth is 3.3 kHz. When BW=1, the bandwidth is 2 kHz. The bandwidth data is for CLKIN=4.096MHz and ADC output frequency of 8 kHz. See Analog-to-Digital Conversion section for details on how CLKIN and ADC output frequency influence the bandwidth selection.

Table 17. Register STATUS0 (Address 0x9)

Bit Location	Bit Mnemonic	Default Value	Description
0	RESET_ON	1	During reset, RESET_ON bit is 1. When the reset ends and the ADE7913/ADE7912 is ready to be configured, RESET_ON bit becomes 0.
1	CRC_STAT	0	If the CRC of the configuration registers changes value, CRC_STAT bit becomes 1.
2	IC_PROT	0	If the configuration registers have not been protected, this bit is 0. After the configuration registers have been protected, this bit becomes 1.
7:3	Reserved	0	Reserved. These bits do not represent any functionality.

Table 18. Register Lock (Address 0xA)

Bit Location	Bit Mnemonic	Default Value	Description
7:0	LOCK_KEY	00000000	When LOCK_KEY bits are equal to 0xCA, the configuration registers protection is enabled. When LOCK_KEY bits are equal to 0x9C, the protection is disabled and the configuration registers may be written. This is a write only register. If the address location is read, the value is 0x00.

Table 19. Register SYNC_SNAP (Address 0xB)

Bit Location	Bit Mnemonic	Default Value	Description
0	SYNC	0	When SYNC is set to 1 via a broadcast SPI write operation, the ADE7913/ADE7912s in the system generate ADC outputs in the same exact moment. The bit clears itself back to 0 after one CLKIN cycle. See Synchronizing Multiple ADE7913/ADE7912 Devices section for more details.
1	SNAP	0	When SNAP is set to 1 via a broadcast SPI write operation, the internal counters of the ADE7913/ADE7912s in the system are latched. The bit clears itself back to 0 after one CLKIN cycle. See Synchronizing Multiple ADE7913/ADE7912 Devices section for more details.
7:2	Reserved	0	Reserved. These bits do not represent any functionality.

Table 20. Register EMI_CTRL (Address 0xE)

Bit Location	Bit Mnemonic	Default Value	Description
0	SLOT0	1	Control the PWM Control block pulse during slot 0 of the CLKIN/4 clock. (see DC-TO-DC Converter section for details).
1	SLOT1	1	Control the PWM Control block pulse during slot 1 of the CLKIN/4 clock.
2	SLOT2	1	Control the PWM Control block pulse during slot 2 of the CLKIN/4 clock.
3	SLOT3	1	Control the PWM Control block pulse during slot 3 of the CLKIN/4 clock.
4	SLOT4	1	Control the PWM Control block pulse during slot 4 of the CLKIN/4 clock.
5	SLOT5	1	Control the PWM Control block pulse during slot 5 of the CLKIN/4 clock.
6	SLOT6	1	Control the PWM Control block pulse during slot 6 of the CLKIN/4 clock.
7	SLOT7	1	Control the PWM Control block pulse during slot 7 of the CLKIN/4 clock.

Table 21. Register STATUS1 (Address 0xF)

Bit Location	Bit Mnemonic	Default Value	Description
2:0	Version	0	The ADE7913/ADE7912 version number.

Bit Location	Bit Mnemonic	Default Value	Description
3	ADC_NA	0	If the ADCs outputs have not been accessed during one ADC output period, ADC_NA bit becomes 1. When STATUS1 register is read, the bit is cleared to 0.
6:3	Reserved	0	Reserved. These bits do not represent any functionality.
7	Reserved	0	Reserved. Internal functionality is associated with this bit.

OUTLINE DIMENSIONS

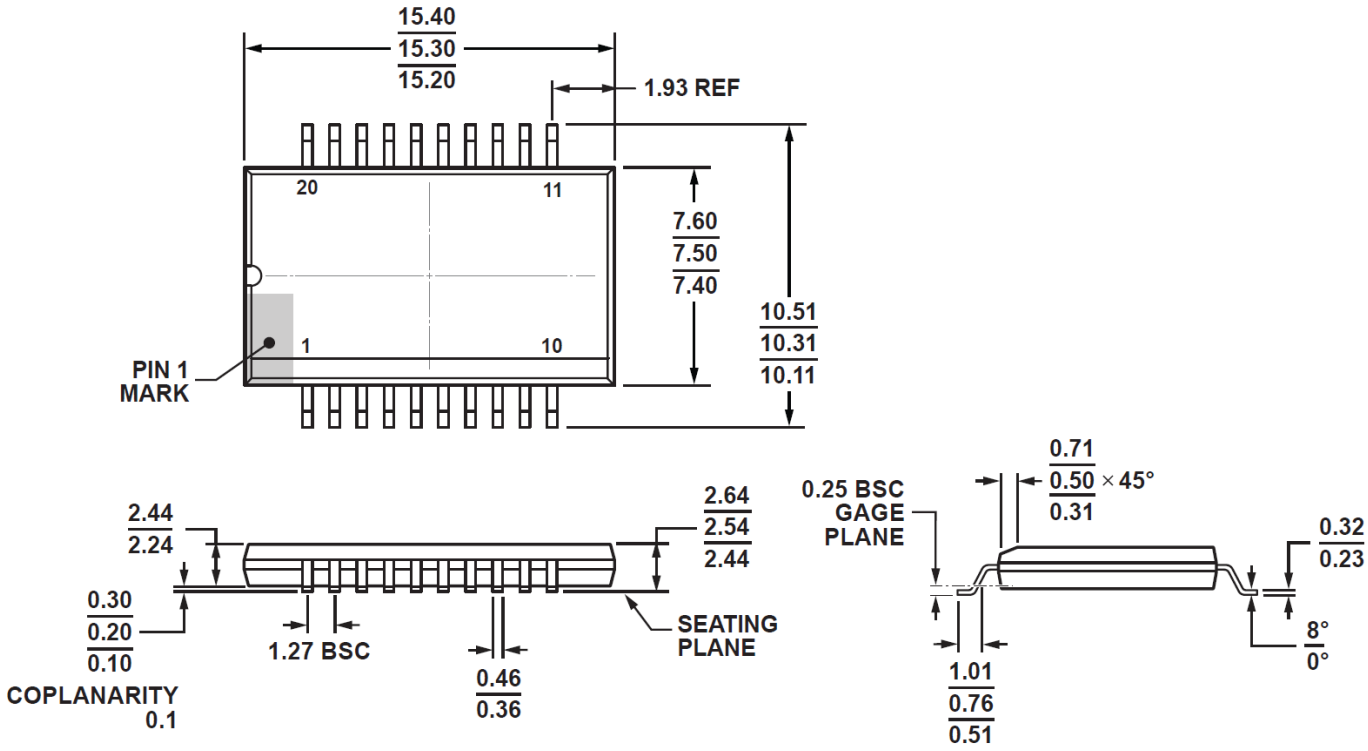

Figure 41. 20-Lead Standard Small Outline Package, with increased Creepage [SOIC_IC]
Wide Body, (RI-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADE7913ARIZ	–40°C to +85°C	20-Lead SOIC_W	RI-20-1
ADE7913ARIZ-RL	–40°C to +85°C	20-Lead SOIC_W, 13" Tape and Reel	RI-20-1
ADE7912ARIZ	–40°C to +85°C	20-Lead SOIC_W	RI-20-1
ADE7912ARIZ-RL	–40°C to +85°C	20-Lead SOIC_W, 13" Tape and Reel	RI-20-1
EVAL-ADE7913EBZ		Evaluation Board	

NOTES

PR11115-0-4/13(PrL)