

## FEATURES

**0.58  $\Omega$  typical on resistance**  
**0.82  $\Omega$  maximum on resistance at 85°C**  
**1.8 V to 5.5 V single supply**  
**High current carrying capability: 250 mA continuous**  
**Rail-to-rail switching operation**  
**Fast-switching times: <20 ns**  
**Typical power consumption: <0.1  $\mu$ W**  
**2.1 mm  $\times$  2.1 mm mini LFCSP**

## APPLICATIONS

**Cellular phones**  
**PDA's**  
**MP3 players**  
**Power routing**  
**Battery-powered systems**  
**PCMCIA cards**  
**Modems**  
**Audio and video signal routing**  
**Communication systems**

## GENERAL DESCRIPTION

The ADG858 is a low voltage CMOS device containing four single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of less than 0.82  $\Omega$  over the full temperature range. The ADG858 is fully specified for 4.2 V to 5.5 V and 2.7 V to 3.6 V supply operation.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG858 exhibits break-before-make switching action.

The ADG858 is available in a 2.1 mm  $\times$  2.1 mm, 16-lead mini LFCSP. This tiny package makes the part ideal for space-constrained applications, such as handsets, PDA's, and MP3's.

## FUNCTIONAL BLOCK DIAGRAM

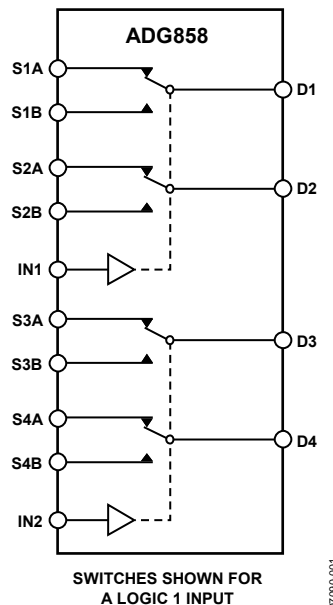


Figure 1.

## PRODUCT HIGHLIGHTS

1. <0.82  $\Omega$  over the full temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .
2. Single 1.8 V to 5.5 V operation.
3. Compatible with 1.8 V CMOS logic.
4. High current handling capability (250 mA continuous current per channel).
5. Low THD + N: 0.06% typical.
6. 2.1 mm  $\times$  2.1 mm, 16-lead mini LFCSP.

### Rev. A

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REVISION HISTORY

8/08—Rev. 0 to Rev. A	
Changes to Features Section.....	1

8/08—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 4.2\text{ V to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	+25°C	–40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V <sub>DD</sub>	V	
On Resistance, R <sub>ON</sub>	0.58		Ω typ	V <sub>DD</sub> = 4.2 V, V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = 100 mA, see Figure 16
	0.72	0.82	Ω max	
On-Resistance Match Between Channels, ΔR <sub>ON</sub>	0.04		Ω typ	V <sub>DD</sub> = 4.2 V, V <sub>S</sub> = 2 V, I <sub>S</sub> = 100 mA
		0.14	Ω max	
On-Resistance Flatness, R <sub>FLAT (ON)</sub>	0.12		Ω typ	V <sub>DD</sub> = 4.2 V, V <sub>S</sub> = 0 V to V <sub>DD</sub>
		0.26	Ω max	I <sub>S</sub> = 100 mA
LEAKAGE CURRENTS				
Source Off Leakage, I <sub>S</sub> (Off)	±10		pA typ	V <sub>DD</sub> = 5.5 V V <sub>S</sub> = 0.6 V/4.2 V, V <sub>D</sub> = 4.2 V/0.6 V, see Figure 17
Channel On Leakage, I <sub>D</sub> , I <sub>S</sub> (On)	±10		pA typ	V <sub>S</sub> = V <sub>D</sub> = 0.6 V or 4.2 V, see Figure 18
DIGITAL INPUTS				
Input High Voltage, V <sub>INH</sub>		2.0	V min	
Input Low Voltage, V <sub>INL</sub>		0.8	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>	0.004		μA typ	V <sub>IN</sub> = V <sub>GND</sub> or V <sub>DD</sub>
		0.05	μA max	
Digital Input Capacitance, C <sub>IN</sub>	2		pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>				
t <sub>ON</sub>	20		ns typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF
	27	36	ns max	V <sub>S</sub> = 3 V/0 V, see Figure 19
t <sub>OFF</sub>	8		ns typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF
	12	13	ns max	V <sub>S</sub> = 3 V, see Figure 19
Break-Before-Make Time Delay, t <sub>BBM</sub>	14		ns typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF
		9	ns min	V <sub>S1</sub> = V <sub>S2</sub> = 1.5 V, see Figure 20
Charge Injection	45		pC typ	V <sub>S</sub> = 1.5 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF, see Figure 21
Off Isolation	–67		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz, see Figure 22
Channel-to-Channel Crosstalk	–85		dB typ	S1A to S2A/S1B to S2B/S3A to S4A/S3B to S4B, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz, see Figure 25
	–67		dB typ	S1A to S1B/S2A to S2B/S3A to S3B/S4A to S4B, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz, see Figure 24
Total Harmonic Distortion, THD + N	0.06		%	R <sub>L</sub> = 32 Ω, f = 20 Hz to 20 kHz, V <sub>S</sub> = 2 V p-p
Insertion Loss	–0.05		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, see Figure 23
–3 dB Bandwidth	70		MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, see Figure 23
C <sub>S</sub> (Off)	25		pF typ	
C <sub>D</sub> , C <sub>S</sub> (On)	75		pF typ	
POWER REQUIREMENTS				
I <sub>DD</sub>	0.003		μA typ	V <sub>DD</sub> = 5.5 V Digital inputs = 0 V or 5.5 V
		1	μA max	

<sup>1</sup> Guaranteed by design, not subject to production test.

# ADG858

$V_{DD} = 2.7 \text{ V}$  to  $3.6 \text{ V}$ ,  $GND = 0 \text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	+25°C	–40°C to +85°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 to $V_{DD}$	V	
On Resistance, $R_{ON}$	1		$\Omega$ typ	$V_{DD} = 2.7 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 100 \text{ mA}$ , see Figure 16
	1.35	1.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.05		$\Omega$ typ	$V_{DD} = 2.7 \text{ V}$ , $V_S = 0.7 \text{ V}$ , $I_S = 100 \text{ mA}$
		0.15	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.35		$\Omega$ typ	$V_{DD} = 2.7 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 100 \text{ mA}$
		0.79	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage $I_S$ (Off)	$\pm 10$		pA typ	$V_{DD} = 3.6 \text{ V}$ $V_S = 0.6 \text{ V}/3.3 \text{ V}$ , $V_D = 3.3 \text{ V}/0.6 \text{ V}$ , see Figure 17
Channel On Leakage $I_D$ , $I_S$ (On)	$\pm 10$		pA typ	$V_S = V_D = 0.6 \text{ V}$ or $3.3 \text{ V}$ , see Figure 18
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		1.35	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				
$I_{INL}$ or $I_{INH}$	0.004		$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
		0.05	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>				
$t_{ON}$	30		ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	50	59	ns max	$V_S = 1.5 \text{ V}/0 \text{ V}$ , see Figure 19
$t_{OFF}$	9		ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	14	15	ns max	$V_S = 1.5 \text{ V}$ , see Figure 19
Break-Before-Make Time Delay, $t_{BBM}$	25		ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
		11	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$ , see Figure 20
Charge Injection	35		pC typ	$V_S = 1.5 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 21
Off Isolation	–67		dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ , see Figure 22
Channel-to-Channel Crosstalk	–85		dB typ	S1A to S2A/S1B to S2B/S3A to S4A/S3B to S4B, $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ , see Figure 25
	–67		dB typ	S1A to S1B/S2A to S2B/S3A to S3B/S4A to S4B, $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ , see Figure 24
Total Harmonic Distortion, THD + N	0.1		%	$R_L = 32 \Omega$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , $V_S = 1.5 \text{ V}$ p-p
Insertion Loss	–0.06		dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 23
–3 dB Bandwidth	70		MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 23
$C_S$ (Off)	25		pF typ	
$C_D$ , $C_S$ (On)	75		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.003		$\mu\text{A}$ typ	$V_{DD} = 3.6 \text{ V}$ Digital inputs = $0 \text{ V}$ or $3.6 \text{ V}$
		1	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to GND	−0.3 V to +6 V
Analog Inputs <sup>1</sup>	−0.3 V to $V_{DD} + 0.3$ V
Digital Inputs <sup>1</sup>	−0.3 V to $V_{DD}$ or 10 mA, whichever occurs first
Peak Current, S or D	500 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	250 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead Mini LFCSP	
$\theta_{JA}$ Thermal Impedance, 3-Layer Board	84.9°C/W
Reflow Soldering, Pb-Free	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

### ESD CAUTION



#### **ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG858

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

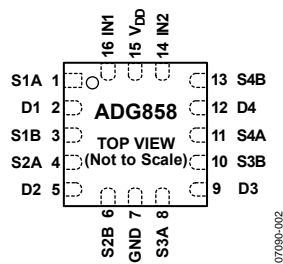


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 8, 10, 11, 13	S1A, S1B, S2A, S2B, S3A, S3B, S4A, S4B	Source Terminal. Can be an input or output.
2, 5, 9, 12	D1, D2, D3, D4	Drain Terminal. Can be an input or output.
7	GND	Ground (0 V) Reference.
14, 16	IN1, IN2	Logic Control Input.
15	V <sub>DD</sub>	Most Positive Power Supply Potential.

Table 5. ADG858 Truth Table

Logic (IN1/IN2)	Switch A (S1A/S2A/S3A/S4A)	Switch B (S1B/S2B/S3B/S4B)
0	Off	On
1	On	Off

# TYPICAL PERFORMANCE CHARACTERISTICS

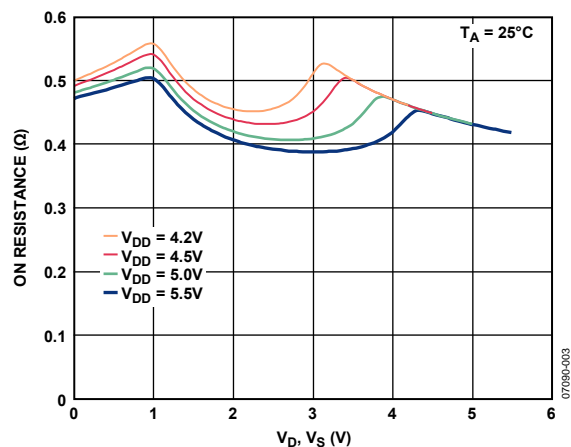


Figure 3. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 4.2$  V to 5.5 V

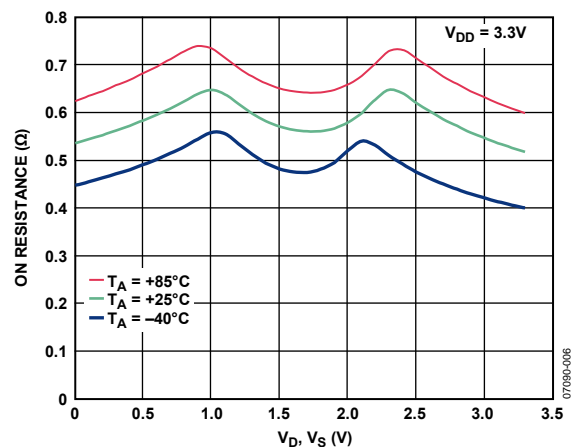


Figure 6. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 3.3$  V

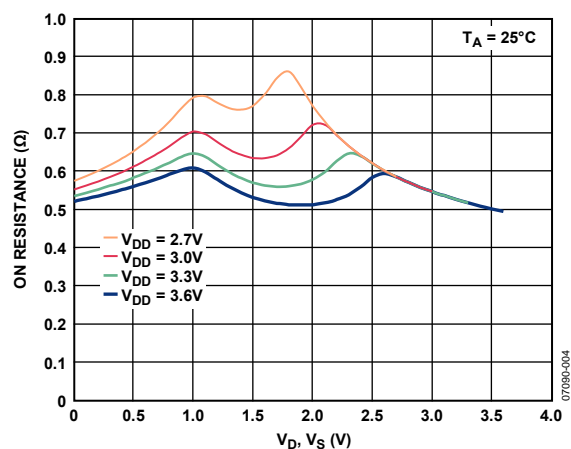


Figure 4. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.7$  V to 3.6 V

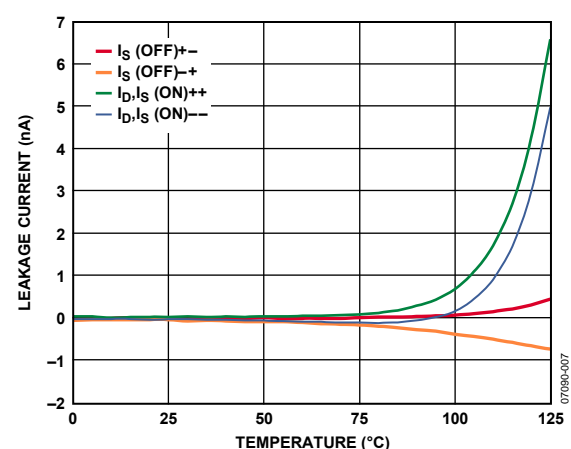


Figure 7. Leakage Current vs. Temperature,  $V_{DD} = 5$  V

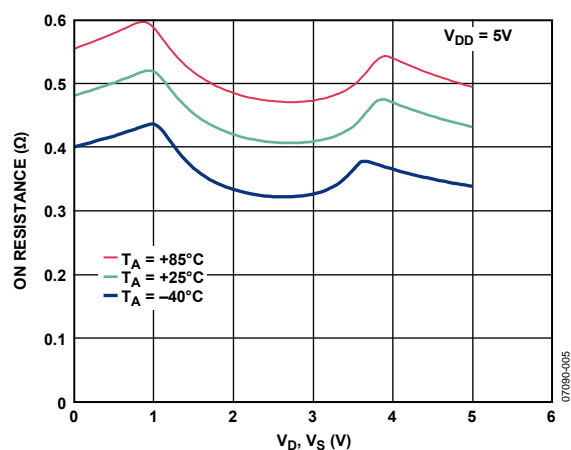


Figure 5. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 5$  V

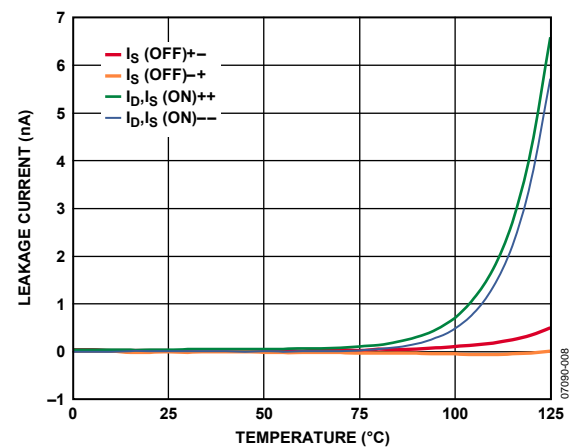


Figure 8. Leakage Current vs. Temperature,  $V_{DD} = 3.3$  V

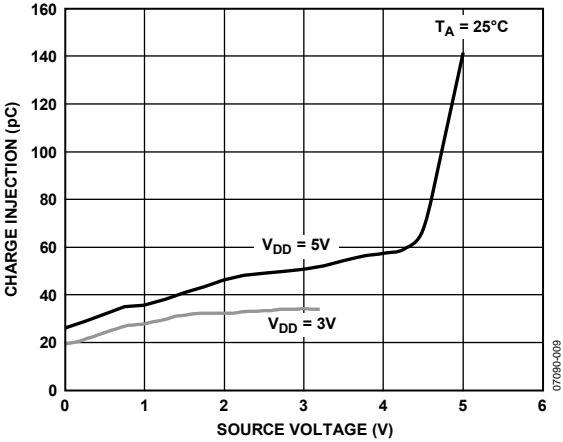


Figure 9. Charge Injection vs. Source Voltage

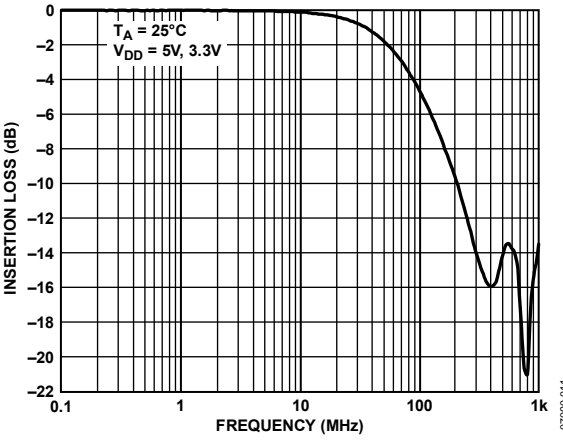


Figure 11. Bandwidth

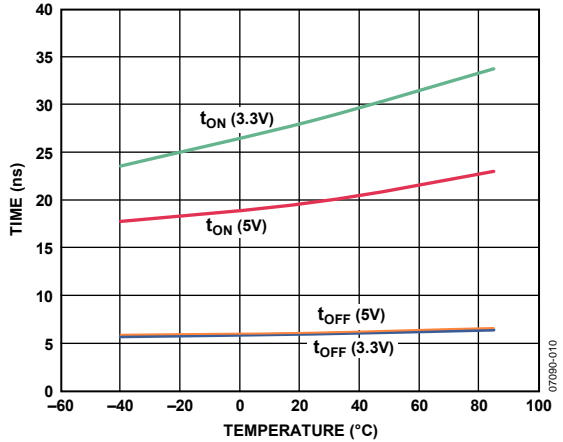


Figure 10.  $t_{ON}/t_{OFF}$  Times vs. Temperature

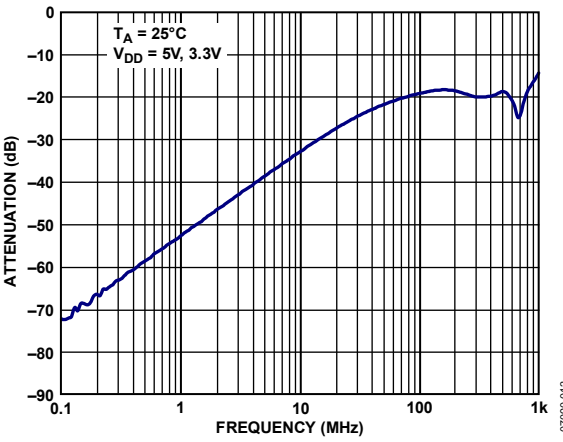


Figure 12. Off Isolation vs. Frequency



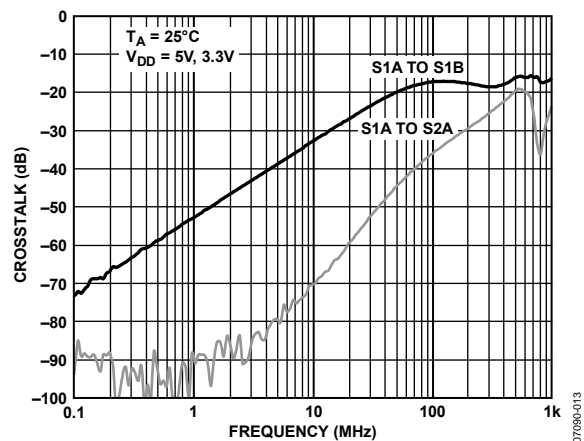


Figure 13. Crosstalk vs. Frequency

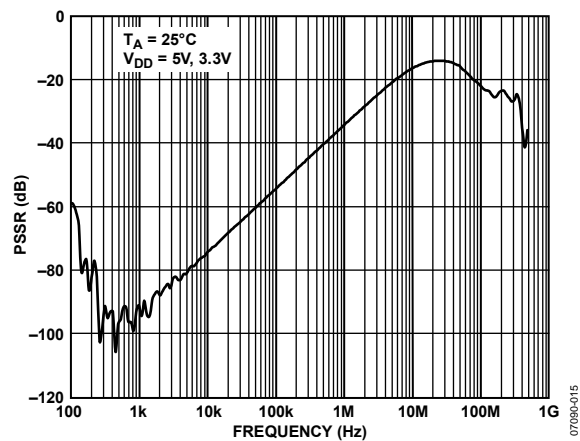


Figure 15. PSSR vs. Frequency

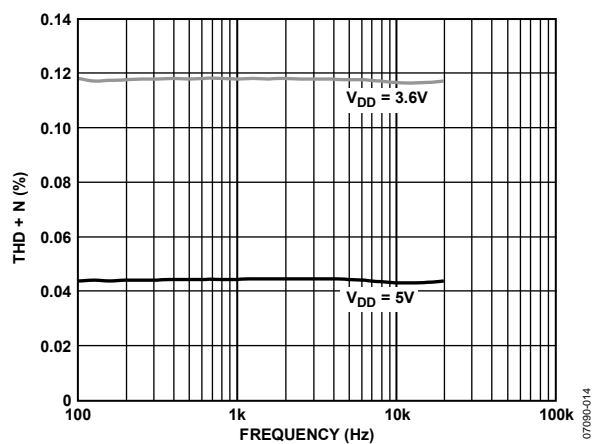


Figure 14. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

## TEST CIRCUITS

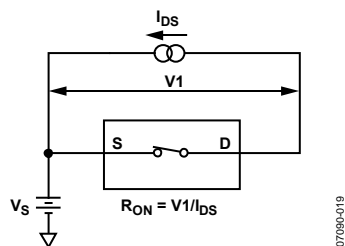


Figure 16. On Resistance

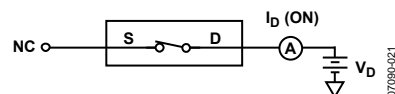


Figure 18. On Leakage

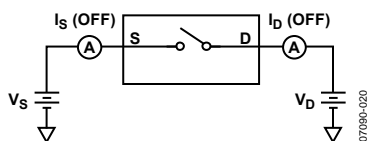


Figure 17. Off Leakage

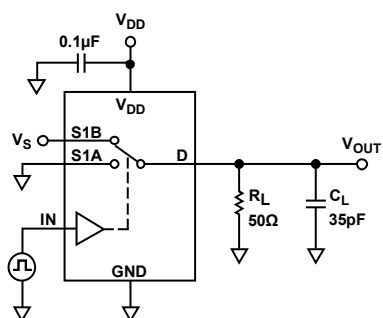


Figure 19. Switching Times,  $t_{ON}$ ,  $t_{OFF}$

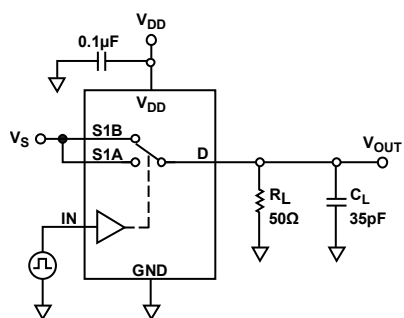
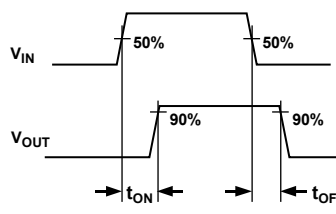


Figure 20. Break-Before-Make Time Delay,  $t_{BBM}$

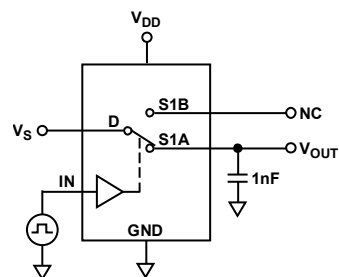
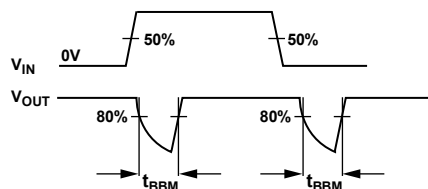
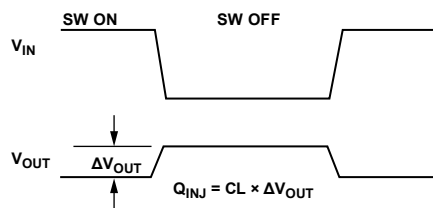


Figure 21. Charge Injection



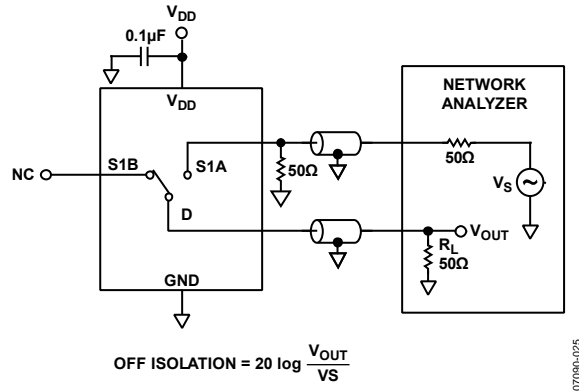


Figure 22. Off Isolation

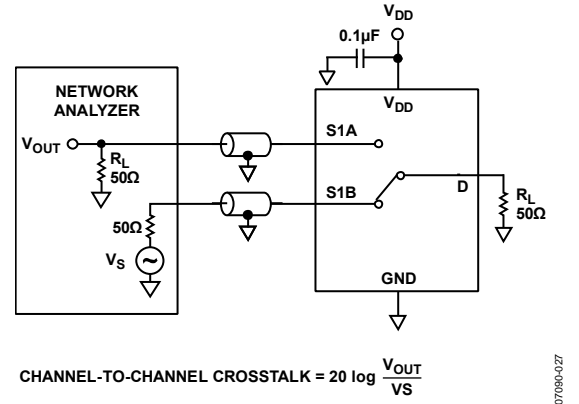


Figure 24. Channel-to-Channel Crosstalk (S1A to S1B)

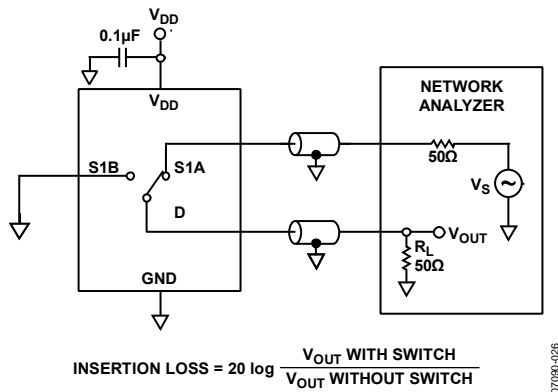


Figure 23. Bandwidth

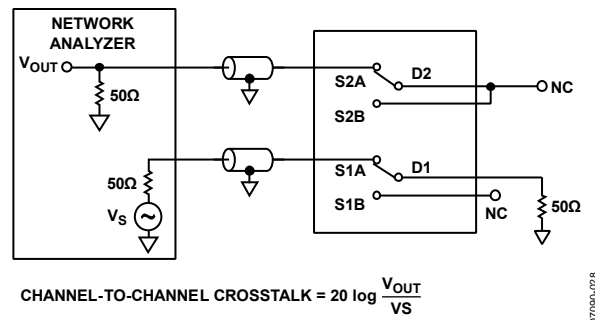


Figure 25. Channel-to-Channel Crosstalk (S1A to S2A)

## TERMINOLOGY

### **I<sub>DD</sub>**

Positive supply current.

### **V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on Terminal D and Terminal S.

### **R<sub>ON</sub>**

Ohmic resistance between Terminal D and Terminal S.

### **R<sub>FLAT</sub> (ON)**

The difference between the maximum and minimum values of on resistance as measured on the switch.

### **ΔR<sub>ON</sub>**

On resistance match between any two channels.

### **I<sub>S</sub> (Off)**

Source leakage current with the switch off.

### **I<sub>D</sub> (Off)**

Drain leakage current with the switch off.

### **I<sub>D</sub>, I<sub>S</sub> (On)**

Channel leakage current with the switch on.

### **V<sub>INL</sub>**

Maximum input voltage for Logic 0.

### **V<sub>INH</sub>**

Minimum input voltage for Logic 1.

### **I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

### **C<sub>S</sub> (Off)**

Off switch source capacitance. Measured with reference to ground.

### **C<sub>D</sub> (Off)**

Off switch drain capacitance. Measured with reference to ground.

### **C<sub>D</sub>, C<sub>S</sub> (On)**

On switch capacitance. Measured with reference to ground.

### **C<sub>IN</sub>**

Digital input capacitance.

### **t<sub>ON</sub>**

Delay time between the 50% and 90% points of the digital input and switch on condition.

### **t<sub>OFF</sub>**

Delay time between the 50% and 90% points of the digital input and switch off condition.

### **t<sub>BEM</sub>**

On or off time measured between the 80% points of both switches when switching from one to another.

### **Charge Injection**

Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

### **Off Isolation**

Measure of unwanted signal coupling through an off switch.

### **Crosstalk**

Measure of unwanted signal that is coupled from one channel to another because of parasitic capacitance.

### **–3 dB Bandwidth**

Frequency at which the output is attenuated by 3 dB.

### **On Response**

Frequency response of the on switch.

### **Insertion Loss**

The loss due to the on resistance of the switch.

### **THD + N**

Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

## OUTLINE DIMENSIONS

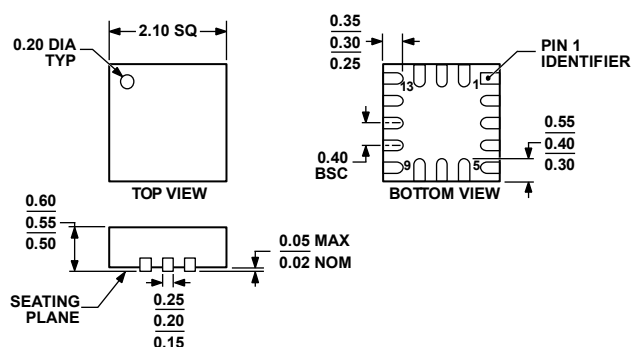


Figure 26. 16-Lead Lead Frame Chip Scale Package [LFCSP\_UQ]  
 2.10 mm × 2.10 mm Body, Ultra Thin Quad  
 (CP-16-15)  
 Dimensions shown in millimeters

032807-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG858BCPZ-REEL <sup>1</sup>	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_UQ]	CP-16-15	11
ADG858BCPZ-REEL7 <sup>1</sup>	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_UQ]	CP-16-15	11

<sup>1</sup> Z = RoHS Compliant Part.

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**NOTES**

## NOTES

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