Charge Pump Regulator for Color TFT Panel

ADM8832

FEATURES

3 output voltages (+5.1 V, +15.3 V, −10.2 V) from one 3 V input supply
Power efficiency optimized for use with TFT in mobile phones
Low quiescent current
Low shutdown current (<1 µA)
Fast transient response
Shutdown function
Power saving during blanking period
Option to use external ldo

APPLICATIONS

Handheld instruments
TFT LCD panels
Cellular phones

FUNCTIONAL BLOCK DIAGRAM

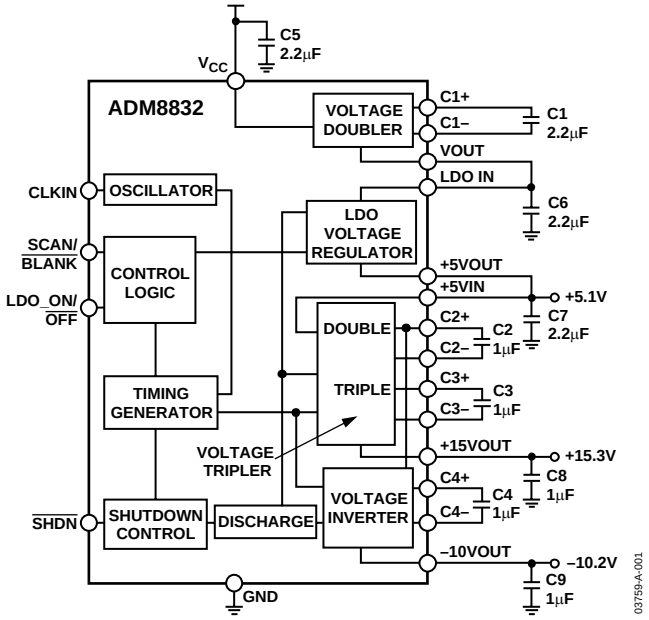

Figure 1.

GENERAL DESCRIPTION

The ADM8832 is a charge pump regulator used for color thin film transistor (TFT) liquid crystal displays (LCD). Using charge pump technology, the device can be used to generate three output voltages (+5.1 V ±2%, +15.3 V, −10.2 V) from a single 3 V input supply. These outputs are then used to provide supplies for the LCD controller (+5.1 V) and the gate drives for the transistors in the panel (+15.3 V and −10.2 V). Only a few external capacitors are needed for the charge pumps. An efficient low dropout voltage regulator also ensures that the power efficiency is high and provides a low ripple 5.1 V output. This LDO can be shut down and an external LDO used to regulate the 5 V doubler output and drive the input to the charge pump section, which generates the +15.3 V and −10.2 V outputs if so required by the user.

The ADM8832 has an internal 100 kHz oscillator for use in scanning mode, but the part must be clocked by an external clock source in blanking (low current) mode. The internal oscillator is used to clock the charge pumps during scanning mode where the current is highest. During blanking periods, the ADM8832 switches to an external, lower frequency clock. This allows the user to vary the frequency and maximize power efficiency during blanking periods. The tolerances on the output voltages are seamlessly maintained when switching from scanning mode to blanking mode or vice versa.

The ADM8832 power saving features include low power shutdown and reduced quiescent current consumption during the blanking periods. The 5.1 V output consumes the most power, so power efficiency is also maximized on this output with an oscillator enabling scheme (Green Idle™). This effectively senses the load current that is flowing and turns on the charge pump only when charge needs to be delivered to the 5 V pump doubler output.

The ADM8832 is fabricated using CMOS technology for minimal power consumption. The part is packaged in a 20-lead LFCSP (lead frame chip scale package).

Rev. A

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REVISION HISTORY

4/04—Changed from Rev. 0 to Rev. A

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7/03—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted; C1, C5, C6, C7 = 2.2 µF, C2, C3, C4, C8, C9 = 1 µF, CLKIN = 1 kHz in blanking mode.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
INPUT VOLTAGE, V_{CC}	2.6		3.6	V	
SUPPLY CURRENT, I_{CC}		150	400	µA	Unloaded, Scanning Period
		70	140	µA	Unloaded, Blanking Period
			1	µA	Shutdown Mode, T_A = 25°C
+5.1 V OUTPUT					
Output Voltage	5.0	5.1	5.2	V	I_L = 10 µA to 8 mA
Output Current		4	5	mA	Scanning Period
		5	8	mA	Scanning Period, V_{CC} > 2.7 V
		50	200	µA	Blanking Period
Power Efficiency		80		%	V_{CC} = 3 V, I_L = 5 mA (Scanning)
		70		%	V_{CC} = 3 V, I_L = 200 µA (Blanking)
Output Ripple		10		mV p-p	8 mA Load
Transient Response		5		µs	I_L Stepped from 10 µA to 8 mA
+15.3 V OUTPUT					
Output Voltage	14.4	15.3	15.6	V	I_L = 1 µA to 100 µA
Output Current		50	100	µA	Scanning Period
		1	10	µA	Blanking Period
Output Ripple		50		mV p-p	I_L = 100 µA
−10.2 V OUTPUT					
Output Voltage	−10.4	−10.2	−9.6	V	I_L = −1 µA to −100 µA
Output Current	−100	−50		µA	Scanning Period
	−10	−1		µA	Blanking Period
Output Ripple		50		mV p-p	I_L = −100 µA
POWER EFFICIENCY		90		%	Relative to 5.1 V Output, I_L = 100 µA (Scanning)
(+15.3 V and −10.2 V Outputs)		80		%	Relative to 5.1 V Output, I_L = 10 µA (Blanking)
CHARGE PUMP FREQUENCY	60	100	140	kHz	Scanning Period
CONTROL PINS					
$\overline{SHDN}$					
Input Voltage, V_{SHDN}			0.3 V_{CC}	V	$\overline{SHDN}$ Low = Shutdown Mode
	0.7 V_{CC}			V	$\overline{SHDN}$ High = Normal Mode
Digital Input Current			±1	µA	
Digital Input Capacitance[1]			10	pF	
SCAN/$\overline{BLANK}$					
Input Voltage			0.3 V_{CC}	V	Low = $\overline{BLANK}$ Period
	0.7 V_{CC}			V	High = SCAN Period
Digital Input Current			±1	µA	
Digital Input Capacitance[1]			10	pF	
LDO_ON/$\overline{OFF}$					
Input Voltage			0.3 V_{CC}	V	Low = External LDO
	0.7 V_{CC}			V	High = Internal LDO
Digital Input Current			±1	µA	
Digital Input Capacitance[1]			10	pF	

Footnotes after table.

Parameter	Min	Typ	Max	Unit	Test Conditions
CLKIN					
Minimum Frequency	0.9	1		kHz	Duty Cycle = 50%, Rise/Fall Times = 20 ns
Input Voltage					
V_{IL}			0.3 V_{CC}	V	
V_{IH}	0.7 V_{CC}			V	
Digital Input Current			±1	µA	
Digital Input Capacitance[1]			10	pF	

[1] Guaranteed by design. Not 100% production tested.
Specifications are subject to change without notice.

TIMING SPECIFICATIONS

V_{CC} = 2.6 V to 3.6 V, T_A = −40°C to +85°C, unless otherwise noted; C1, C5, C6, C7 = 2.2 µF, C2, C3, C4, C8, C9 = 1 µF, CLKIN = 1 kHz in blanking mode.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-UP SEQUENCE					
+5 V Rise Time, t_{R5V}		300		µs	10% to 90%, Figure 17
+15 V Rise Time, t_{R15V}		8		ms	10% to 90%, Figure 17
−10 V Fall Time, t_{F10V}		12		ms	90% to 10%, Figure 17
Delay between −10 V Fall and +15 V, t_{DELAY}		3		ms	Figure 17
POWER-DOWN SEQUENCE					
+5 V Fall Time, t_{F5V}		75		ms	90% to 10%, Figure 17
+15 V Fall Time, t_{F15V}		40		ms	90% to 10%, Figure 17
−10 V Rise Time, t_{R10V}		40		ms	10% to 90%, Figure 17

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Ratings
Supply Voltage	−0.3 V to +4.0 V
Input Voltage to Digital Inputs	−0.3 V to +4.0 V
Output Short Circuit Duration to GND	10 sec
Output Voltage	
+5.1 V Output	−0.3 V to +6 V
−10.2 V Output	−12 V to +0.3 V
+15.3 V Output	−0.3 V to +17 V
Operating Temperature Range	−40°C to +85°C
Power Dissipation (Derate 33 mW/°C above 25°C)	3.55 W
Storage Temperature Range	−65°C to +150°C
ESD	Class I

THERMAL CHARACTERISTICS

20-Lead LFCSP:
θ_{JA} = 31°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

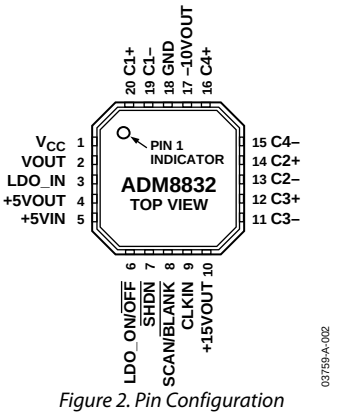


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{CC}	Positive Supply Voltage Input. Connect this pin to 3 V supply with a 2.2 µF decoupling capacitor.
2	VOUT	Voltage Doubler Output. This is derived by doubling the 3 V supply. A 2.2 µF capacitor to ground is required on this pin.
3	LDO_IN	Voltage Regulator Input. The user has the option to bypass this circuit using the LDO_ON/$\overline{OFF}$ pin.
4	+5VOUT	+5.1 V Output Pin. This is derived by doubling and regulating the +3 V supply. A 2.2 µF capacitor to ground is required on this pin to stabilize the regulator.
5	+5VIN	+5.1 V Input Pin. This is the input to the voltage tripler and doubler inverter charge pump circuits.
6	LDO_ON/$\overline{OFF}$	Control Logic Input. 3 V CMOS logic. A logic high selects the internal LDO for regulation of the 5 V voltage doubler output. A logic low isolates the internal LDO from the rest of the charge pump circuits. This allows the use of an external LDO to regulate the 5 V voltage doubler output. The output of this LDO is then fed back into the voltage tripler and doubler/inverter circuits of the ADM8832.
7	$\overline{SHDN}$	Digital Input. 3 V CMOS logic. Active low shutdown control. This pin shuts down the timing generator and enables the discharge circuit to dissipate the charge on the voltage outputs, thus driving them to 0 V.
8	SCAN/$\overline{BLANK}$	Drive Mode Input. 3 V CMOS logic. A logic high places the part in scan (high current) mode, and the charge pump is driven by the internal oscillator. A logic low places the part in blanking (low current) mode, and the charge pump is driven by the (slower) external oscillator. This is a power saving feature on the ADM8832.
9	CLKIN	External CLOCK Input. During a blanking period, the oscillator circuit selects this pin to drive the charge pump circuit. This is at a lower frequency than the internal oscillator, resulting in lower quiescent current consumption, thus saving power.
10	+15VOUT	+15.3 V Output Pin. This is derived by tripling the +5.1 V regulated output. A 1 µF capacitor is required on this pin.
11, 12	C3–, C3+	External capacitor C3 is connected between these pins. A 1 µF capacitor is recommended.
13, 14	C2–, C2+	External capacitor C2 is connected between these pins. A 1 µF capacitor is recommended.
15, 16	C4–, C4+	External capacitor C4 is connected between these pins. A 1 µF capacitor is recommended.
17	−10VOUT	−10.2 V Output Pin. This is derived by doubling and inverting the +5.1 V regulated output. A 1 µF capacitor is required on this pin.
18	GND	Device Ground Pin.
19, 20	C1–, C1+	External capacitor C1 is connected between these pins. A 2.2 µF capacitor is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

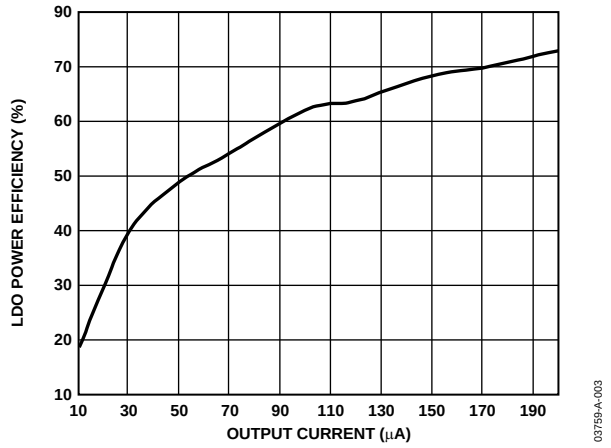


Figure 3. LDO Efficiency in Blanking Mode with V_{CC} = 3 V

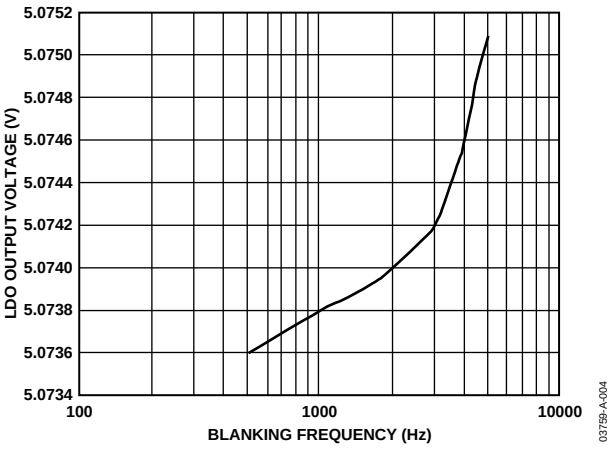


Figure 4. LDO Output Voltage (Unloaded) vs. Blanking Mode Frequency

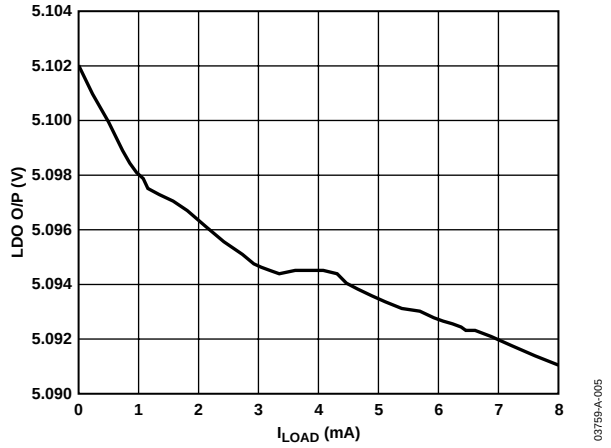


Figure 5. LDO O/P Voltage vs. Load Current in Scanning Mode, V_{CC} = 3.3 V

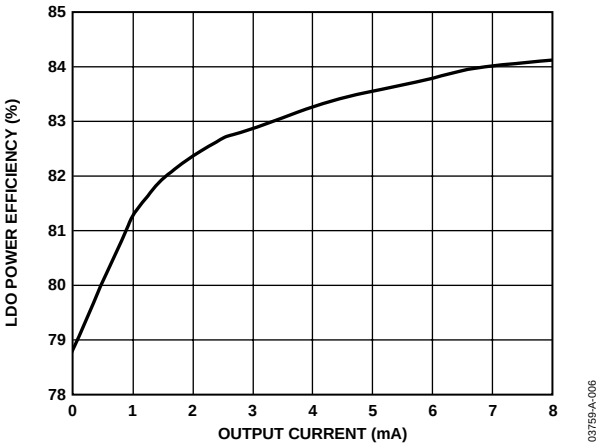


Figure 6. LDO Efficiency in Scanning Mode with V_{CC} = 3 V

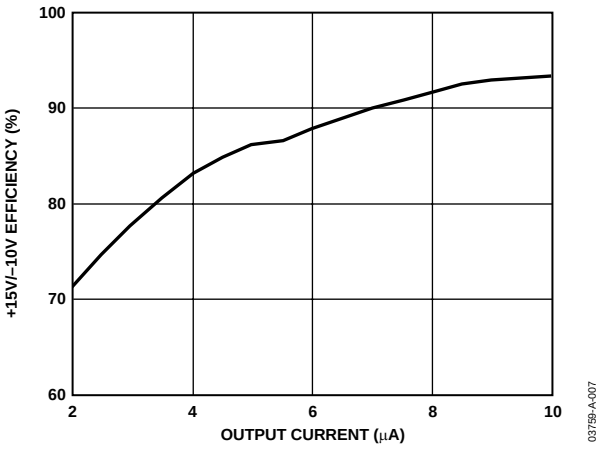


Figure 7. +15 V/−10 V Efficiency vs. Output Current in Blanking Mode, V_{CC} = 3 V

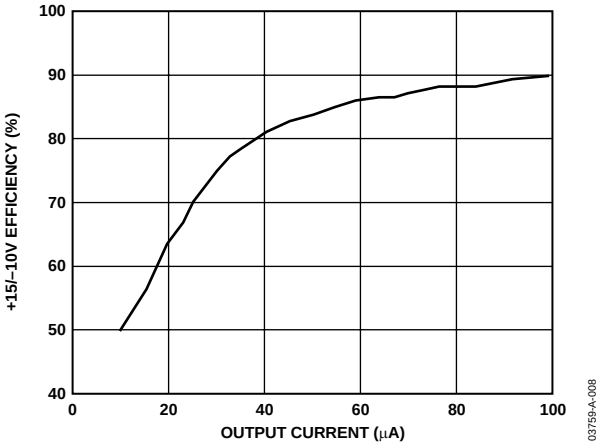


Figure 8. +15 V/−10 V Efficiency vs. Output Current in Scanning Mode, V_{CC} = 3 V

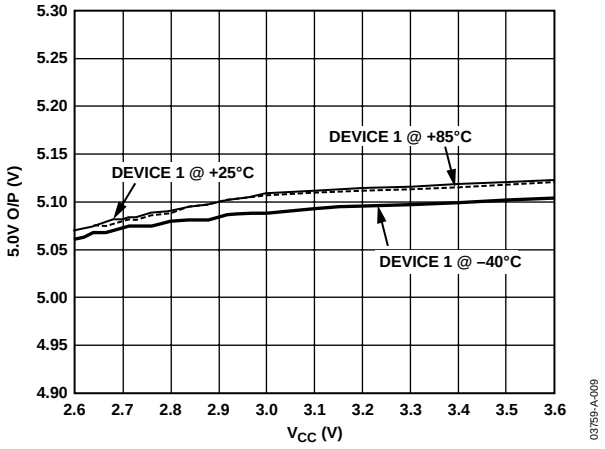


Figure 9. LDO Variation over Supply and Temperature

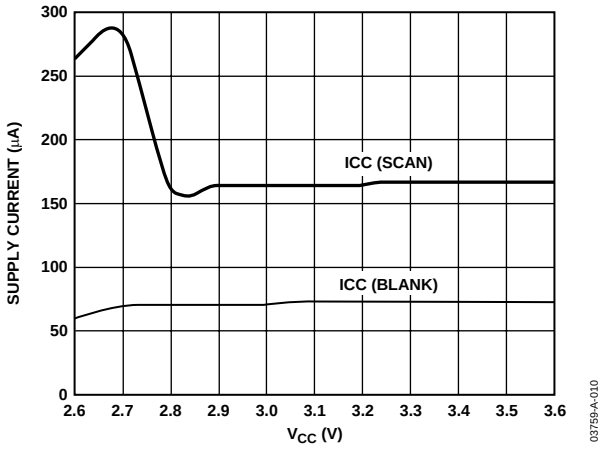


Figure 10. Supply Current vs. Voltage

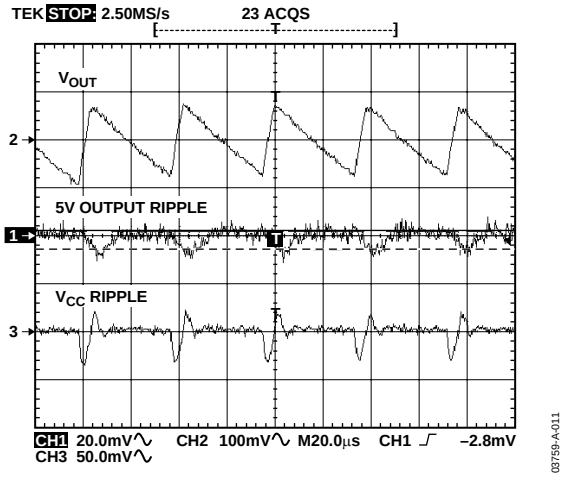


Figure 11. Output Ripple on LDO (5 V Output)

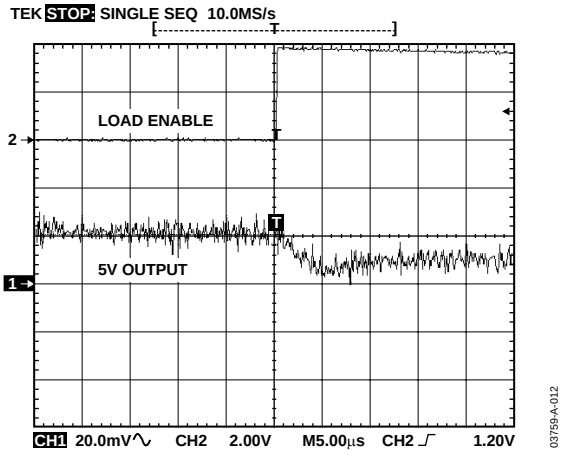


Figure 12. 5 V Output Transient Response for Max load Current

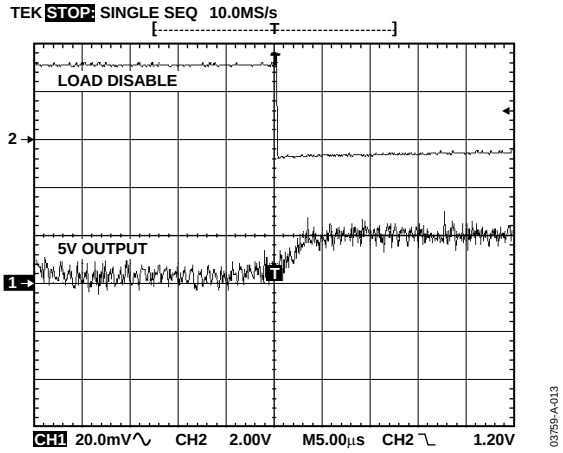


Figure 13. 5 V Output Transient Response, Load Disconnected

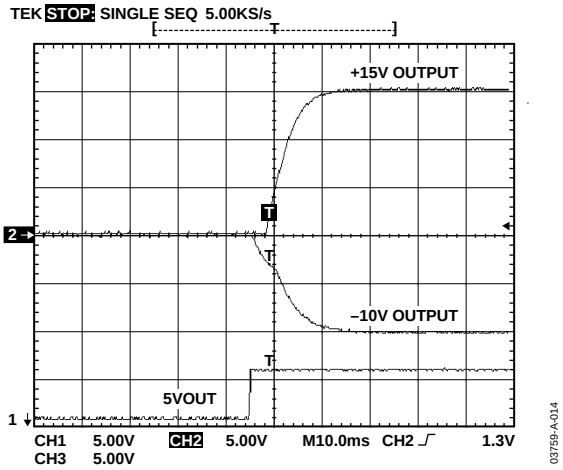


Figure 14. +15 V and −10 V Outputs at Power-Up

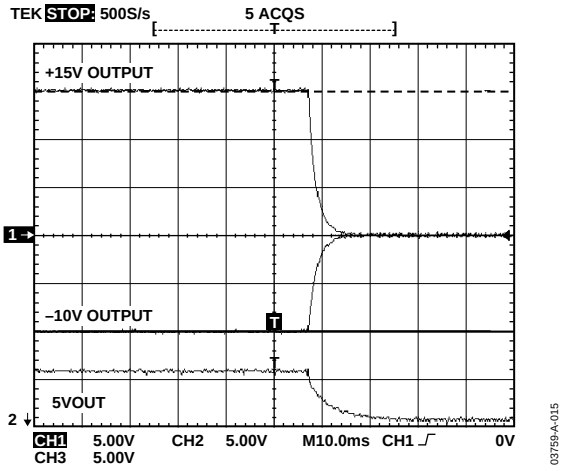


Figure 15. +15 V and −10 V Outputs at Power-Down (Unloaded)

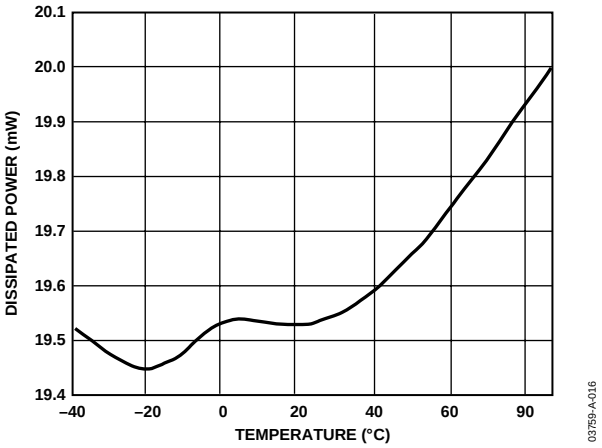


Figure 16. Power Dissipation over Temperature, V_{CC} = 3.6 V, Scanning Mode with All O/Ps at Maximum Load

THEORY OF OPERATION

SCANNING AND BLANKING

A TFT LCD panel is made up of a bank of capacitors, each representing a pixel in the display. These capacitors store different levels of charge, depending on the amount of luminescence required for a given pixel. When a picture is displayed on the panel, a scan of all the pixel capacitors is performed, placing different levels of charge on each in order to create the image. The process of updating the display like this is called scanning. Once scanned, an image is held by pixel capacitance, and the controller and source line drivers can be put into a low power mode. This low power mode is referred to as the blanking mode on the ADM8832. Over a finite period of time, this pixel charge will leak and the capacitors will need to be refreshed in order to maintain the image.

The ADM8832 uses scanning and blanking modes, as follows. When the TFT LCD panel is in scanning mode, a logic high on the SCAN/$\overline{\text{BLANK}}$ input places the device in high current power mode, providing extra power (extra current) to the LCD controller and the source line drivers. If the panel continues to be updated (as when a moving picture is being displayed), the ADM8832 can be continually operated in scanning mode. If the same image is kept on the panel, a logic low is applied to the SCAN/$\overline{\text{BLANK}}$ input, and the ADM8832 enters blanking (low current) mode. Depending on how often the image is updated, the ADM8832 can be operated with a variable SCAN/ $\overline{\text{BLANK}}$ duty cycle. This helps to maximize power efficiency and, therefore, extends the battery life.

POWER SEQUENCING

The gate drive supplies must be sequenced such that the −10 V supply is up before the +15 V supply for the TFT panel to power on correctly. The ADM8832 controls this sequence. When the device is turned on (a logic high on $\overline{\text{SHDN}}$), the ADM8832 allows the −10 V output to ramp immediately, but holds off the +15 V output. It continues to do this until the negative output reaches −3 V. At this point, the positive output is enabled and allowed to ramp up to +15 V. This sequence is shown in Figure 17.

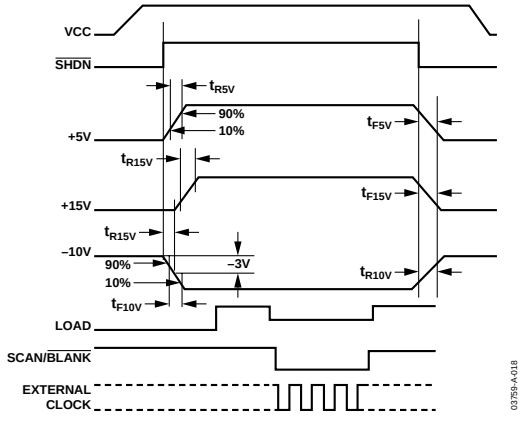


Figure 17. Power Sequence

TRANSIENT RESPONSE

The ADM8832 features extremely fast transient response, making it very suitable for fast image updates on TFT LCD panels. This means that even under changing load conditions there is still very effective regulation of the 5 V output. Figure 12 and Figure 13 show how the 5.1 V output responds when a maximum load is dynamically connected and disconnected. Note that the output settles within 5 µs to less than 1% of the output level.

EXTERNAL CLOCK

The ADM8832 has an internal 100 kHz oscillator, but an external clock source can also be used to clock the part. This clock source must be applied to the CLKIN pin. Power is saved during blanking periods by disabling the internal oscillator and by switching to the lower frequency external clock source. To achieve optimum performance of the charge pump circuitry, it is important that the duty cycle of the external clock source is 50% and that the rise and fall times are less than 20 ns.

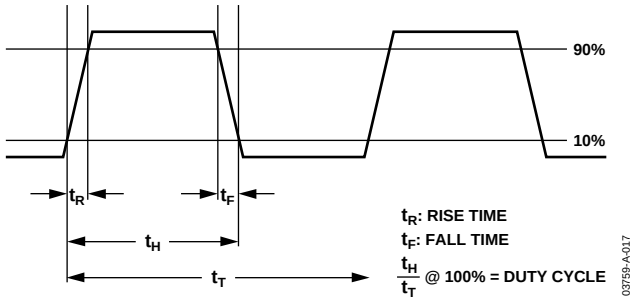


Figure 18. Duty Cycle of External Clock

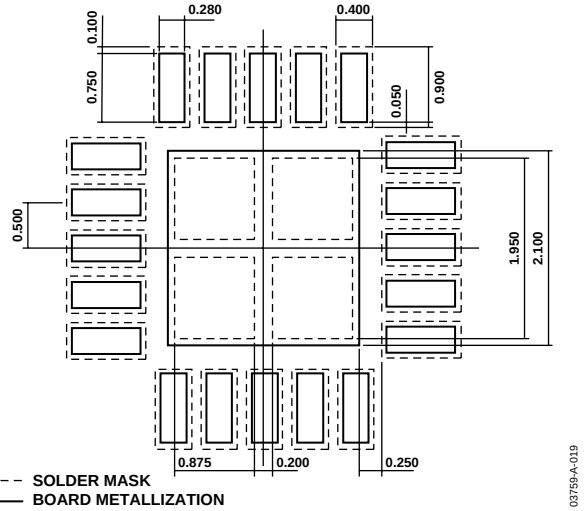
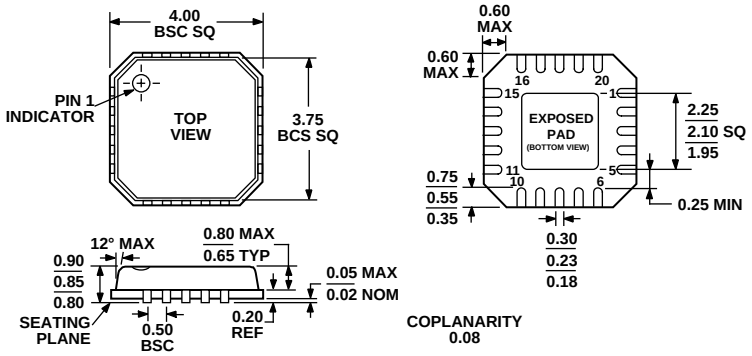


Figure 19. Suggested LFCSP 4 mm × 4mm 20 Lead Land Pattern

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 20. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body
(CP-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM8832ACP	−40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADM8832ACP-REEL	−40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADM8832ACP-REEL7	−40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADM8832ACPZ[1]	−40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADM8832ACPZ-REEL[1]	−40°C to +85°C	Lead Frame Chip Scale Package	CP-20
ADM8832ACPZ-REEL7[1]	−40°C to +85°C	Lead Frame Chip Scale Package	CP-20

[1] Z = Pb-free part.

NOTES

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ANALOG DEVICES

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