

Ultralow Noise, Low Sensitivity Tolerance, PDM Digital Microphone

Data Sheet

ADMP522

1530-001

CLK

Ödata

FUNCTIONAL BLOCK DIAGRAM ADMP522

ADC

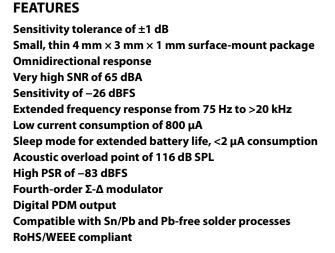
POWER MANAGEMENT

a dug

PDM MODULATOR

CHANNEL SELECT

SELECT



APPLICATIONS

Smartphones and feature phones Microphone arrays Tablet computers Teleconferencing systems Digital still and video cameras Bluetooth headsets Notebook PCs Security and surveillance

GENERAL DESCRIPTION

The ADMP522¹ is an omnidirectional, bottom-ported, digital output MEMS microphone with high performance, ultralow noise, and low power. The ADMP522 has a sensitivity tolerance of ±1 dB from part to part, making it ideal for microphone array and beamforming applications.

The ADMP522 consists of a MEMS microphone element and an impedance converter amplifier followed by a fourth-order Σ - Δ modulator. The digital interface enables the pulse density modulated (PDM) output of two microphones to be time multiplexed on a single data line using a single clock. The ADMP522 is function- and pin-compatible with the ADMP521 and ADMP421 microphones, providing an easy upgrade path.

The ADMP522 has a very high signal-to-noise ratio (SNR) of 65 dBA and sensitivity of -26 dBFS, making it an excellent choice for near- and far-field applications. The ADMP522 has an extended wideband frequency response, resulting in natural sound with high intelligibility. Low current consumption and a sleep mode with less than 2 µA current consumption enables long battery life for portable applications.

The ADMP522 is available in a thin 4 mm \times 3 mm \times 1 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation.

¹ Protected by U.S. Patents 7,449,356; 7,825,484; 7,885,423; and 7,961,897. Other patents are pending.

Rev. 0

Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A. Tel: 781.329.4700 ©2013 Analog Devices, Inc. All rights reserved. **Technical Support** www.analog.com

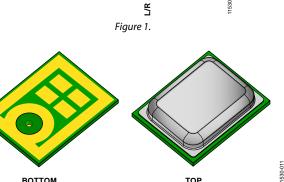


Figure 2. Isometric Views of the Microphone Package

IMPORTANT LINKS for the <u>ADMP522</u>*

Last content update 09/20/2013 10:15 pm

PARAMETRIC SELECTION TABLES Find Similar Products By Operating Parameters	DESIGN COLLABORATION COMMUNITY
DOCUMENTATION AN-1140: Microphone Array Beamforming AN-1124: Recommendations for Sealing Analog Devices, Inc., Bottom- Port MEMS Microphones from Dust and Liquid Ingress	Collaborate Online with the ADI support team and other designer about select ADI products. Follow us on Twitter: <u>www.twitter.com/ADI_News</u> Like us on Facebook: <u>www.facebook.com/AnalogDevicesInc</u>
AN-1112: Microphone Specifications Explained AN-1068: Reflow Soldering of the MEMS Microphone AN-1003: Recommendations for Mounting and Connecting Analog Devices, Inc., Bottom-Ported MEMS Microphones UG-326: PDM Digital Output MEMS Microphone Evaluation Board MS-2472: Analog and Digital MEMS Microphone Design Considerations EVALUATION KITS & SYMBOLS & FOOTPRINTS View the Evaluation Boards and Kits page for documentation and	DESIGN SUPPORT Submit your support request here: Linear and Data Converters Embedded Processing and DSP Telephone our Customer Interaction Centers toll free: Americas: 1-800-262-5643 Europe: 00800-266-822-82 China: 4006-100-006 India: 1800-419-0108 Russia: 8-800-555-45-90
View the Evaluation Boards and Kits page for documentation and purchasing Symbols and Footprints	<u>Quality and Reliability</u> <u>Lead(Pb)-Free Data</u>
	<section-header><section-header><section-header><section-header><section-header><section-header><section-header></section-header></section-header></section-header></section-header></section-header></section-header></section-header>



* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet. Note: Dynamic changes to the content on this page (labeled 'Important Links') does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.

TABLE OF CONTENTS

Features
Applications1
Functional Block Diagram1
General Description
Revision History
Specifications
Timing Characteristics4
Absolute Maximum Ratings
ESD Caution
Soldering Profile
Pin Configuration and Function Descriptions
Typical Performance Characteristics7
Theory of Operation
PDM Data Format
PDM Microphone Sensitivity

Connecting PDM Microphones	9
Sleep Mode	9
Start-Up Time	9
Applications Information	10
Interfacing with Analog Devices Codecs	10
Supporting Documents	10
PCB Design and Land Pattern Layout	11
Alternative PCB Land Patterns	12
PCB Material and Thickness	12
Handling Instructions	13
Pick-and-Place Equipment	13
Reflow Solder	
Board Wash	13
Outline Dimensions	14
Ordering Guide	14

REVISION HISTORY

7/13—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{DD} = 1.8 V, CLK = 2.4 MHz, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.					
Parameter	Test Conditions/Comments	Min	Тур	Max	Unit
PERFORMANCE					
Directionality			Omni		
Sensitivity ¹	1 kHz, 94 dB sound pressure level (SPL)	-27	-26	-25	dBFS
Signal-to-Noise Ratio (SNR)	20 Hz to 20 kHz, A-weighted		65		dBA
Equivalent Input Noise (EIN)	20 Hz to 20 kHz, A-weighted		29		dBA SPL
Dynamic Range	Derived from EIN and maximum acoustic input		91		dB
Frequency Response ²	Low frequency –3 dB point		75		Hz
	High frequency –3 dB point		>20		kHz
Total Harmonic Distortion (THD)	105 dB SPL		0.5	1.5	%
Power Supply Rejection (PSR)	217 Hz, 100 mV p-p sine wave superimposed on V_{DD} = 1.8 V		-83		dBFS
Acoustic Overload Point	10% THD		116		dB SPL
Full-Scale Acoustic Level	0 dBFS, derived from sensitivity		120		dB SPL
POWER SUPPLY					
Supply Voltage (VDD)		1.62		3.63	V
Supply Current (Is)					
Normal Mode	$V_{DD} = 1.8 V$		0.8	1.2	mA
	$V_{DD} = 3.3 V$		1.0	1.4	mA
Sleep Mode ³	$V_{DD} = 1.8 V$			2	μΑ
	$V_{DD} = 3.3 V$			3	μΑ
DIGITAL INPUT/OUTPUT CHARACTERISTICS					
Input Voltage High (V _{IH})		$0.65 \times V_{\text{DD}}$			V
Input Voltage Low (V⊫)				$0.35 \times V_{\text{DD}}$	V
Output Voltage High (V _{он})	$I_{LOAD} = 0.5 \text{ mA}$	$0.7 \times V_{\text{DD}}$	V_{DD}		V
Output Voltage Low (Vol)	$I_{LOAD} = 0.5 \text{ mA}$		0	$0.3 \times V_{\text{DD}}$	V
Output DC Offset	Percent of full scale		5		%
Latency			<30		μs
Noise Floor	20 Hz to 20 kHz, A-weighted		-91		dBFS

¹ Relative to the rms level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.

² See Figure 6 and Figure 7. ³ The microphone enters sleep mode when the clock frequency is less than 1 kHz.

TIMING CHARACTERISTICS

Table 2.

Parameter	Description	Min	Тур	Max	Unit
SLEEP MODE					
Sleep Time	Time from CLK falling ($f_{CLK} < 1 \text{ kHz}$)		30		μs
Wake-Up Time	Time from CLK rising (f _{CLK} > 1 kHz), power on		10		ms
INPUT					
t _{clkin}	Input clock period	270		1111	ns
Clock Frequency (CLK) ¹		0.9	2.4	3.6	MHz
Clock Duty Cycle		40		60	%
OUTPUT					
t10UTEN	DATA1 (right) driven after falling clock edge	54			ns
t10UTDIS	DATA1 (right) disabled after rising clock edge	15		54	ns
t _{20UTEN}	DATA2 (left) driven after rising clock edge 54		ns		
t _{20UTDIS}	DATA2 (left) disabled after falling clock edge	15		54	ns

¹ The microphone operates at any clock frequency between 0.9 MHz and 3.6 MHz. Some specifications may not be guaranteed at frequencies other than 2.4 MHz.

Timing Diagram

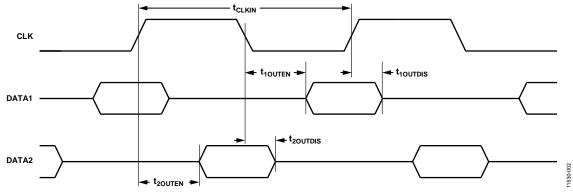


Figure 3. Pulse Density Modulated Output Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

1.0010-01	
Parameter	Rating
Supply Voltage	–0.3 V to +3.6 V
Digital Pin Input Voltage	-0.3 V to V _{DD} + 0.3 V or +3.6 V, whichever is less
Sound Pressure Level (SPL)	160 dB
Mechanical Shock	10,000 <i>g</i>
Vibration	Per MIL-STD-883, Method 2007, Test Condition B
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	–55°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SOLDERING PROFILE

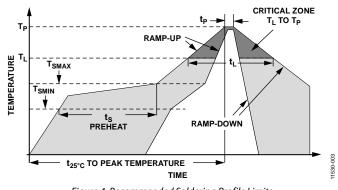


Figure 4. Recommended Soldering Profile Limits

Table 4. Recommended Soldering Profile Limits

Profile Feature	Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)	1.25°C/sec maximum	1.25°C/sec maximum
Preheat		
Minimum Temperature (T _{SMIN})	100°C	100°C
Maximum Temperature (T _{SMAX})	150°C	200°C
Time, T _{SMIN} to T _{SMAX} (ts)	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T _{SMAX} to T _L)	1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t _L)	45 sec to 75 sec	~50 sec
Liquidous Temperature (T _L)	183°C	217°C
Peak Temperature (T _P)	215°C +3°C/–3°C	260°C +0°C/-5°C
Time Within 5°C of Actual Peak Temperature (t _P)	20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate	3°C/sec maximum	3°C/sec maximum
Time 25°C ($t_{25°C}$) to Peak Temperature	5 minutes maximum	5 minutes maximum

ADMP522

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

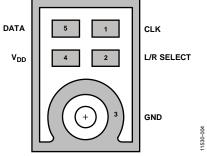
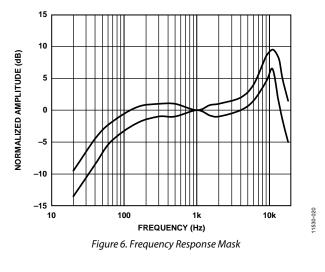


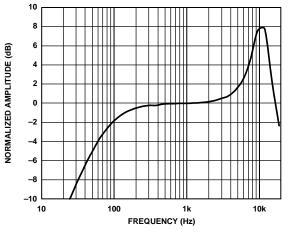
Figure 5. Pin Configuration (Bottom View)

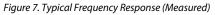
Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Clock Input to Microphone.
2	L/R SELECT	Left Channel or Right Channel Select.
		DATA1 (right): L/R SELECT tied to GND.
		DATA2 (left): L/R SELECT tied to V_{DD} .
3	GND	Ground.
4	V _{DD}	Power Supply. For best performance and to avoid potential parasitic artifacts, place a 0.1 µF (100 nF) ceramic type X7R capacitor between Pin 4 (V _{DD}) and ground. Place the capacitor as close to Pin 4 as possible.
5	DATA	Digital Output Signal (DATA1 or DATA2).

TYPICAL PERFORMANCE CHARACTERISTICS







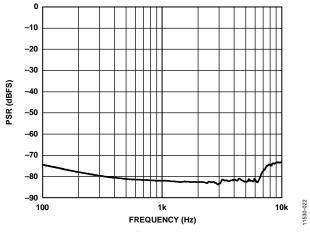


Figure 8. Power Supply Rejection (PSR) vs. Frequency

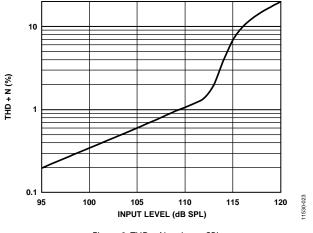


Figure 9. THD + N vs. Input SPL

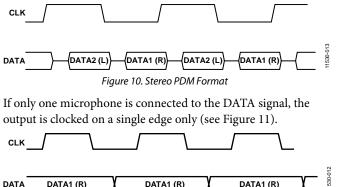
11530-021

THEORY OF OPERATION PDM DATA FORMAT

The output from the DATA pin of the ADMP522 is in PDM format. This data is the 1-bit output of a fourth-order Σ - Δ modulator. The data is encoded so that the left channel is clocked on the falling edge of CLK and the right channel is clocked on the rising edge of CLK.

After driving the DATA signal high or low in the appropriate half frame of the CLK signal, the DATA driver of the microphone is tristated. In this way, two microphones—one set to the left channel and the other to the right channel—can drive a single DATA line.

Figure 3 shows a timing diagram of the PDM data format; the DATA1 and DATA2 lines shown in Figure 3 are two halves of the single physical DATA signal. Figure 10 shows a diagram of the two stereo channels sharing a common DATA line.



DATA	DATA1 (R)	DATA1 (R)	DATA1 (R)	
	Fig	ure 11. Mono PDM For	rmat	

For example, a left channel microphone is never clocked on the rising edge of CLK. In a single microphone application, each bit of the DATA signal is typically held for the full CLK period until the next transition of the CLK signal because the leakage of the DATA line is not sufficient to discharge the line while the driver is tristated.

The channel assignments are determined by the logic level on the L/R SELECT pin (see Table 6).

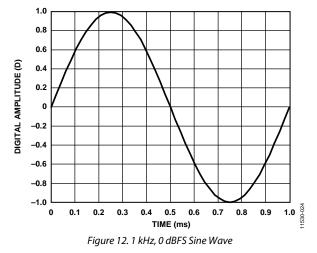
Table 6. ADMP522 Channel Setting

L/R SELECT Pin Setting	Channel
Low (tie to GND)	Right (DATA1)
High (tie to V _{DD})	Left (DATA2)

For PDM data, the density of the pulses indicates the signal amplitude. A high density of high pulses indicates a signal near positive full scale, and a high density of low pulses indicates a signal near negative full scale. A perfect zero (dc) audio signal is indicated by an alternating pattern of high and low pulses. The output PDM data signal has a small dc offset of approximately 5% of full scale. A high-pass filter in the codec that is connected to the digital microphone typically removes this dc signal and does not affect the performance of the microphone.

PDM MICROPHONE SENSITIVITY

The sensitivity of a PDM output microphone is specified in units of dBFS (decibels relative to a full-scale digital output). A 0 dBFS sine wave is defined as a signal whose peak just touches the fullscale code of the digital word (see Figure 12). This measurement convention means that signals with a different crest factor may have an rms level higher than 0 dBFS. For example, a full-scale square wave has an rms level of 3 dBFS.



The definition of a 0 dBFS signal must be understood when measuring the sensitivity of the ADMP522. An acoustic input signal of a 1 kHz sine wave at 94 dB SPL applied to the ADMP522 results in an output signal with a -26 dBFS level. This means that the output digital word peaks at -26 dB below the digital full-scale level. A common misunderstanding is that the output has an rms level of -29 dBFS; however, this is not the case because of the definition of a 0 dBFS sine wave.

There is no commonly accepted unit of measurement to express the instantaneous level of a digital signal output from the microphone, as opposed to the rms level of the signal. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale (see Figure 12). In this case, a –26 dBFS sine wave has peaks at 0.05 D.

For more information about digital microphone sensitivity, see the AN-1112 Application Note, *Microphone Specifications Explained*.

CONNECTING PDM MICROPHONES

A PDM output microphone is typically connected to a codec with a dedicated PDM input. This codec separately decodes the left and right channels and filters the high sample rate modulated data back to the audio frequency band. The codec also generates the clock for the PDM microphones or is synchronous with the source that generates the clock. For more information about connecting the ADMP522 to Analog Devices, Inc., audio codecs with a PDM input, see the Applications Information section.

Figure 13 and Figure 14 show mono and stereo connections between the ADMP522 and a codec. The mono connection shows an ADMP522 set to output data on the right channel. To output data on the left channel, tie the L/R SELECT pin to $V_{\rm DD}$ instead of GND.

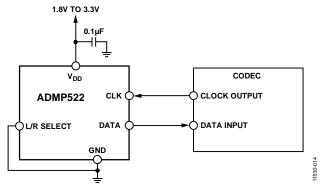
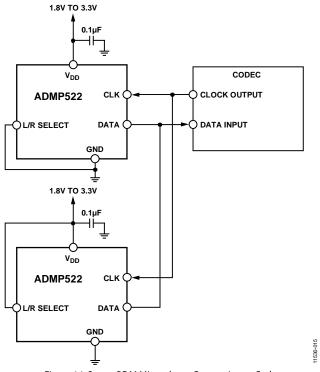


Figure 13. Mono PDM Microphone (Right Channel) Connection to Codec





Decouple the $V_{\rm DD}$ pin of the ADMP522 to GND with a 0.1 μF capacitor. Place this capacitor as close to $V_{\rm DD}$ as the printed circuit board (PCB) layout allows.

Do not use a pull-up or pull-down resistor on the PDM data signal line because the resistor can pull the signal to an incorrect state during the period that the signal line is tristated.

The DATA signal does not need to be buffered in normal use when the ADMP522 microphones are placed close to the codec on the PCB. If the ADMP522 must drive the DATA signal over a long cable (>15 cm) or other large capacitive load, a digital buffer may be needed. Use a signal buffer on the DATA line only when one microphone is in use or after the point where two microphones are connected (see Figure 15).

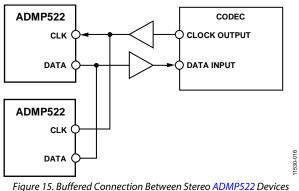


Figure 15. Buffered Connection Between Stereo ADMP522 Devices and a Codec

The DATA output of each microphone in a stereo configuration cannot be individually buffered because the two buffer outputs cannot drive a single signal line. If a buffer is used, take care to select a buffer with low propagation delay so that the timing of the data connected to the codec is not corrupted.

When long wires are used to connect the codec to the ADMP522, a 100 Ω source termination resistor can be used on the clock output of the codec instead of a buffer to minimize signal overshoot or ringing. Depending on the drive capability of the codec clock output, a buffer may still be needed, as shown in Figure 15.

SLEEP MODE

The microphone enters sleep mode when the clock frequency falls below 1 kHz. In sleep mode, the microphone data output is in a high impedance state. The current consumption of the ADMP522 in sleep mode is less than 2 μ A at V_{DD} = 1.8 V.

The ADMP522 enters sleep mode within 1 ms of the clock frequency falling below 1 kHz. The microphone wakes up from sleep mode 32,768 cycles after the clock becomes active. For a 2.4 MHz clock, the microphone begins to output data in 13.7 ms. The wake-up time, as specified in Table 2, indicates the time from when the clock is enabled to when the ADMP522 is consuming its specified current.

START-UP TIME

The start-up time of the ADMP522 from when the clock is active is the same as the wake-up time from sleep mode. The microphone starts up 32,768 cycles after the clock is active.

APPLICATIONS INFORMATION INTERFACING WITH ANALOG DEVICES CODECS

The PDM output of the ADMP522 interfaces directly with the digital microphone inputs on the Analog Devices ADAU1361, ADAU1761, ADAU1772, and ADAU1781 codecs (see Figure 16).

For more information about the digital microphone interface, see the AN-1003 Application Note and the data sheet for the ADAU1361, ADAU1761, ADAU1772, or ADAU1781 codec.

The CN-0078 Circuit Note describes the connection between these codecs and a digital microphone. All configuration information for the ADMP522 is the same as for the ADMP421.

SUPPORTING DOCUMENTS

For additional information, see the following documents.

Evaluation Board User Guide

UG-326, PDM Digital Output MEMS Microphone Evaluation Board

Circuit Note

CN-0078, *High Performance Digital MEMS Microphone Simple Interface to a SigmaDSP Audio Codec*

Application Notes

AN-1003, Recommendations for Mounting and Connecting the Analog Devices, Inc., Bottom-Ported MEMS Microphones

AN-1068, Reflow Soldering of the MEMS Microphone

AN-1112, Microphone Specifications Explained

AN-1124, Recommendations for Sealing Analog Devices, Inc., Bottom-Port MEMS Microphones from Dust and Liquid Ingress

AN-1140, Microphone Array Beamforming

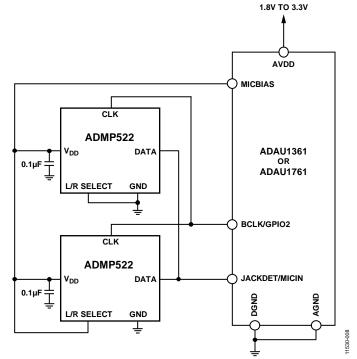


Figure 16. ADAU1361 or ADAU1761 Stereo Interface Block Diagram

PCB DESIGN AND LAND PATTERN LAYOUT

Lay out the PCB land pattern for the ADMP522 at a 1:1 ratio to the solder pads on the microphone package (see Figure 17). Take care to avoid applying solder paste to the sound hole in the PCB. Figure 18 shows a suggested solder paste stencil pattern layout.

The response of the ADMP522 is not affected by the PCB hole size as long as the hole is not smaller than the sound port of the microphone (0.25 mm, or 0.010 inch, in diameter). A 0.5 mm to 1 mm (0.020 inch to 0.040 inch) diameter for the hole is recommended. Align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the performance of the microphone as long as the holes are not partially or completely blocked.

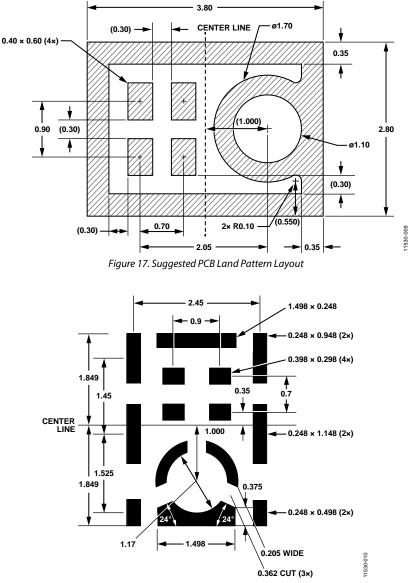


Figure 18. Suggested Solder Paste Stencil Pattern Layout

ALTERNATIVE PCB LAND PATTERNS

The standard PCB land pattern of the ADMP522 has a solid ring around the edge of the footprint (see Figure 17). In some board designs, this ring can make routing the microphone signals more difficult. The ring is used to improve the RF immunity performance of the ADMP522; however, it is not necessary to have the full ring connected for electrical functionality. If a design can tolerate reduced RF immunity, this ring can either be broken or removed completely from the PCB footprint.

Figure 19 shows an example PCB land pattern with no enclosing ring around the edge of the part.

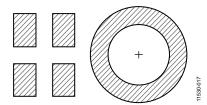


Figure 19. Example PCB Land Pattern with No Enclosing Ring

Figure 20 shows an example PCB land pattern with the ring broken on two sides so that the inner pads can be more easily routed on the PCB.

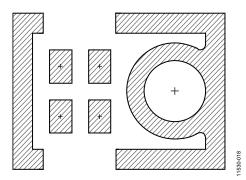


Figure 20. Example PCB Land Pattern with Broken Enclosing Ring

Note that in both of these patterns, the solid ring around the sound port is still present; this ring is needed to ground the microphone and for acoustic performance. The pad on the package connected to this ring is ground and still needs a solid electrical connection to the PCB ground.

If a land pattern similar to Figure 19 or Figure 20 is used on a PCB, make sure that the unconnected ring on the bottom of the ADMP522 is not placed directly over any exposed copper. The ring on the microphone is still at ground, and any PCB traces routed beneath it must be properly masked to avoid short circuits.

PCB MATERIAL AND THICKNESS

The performance of the ADMP522 is not affected by PCB thickness. The ADMP522 can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality.

HANDLING INSTRUCTIONS PICK-AND-PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-andplace and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 4 and Table 4.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

04-19-2012-G

OUTLINE DIMENSIONS

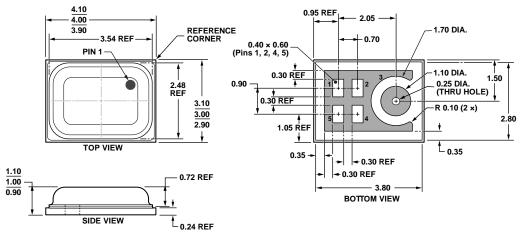


Figure 21. 5-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV] 4 mm × 3 mm Body (CE-5-1) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option ²	Ordering Quantity
ADMP522ACEZ-RL	-40°C to +85°C	5-Terminal LGA_CAV, 13" Tape and Reel	CE-5-1	5,000
ADMP522ACEZ-RL7	-40°C to +85°C	5-Terminal LGA_CAV, 7" Tape and Reel	CE-5-1	1,000
EVAL-ADMP522Z-FLEX		Flexible Evaluation Board		

 1 Z = RoHS Compliant Part.

² This package option is halide free.

NOTES

ADMP522

Data Sheet

NOTES

©2013 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. D11530-0-7/13(0)



www.analog.com

Rev. 0 | Page 16 of 16