CDMA Power Management System

Preliminary Technical Data ADP3500

FEATURES

Handles all CDMA Baseband and RF/IF Power Management Functions
LDOs Optimized for Specific CDMA Subsystems
Four Backup LDOs for Stand-By mode operation
Four Li-Ion Battery Charge Modes
5mA Pre Charge
Low Current Charge
Full Current Charge
Regulator mode (no current limit)
Ambient Temperature: -30 ºC to +85 ºC
64pin 7x7 LQFP package

APPLICATIONS

CDMA/CDMA2000/PCS Handsets

GENERAL DESCRIPTION

The ADP3500 is a multifunction power system chip optimized for CDMA cell phone power management. It contains 15 LDOs. Sophisticated controls are available for power up during battery charging, keypad interface, GPIO/INT function and RTC function. The battery charger has four modes as Pre-charge, Low Current Charge, Full Current Charge, and Regulator modes, and is designed for Li-Ion/Li-Polymer batteries.

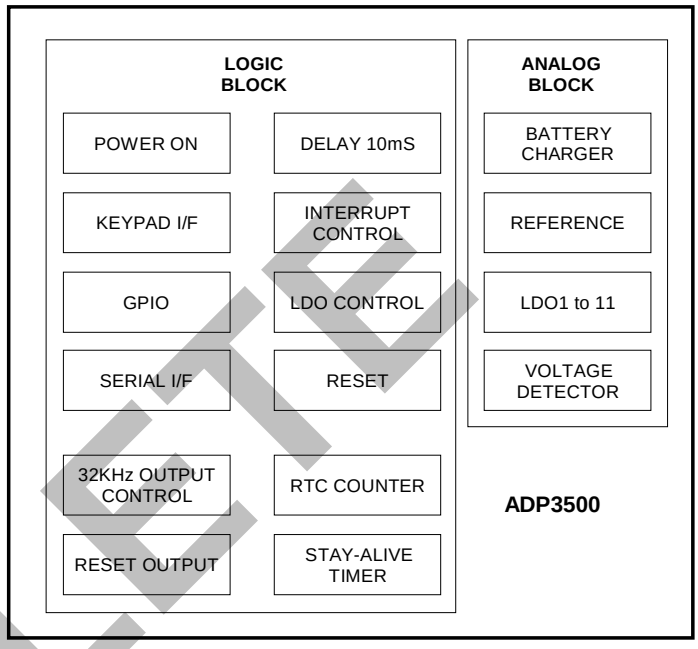

Figure 1. Functional Block Diagram

REV. PrP 2/6/02

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ADP3500 - SPECIFICATIONS

MAIN FUNCTIONS

T_A =-30 to +85°C, C_{VBAT}=1µF MLCC, VBAT=3.6V unless otherwise noted. See Table 2 for C_{OUT}.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SHUTDOWN GND CURRENT Power OFF	IGND	LDO3b : ON, connect to RTCV through Schottky diode. RTC/32K OSC : Active All other LDOs: OFF All logic inputs : VBAT or GND MVBAT: OFF		25	40	µA
OPERATING GND CURRENT Stand-by mode operation (light load)	IGND	LDO1b, 2b, 3b, 6b: ON Io=1mA for LDO1b & 3b Io=300µA for LDO2b & 6b All other LDOs: OFF RTC/32K OSC: Active MVBAT: OFF All logic output: no load		60	125	µA
Stand-by mode operation (Mid-load)		LDO1, 2, 3, 6, all Sub-LDO: ON, Io=70% load All other LDOs: OFF RTC/32K OSC: Active MVBAT: ON All logic outputs: no load		275		µA
Active operation		LDO5: OFF All other LDOs: ON, 70% load RTC/32K OSC: Active All logic outputs: no load MVBAT: ON		650		µA
Thermal Shutdown Threshold				160		°C
Thermal Shutdown Hysteresis				35		°C
Operational Temperature range	Tope		-30		+85	°C
Adapter Voltage range (recommendation)	VADP		5.5		12	V
VBAT Voltage range	VBAT		3.3		5.5	V

LDO SPECIFICATIONS

T_A =25°C, C_{VBAT}=1µF MLCC, VBAT = Vout+1V, NRCAP=0.1µF. See Table 2 for C_{OUT}.

Baseband VDD Main-LDO (LDO #1a)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE	$V_{LDO\#1}$	Io = 1 to 150 mA Ta= -30 to +85°C	2.81	2.90	2.99	V
OUTPUT CAPACITOR REQUIRED FOR STABILITY	$C_{LDO\#1}$		2.2			µF
DROPOUT VOLTAGE	V_{DO}	Io = 150 mA		200		mV
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#1}$	Io = 150 mA		50		µA

Baseband VDD Sub-LDO (LDO #1b)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE	$V_{LDO\#1b}$	Io = 1mA Ta= -30 to +85°C	2.8	2.87	3.0	V
GND Current	$I_{LDO\#1b}$			10		µA

Baseband AVDD Main-LDO (LDO #2a)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT Voltage	$V_{LDO\#2}$	16 steps, 20mV/step, Ta= 25C, Io=50mA				
		Code : 1000	2.30	2.36	2.43	V
		Code : 0111	2.60	2.66	2.74	V
OUTPUT default voltage	$V_{LDO\#2}$	Io = 50 mA, Ta= 25°C	2.46	2.52	2.6	V
OUTPUT Voltage	$V_{LDO\#2}$	16 steps, 20mV/step, Io=50mA, Ta= -30 to +85°C				
		Code : 1000	2.29	2.36	2.47	V
		Code : 0111	2.57	2.66	2.81	V
OUTPUT default voltage	$V_{LDO\#2}$	Io = 50 mA, Ta= -30 to +85°C	2.42	2.52	2.66	V
OUTPUT CAPACITOR REQUIRED FOR STABILITY	$C_{LDO\#2}$		1			µF
DROPOUT VOLTAGE	V_{DO}	Io = 50 mA		210		mV
RIPPLE REJECTION		f = 1KHz		50		dB
OUTPUT NOISE VOLTAGE	V_{NOISE}	f = 100 Hz to 100 kHz		120		μV_{RMS}
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#2}$	Io = 50 mA		50		µA

Baseband AVDD Sub-LDO (LDO #2b)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT Voltage	$V_{LDO\#2b}$	Io = 300 µA, $V_{LDO\#2a}$=2.6V Ta= -30 to +85°C	2.50		2.70	V
GND Current	$I_{LDO\#2b}$			5		µA

REFO switch

Parameter	Symbol	Conditions	Min	Typ	Max	Units
On resistance	R_{ON}	Ta= -30~+85°C, Io=500µA		50	130	Ω
Off leak	I_{LEAK}	LDO2: ON, Switch: OFF		0.01	1	µA

Coin Cell Main-LDO (LDO #3a)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE	$V_{LDO\#3}$	Io = 1 to 50 mA Ta= -30 to +85°C	2.85	3.0	3.09	V
Dropout Voltage	V_{DO}	Io= 50 mA		140		mV
OUTPUT CAPACITOR REQUIRED FOR STABILITY	$C_{LDO\#3}$		1			µF
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#3}$	Io = 50 mA		50		µA

Coin Cell Sub-LDO (LDO #3b)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE	$V_{LDO\#3b}$	Io=1mA Ta= -30 to +85°C	2.85	2.97	3.15	V
GND Current	$I_{LDO\#3b}$			10		µA

Audio LDO (LDO #4)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE	$V_{LDO\#4}$	Io = 1 to 180 mA Ta = -30 to +85°C	2.81	2.90	2.99	V
OUTPUT CAPACITOR REQUIRED FOR STABILITY	$C_{LDO\#4}$		2.2			µF
Dropout Voltage	V_{DO}	Io = 180 mA		200		mV
RIPPLE REJECTION		f = 1KHz		50		dB
OUTPUT NOISE VOLTAGE	V_{NOISE}	f = 100 Hz to 10 kHz		50		μV_{RMS}
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#4}$	Io = 180 mA		50		µA

Vibrator LDO (LDO #5)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	$V_{LDO\#5}$	Io = 1 to 150 mA Ta= -30 to +85°C	2.75	2.9	3.05	V
Dropout Voltage	V_{DO}	Io = 150mA		200		mV
Output capacitor required for stability	$C_{LDO\#5}$		2.2			µF
GND Current	$I_{LDO\#5}$	Io = 150 mA		50		µA

Baseband Core Main-LDO (LDO #6a)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	$V_{LDO\#6}$	Io = 1 to 50 mA Ta= -30 to +85°C	2.52	2.60	2.68	V
Output capacitor required for stability	$C_{LDO\#6}$		1			µF
Dropout Voltage	V_{DO}	Io = 50 mA		160		mV
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#6}$	Io = 50 mA		50		µA

Baseband Core Sub-LDO (LDO #6b)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT VOLTAGE	$V_{LDO\#6b}$	Io = 300 µA Ta= -30 to +85°C	2.5	2.57	2.7	V
GND Current	$I_{LDO\#6b}$			5		µA

RF Rx1 LDO (LDO #7)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output voltage	$V_{LDO\#7}$	Io = 1 to 100 mA Ta= -30 to +85°C	2.81	2.9	2.99	V
Output capacitor required for stability	$C_{LDO\#7}$		1.5			µF
Dropout voltage	V_{DO}	Io = 100 mA		200		mV
Ripple rejection		f = 1KHz		50		dB
Output noise voltage	V_{NOISE}	f = 100 Hz to 100KHz		40		μV_{RMS}
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#7}$	Io=100mA		50		µA

RF Tx LDO (LDO #8)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output voltage	$V_{LDO\#8}$	Io = 1 to 150 mA Ta= -30 to +85°C	2.81	2.9	2.99	V
Output capacitor required for stability	$C_{LDO\#8}$		2.2			µF
Dropout voltage	V_{DO}	Io = 150mA		200		mV
Ripple Rejection		f = 1KHz		50		dB
Output noise voltage	V_{NOISE}	f = 100 Hz to 100KHz		40		μV_{RMS}
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#8}$	Io=150mA		50		µA

RF Rx 2 LDO (LDO #9)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output voltage	$V_{LDO\#9}$	Io = 1 to 50 mA Ta= -30 to +85°C	2.81	2.9	2.99	V
Output capacitor required for stability	$C_{LDO\#9}$		1			µF
Dropout voltage	V_{DO}	Io = 50mA		150		mV
Ripple Rejection		f = 1KHz		50		dB
Output noise voltage	V_{NOISE}	f = 100 Hz to 100KHz		40		μV_{RMS}
Start-up time from shutdown				250		µS
GND Current	$I_{LDO\#9}$	Io=50mA		50		µA

RF Optional LDO (LDO #10)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output voltage	$V_{LDO\#10}$	Io= 1 to 50 mA Ta= -30 to +85°C	2.81	2.9	2.99	V

Output capacitor required for stability	$C_{LDO\#10}$		1			µF
Dropout voltage	V_{DO}	Io = 50mA		150		mV
Ripple rejection		f = 1KHz		50		dB
Output noise voltage	V_{NOISE}	f = 100 Hz to 100KHz		40		μV_{RMS}
Start-up Time from Shutdown				250		µS
GND Current	$I_{LDO\#10}$	Io=50mA		50		µA

Optional LDO (LDO #11)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output voltage	$V_{LDO\#11}$	Io = 1 to 100 mA Ta= -30 to +85°C	1.42	1.5	1.58	V
Output capacitor required for stability	$C_{LDO\#11}$		2.2			µF
Ripple rejection		f = 1KHz		50		dB
Output noise voltage	V_{NOISE}	f = 100 Hz to 100KHz		50		μV_{RMS}
Start-up Time from Shutdown				250		µS
GND Current	$I_{LDO\#11}$	Io=150mA		50		µA

Voltage Detector for LDO1 and LDO6

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LDO1 detect voltage	V_{DET1}	Ta= -30 to +85°C	2.7	2.72		V
LDO1 release voltage	V_{DET1}	Ta= -30 to +85°C		2.77	$V_{LDO1-NOM}$	V
LDO1 Hysteresis	V_{HYS1}	Ta= -30 to +85°C	35	52	85	mV
LDO6 detect voltage	V_{DET6}	Ta= -30 to +85°C	2.3	2.33		V
LDO6 release voltage	V_{DET6}	Ta= -30 to +85°C		2.40	$V_{LDO6-NOM}$	V
LDO6 Hysteresis	V_{HYS6}	Ta= -30 to +85°C	40	60	100	mV

BATTERY VOLTAGE DIVIDER: MVBAT

T_A =-30 to 85°C, C_{VBAT}=10µF MLCC, $C_{Adapter}$=1µF MLCC unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MVBAT Output voltage 5 – bit programmable	V_{MVBAT}	VBAT=4.35V, MVEN = 1 code 10000 code 01111	 2.484 2.673	 2.508 2.697	 2.533 2.727	 V/V V/V
MVBAT Output voltage step	Vstep	VBAT=4.35V, MVEN = 1		6		mV/lsb
Output drive current capability	Iout		1	2		mA
MVBAT Load Regulation	ΔMVBAT	0 < Iout < 100 µA		3	5	mV
MVBAT Output Voltage Step		VBAT = 4.35 V, MVEN = 1		6		mV
Operating Battery Current		VBAT = 4.35 V, MVEN = 1		65	85	µA
Shutdown Current		VBAT = 4.35 V, MVEN = 0			1	µA

BATTERY CHARGER

T_A =-30 to 85°C, C_{VBAT} =10µF MLCC, $C_{Adapter}$ =1µF MLCC, 4.0V ≤ ADAPTER ≤ 12V unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Charger Control Voltage Range 2 – bit programmable	VBAT SENSE	Ta= 25 °C, V_{R_SENSE} = 6mV & 115mV, 5.5V ≤ ADAPTER ≤ 12V (note 1) code 00 (default) code 01 code 10 code 11	 3.926 4.150 4.170 4.190	 3.980 4.190 4.210 4.230	 4.034 4.230 4.250 4.270	 V V V V
Charger Control Voltage Range 2 – bit programmable	VBAT SENSE	Ta= -20 to 55°C, V_{R_SENSE} = 6mV & 115mV, 5.5V ≤ ADAPTER ≤ 12V (note 1) code 00 (default) code 01 code 10 code 11	 3.905 4.130 4.146 4.166	 3.980 4.190 4.210 4.230	 4.065 4.250 4.278 4.300	 V V V V

Charger Detect On Threshold	ADAPTER-VBAT		110	165	225	mV
Charger Detect Off Threshold	ADAPTER-VBAT		5	23	50	mV
Charger Supply Current	$I_{ADAPTER}$	ADAPTER=5V, VBAT=4.3V			2	mA
Current Limit Threshold	ADAPTER-V_{ISNS}	ADAPTER=5V				
High Current Limit (Full charge current enabled)		VBAT=3.6V	135	160	185	mV
Low Current Limit (Full charge current disabled)		VBAT=3.0 V	40	55	70	mV
Pre-Charge Current Source		VBAT ≤ DDLO	3	5	7	mA
Base Pin Drive Current		Note 2.	15	28		mA
Deep Discharge Lock-Out (Releasing voltage)	DDLO	VBAT<DDLO, Ta=25C, 5mA Pre-charge, VBAT ramping up		2.675	2.78	V
Deep Discharge Lock-Out Hysteresis				200		mV
ISENSE Bias Current	I_{ISNS}	V_{ISNS}=5V			1	µA
BATID pull-up resistor to ADAPTER	R_{BATID}		70	100	130	KΩ
Minimum Load for Stability	I_L	BATID=H. Note 3.			10	mA

Note 1: Overhead includes external components, including sense resistor, PNP and isolation diode.
2: DDLO hysteresis is dependent upon DDLO threshold value. If DDLO threshold is at maximum, DDLO hysteresis is at maximum at the same time.
3: Guaranteed but not tested.

LOGICS

DC Specifications

T_A =25°C, C_{VBAT}=1µF MLCC, VBAT = 3.6 V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CS, CLKIN, RESETIN-, TCXO_ON, SLEEP-, KEYPADROW (Internal 10KΩ pull-up)						
Input High Voltage	VIH		2.25			V
Input Low Voltage	VIL				0.5	V
Hysteresis				470		mV
GPIO, DATA						V
Input High Voltage	VIH		2.25			V
Input Low Voltage	VIL				0.5	V
Hysteresis				470		mV
Output High Voltage	VOH	IOH=400µA	2.69			V
Output Low Voltage	VOL	IOL=-1.8mA			0.28	V
INT-						
Output High Voltage	VOH	IOH=400µA	2.69			V
Output Low Voltage	VOL	IOL=-1.8mA			0.28	V
BLIGHT (Open Drain Output)						
Output Low Voltage	VOL	IOL=-100mA			0.4	V
KEYPADCOL (Open Drain Output)						
Output Low Voltage	VOL	IOL=-1.8mA			0.15	V
PWRONKEY-, OPT1 (Internal 140KΩ Pull-up)						
Input High Voltage	VIH		0.8xVBAT			V
Input Low Voltage	VIL				0.2xVBAT	V
Hysteresis	Vhys			950		mV
OPT2- (Input/Open Drain Output)						
Input High Voltage	VIH		0.8xVBAT			V
Input Low Voltage	VIL				0.2xVBAT	V
Hysteresis	Vhys			950		mV
Output Low Voltage	VOL	IOL=-1.8mA			0.1xVBAT	V
OPT3						
Input High Voltage	VIH		0.7xVBAT			V
Input Low Voltage	VIL				0.2xVBAT	V
Hysteresis	Vhys			300		mV
32KOUT						
Output High Voltage	VOH	IOH=400µA	0.9xRTCV			V
Output Low Voltage	VOL	IOL=-1.8mA			0.1xRTCV	V
RESET+ (Open Drain Output)						
Output Low Voltage	VOL	IOL=-1.8mA			0.1xRTCV	V
OFF Leak	OFF_{LEAK}			0.005	1	µA
RSTDELAY-, RESETOUT- (Open Drain Output)						
Output Low Voltage	VOL	IOL=-1.8mA			0.1xRTCV	V
BATID (Internal 100KΩ pull-up)						
Input High Voltage	VIH	VADP=5 to 12V	0.8xVADP			V
Input Low Voltage	VIL				0.2xVADP	V
Hysteresis				0.16 x VADP		V
Supply Current of RTCV	I_{OSC}	RTCV=3V, VBAT=0V All logic: No load.		1		µA

VADP: Adapter voltage

AC Specifications

All specs include temperature unless otherwise noted

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Operational Supply Range	RTCV		2		3.1*	V
Oscillator Frequency	F_{CLK}			32.768		KHz
Start-up Time (note)	t_{START}	RTCV=0V to 3V		100	200	mS
Frequency deviation	f_{DEV}	RTCV=2 to 3V		TBD		

Frequency Jitter Cycle to Cycle >100cycles	f_{JITTER}/SEC	RTCV=3V, TA=25°C	 40* 50*	 nS nS
Long term Drift		RTCV=3V, 3 minutes	10*	ppm

SERIAL INTERFACE

Parameter	Min.	Typ.	Max	Units	Test Condition/Comments
t_{CKS}	50			nS	CLK set-up time
t_{CSS}	50			nS	CS set-up time
t_{CKH}	100			nS	CLK "High" Duration
t_{CKL}	100			nS	CLK "Low" Duration
t_{CSH}	100			nS	CS hold time
t_{CSR}	62			µS	CS recovery time
t_{DS}	50			nS	Input data set-up time
t_{DH}	40			nS	Input data hold time
t_{RD}			50	nS	Data output delay time
t_{RZ}			50	nS	Data output floating time
t_{CSZ}			50	nS	Data output floating time after CS goes low.

Note: These parameters are not tested.

ABSOLUTE MAXIMUM RATINGS

Voltage on ADAPTER pin to GND …….... -0.3, 15Vmax
Voltage on VBAT pin to GND …… -0.3, 7Vmax
Voltage on Pin 6-13, 21-28 to GND …… -0.3, V_{LDO1}+0.3Vmax
Voltage on Pin 1, 62-64 …….. - 0.3, VBAT+0.3V max
Voltage on Pin 20, 32 …….. - 0.3, V_{RTCV}+0.3V max
Voltage on Pin 60, 61 ……... - 0.3, $V_{ADAPTER}$+0.3V max
Voltage on Pin 2-5, 14, 30, 31, 33 ……. - 0.3, 7V max
Storage Temperature Range ……. - 65 to +150 °C
Operating Temperature Range ……. - 30 to +85°C
Maximum Junction Temperature ……. 125°C
θ_{JA} Thermal Impedance (LQFP-64) ……. 2 layer board 76°C/W
θ_{JA} Thermal Impedance (LQFP-64) ……. 4 layer board 54°C/W
Lead Temperature Range (Soldering, 60sec) ……... 300°C

ORDERING GUIDE

Model	Temperature Range	Package
ADP3500AST	-30 C to 85 C	LQFP 64 pins

PIN CONFIGURATION

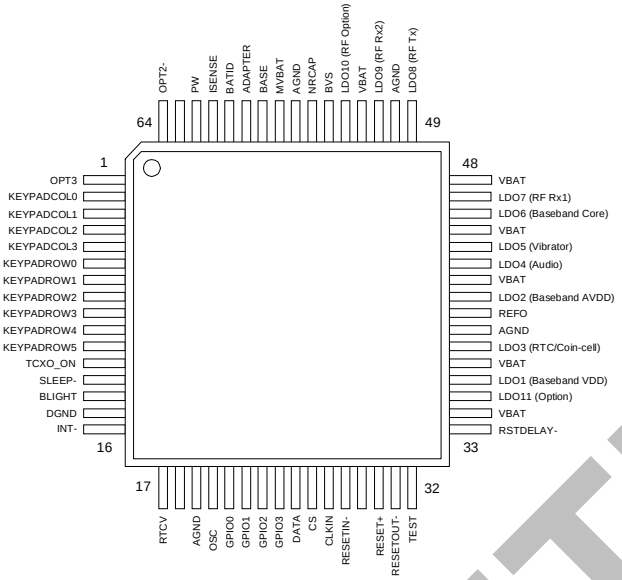


Figure 2. Pin Configuration

PIN DESCRIPTION

Pin	Mnemonic	I/O	Supply	Function
1	OPT3	I	VBAT	Optional Power ON input. ADP3500 will keep "power ON" during this pin goes "High".
2	KEYPADCOL0	O	LDO1	Keypad Column Strobe 0 (Open Drain, pull low)
3	KEYPADCOL1	O	LDO1	Keypad Column Strobe 1 (Open Drain, pull low)
4	KEYPADCOL2	O	LDO1	Keypad Column Strobe 2 (Open Drain, pull low)
5	KEYPADCOL3	O	LDO1	Keypad Column Strobe 3 (Open Drain, pull low)
6	KEYPADROW0	I	LDO1	Keypad Row Input 0. Pulled up internally, 10KΩ
7	KEYPADROW1	I	LDO1	Keypad Row Input 1. Pulled up internally, 10KΩ
8	KEYPADROW2	I	LDO1	Keypad Row Input 2. Pulled up internally, 10KΩ
9	KEYPADROW3	I	LDO1	Keypad Row Input 3. Pulled up internally, 10KΩ
10	KEYPADROW4	I	LDO1	Keypad Row Input 4. Pulled up internally, 10KΩ
11	KEYPADROW5	I	LDO1	Keypad Row Input 5. Pulled up internally, 10KΩ
12	TCXO_ON	I	LDO1	Logic input pin for Main LDOs (LDO1, LDO2, LDO3, LDO6) turning on control. L: OFF, H: ON
13	SLEEP-	I	LDO1	Logic input pin for RF Rx LDOs (LDO7 and LDO9). Gating register data with this input for these LDOs. LDO7 and LDO9 are turned OFF when SLEEP- goes Low even if the registers set to ON.
14	BLIGHT	O	VBAT	LED drive. Open drain output.
15	DGND	-	-	Digital Ground
16	INT-	O	LDO1	Interrupt signal output
17	RTCV	-	-	Supply input for RTC, 32KHz OSC, and some other logics. Connects to Coin cell battery in typical operation.
18	OSCOUT	-	RTCV	Connect to 32.768KHz crystal.
19	AGND	-	-	Analog Ground
20	OSCIN	-	RTCV	Connect to 32.768KHz crystal.
21	GPIO0	I/O	LDO1	General Purpose Input and Output port. Integrated Interrupt function. Interrupt occurs both falling and raising edge.
22	GPIO1	I/O	LDO1	General Purpose Input and Output port. Integrated Interrupt function. Interrupt occurs both falling and raising edge.
23	GPIO2	I/O	LDO1	General Purpose Input and Output port. Integrated Interrupt function. Interrupt occurs both falling and raising edge.
24	GPIO3	I/O	LDO1	General Purpose Input and Output port. Integrated Interrupt function. Interrupt occurs both falling and raising edge.
25	DATA	I/O	LDO1	Serial Interface data input and output.
26	CS	I	LDO1	Serial Interface Chip Select input. Active High input.
27	CLKIN	I	LDO1	Serial Interface Clock input.
28	RESETIN-	I	LDO1	Reset input signal for internal reset signal and starts Stay-Alive timer.
29	32KOUT	O	RTCV	32.768KHz output. Output after 30mS when Reset is released.

30	RESET+	O	RTCV	Reset output. Invert signal of RESETOUT-. Open drain and low OFF leak.
31	RESETOUT-	O	RTCV	Reset output. Follows Voltage Detector operation. Open drain output.
32	TEST	I	RTCV	Test pin. If the pin tied to RTCV, test mode runs. Connect to GND for normal operation.
33	RSTDELAY-	O	RTCV	Reset output. 50mS delayed. Connect to baseband' reset input as typical application. Open drain output.
34	VBAT	-	-	Supply input. Connect to Battery.
35	LDO11	O	VBAT	Regulator #11 output. Use for Optional circuit.
36	LDO1	O	VBAT	Regulator #1 output. Use for Baseband I/O supply.
37	VBAT	-	-	Supply input. Connect to Battery.
38	LDO3	O	VBAT	Regulator #3 output. If VBAT>2.7V, the output is always active. Use for Coin cell supply.
39	AGND	-	-	Analog Ground
40	REFO	O	VBAT	Output of LDO2 through FET switch.
41	LDO2	O	VBAT	Regulator #2 output. Use for Baseband analog supply.
42	VBAT	-	-	Supply input. Connect to Battery.
43	LDO4	O	VBAT	Regulator #4 output. Use for General analog supplies. Ex. Speaker Amp.
44	LDO5	O	VBAT	Regulator #5 output. Use for Vibrator.
45	VBAT	-	-	Supply input. Connect to Battery.
46	LDO6	O	VBAT	Regulator #6 output. Use for Baseband core supply.
47	LDO7	O	VBAT	Regulator #7 output. Use for RF Rx IC supply. Gated with SLEEP- signal input.
48	VBAT	-	-	Supply input. Connect to Battery.
49	LDO8	O	VBAT	Regulator #8 output. Use for RF Tx IC supply.
50	AGND	-	-	Analog Ground
51	LDO9	O	VBAT	Regulator #9 output. Use for RF Rx IC supply. Gated with SLEEP- input signal.
52	VBAT	-	-	Supply input. Connect to Battery.
53	LDO10	O	VBAT	Regulator #10 output. Use for Optional circuit.
54	BVS	-	-	Battery Voltage Sense input for Charger. Connect to Battery.
55	NRCAP	O	VBAT	Noise reduction capacitor. 0.1µF MLCC.
56	AGND	-	-	Analog Ground
57	MVBAT	O	VBAT	Battery voltage divider output. Buffered internally. Connect to Baseband ADC.
58	BASE	O	ADAPTER	Base drive output for PNP pass transistor
59	ADAPTER	-	-	AC adapter input. Use to charger supply.
60	BATID	I	ADAPTER	Battery identification. 100KΩ pulled up internally. "L": Battery exist, "H": No battery. If BATID="H", Charger operates with "No current Limit".
61	ISENSE	I	ADAPTER	Charge current sense input
62	PWRONKEY-	I	VBAT	Power ON/OFF key input. Pulled up internally (140KΩ).
63	OPT1-	I	VBAT	Optional Power ON input. ADP3500 will keep "power ON" during this pin goes "Low".
64	OPT2-	I/O	VBAT	Optional Power ON input. ADP3500 will keep "power ON" during this pin goes "Low". While the part is powered up, the input is pulled to Low (GND) internally. Don't connect to any supply or signal source.

BLOCK DIAGRAM

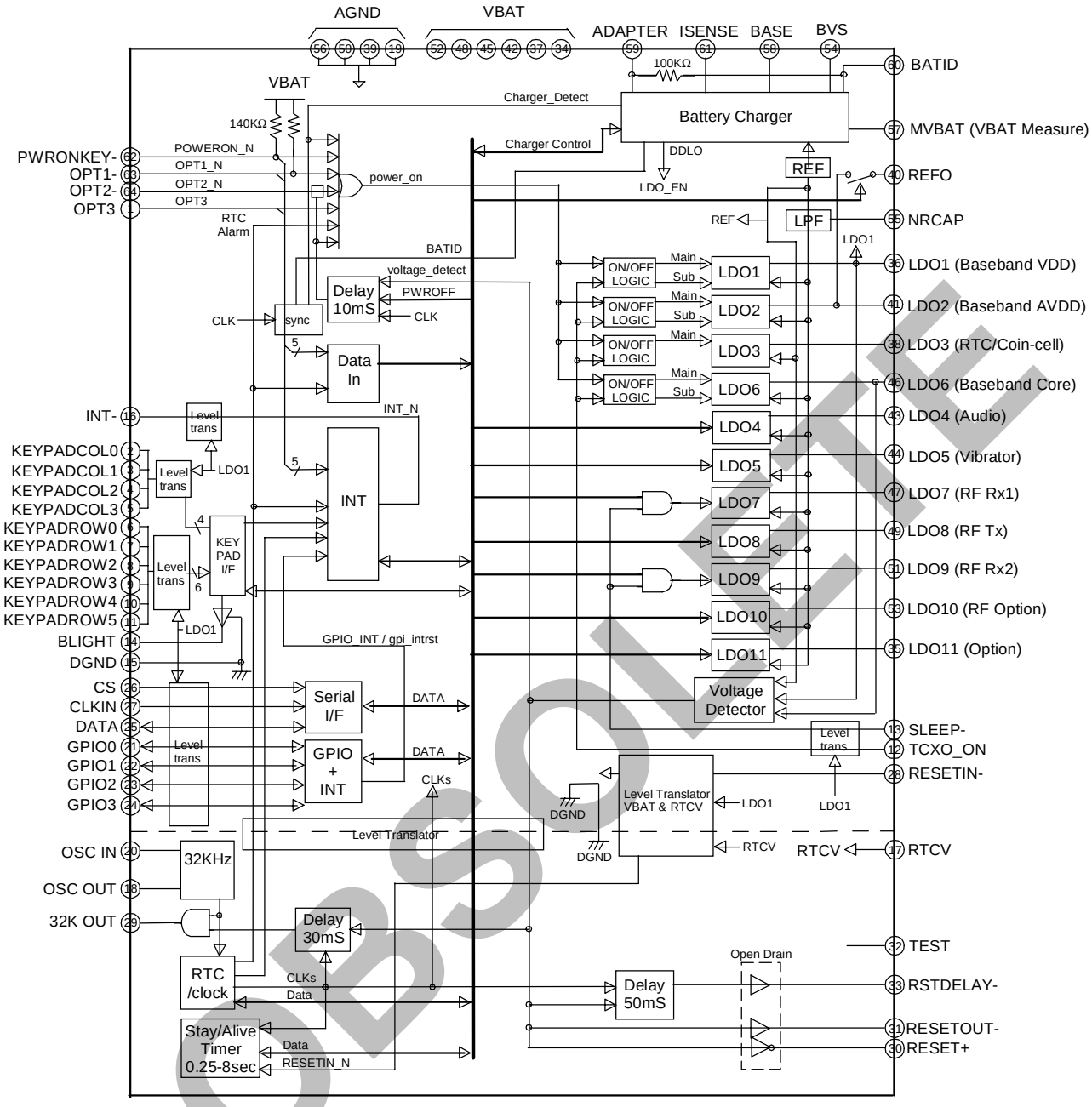


Figure 3. Overall Block Diagram

Theory of Operations

As illustrated in Figure 1 at the beginning, ADP3500 can be divided into two high level blocks – *Analog* and *Logic*. The Analog block mainly consists of LDO regulators, battery charger, reference voltage, and voltage detector sub-blocks, all of which are powered by the main power source(VBAT), namely the main battery or the charging adapter. On the other hand, the Logic block is more complicated. All the Logic sub-blocks are also powered by VBAT except the RTC counter, 32MHz Output control, RESET Output, and Stay-Alive Timer. These sub-blocks are powered from RTCV pin, as indicated in Figure 4 in shaded area.

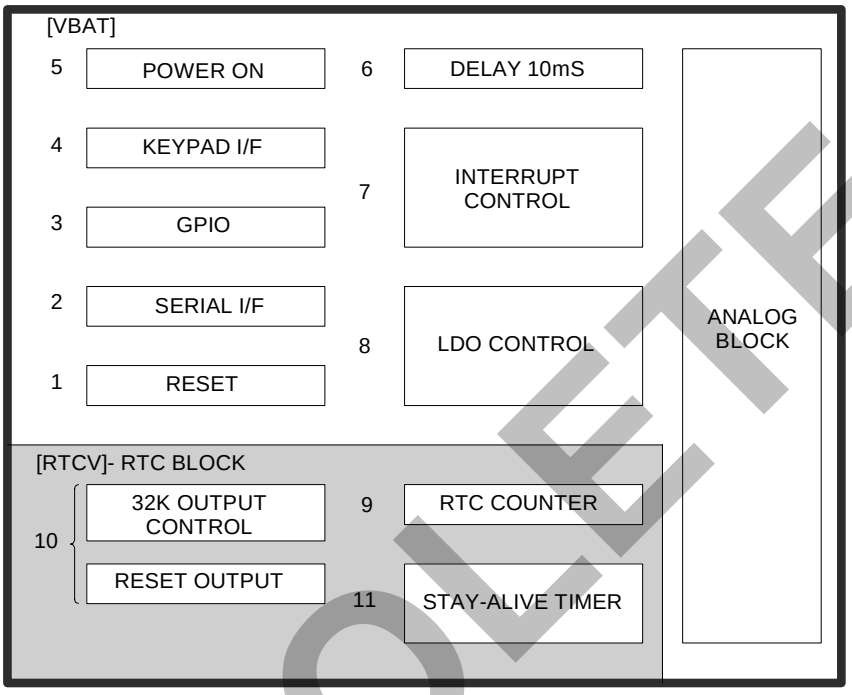


Figure 4. Power partitioning of sub-blocks

1. ANALOG BLOCKS

1.1 LOW DROP-OUT(LDO) REGULATORS

There are total four Sub-LDOs for each LDO1, 2, 3, and 6, in order to meet lower power consumption at light load (stand-by operation). They are used at low load condition, but they are continuously ON even if the each Main-LDOs are ON. The LDO3 and 3b are used for Coin cell and LDO3b is always ON until Main battery (VBAT) is downed to 2.5V due to DDLO function. LDO7 and 9 are controlled with SLEEP- signal. For detail of LDO ON/OFF control, please refer to Section "2.8 LDO Control".

Table 1. Ground currents of LDOs with each handset operations.

LDO names		Baseband VDD	Baseband Core	Coin Cell	Audio	Vibrator	Baseband AVDD	RF Rx1	RF Tx	RF Rx2	RF Option	Option	Main REF	Total LDO IGND
LDO #		1	6	3	4	5	2	7	8	9	10	11		
Power OFF		OFF	OFF	10µA	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	20µA	30µA
Stand-by mode	Light load	10µA	5µA	10µA	OFF	OFF	5µA	OFF	OFF	OFF	OFF	OFF	20µA	50µA
	Mid-load	60µA	55µA	60µA	OFF	OFF	55µA	OFF	OFF	OFF	50µA	OFF	20µA	300µA
	Active load	60µA	55µA	60µA	OFF	OFF	55µA	50µA	50µA	50µA	50µA	OFF	20µA	450µA
Talk		60µA	55µA	60µA	50µA	OFF	55µA	50µA	50µA	50µA	50µA	50µA	20µA	550µA
Ring		60µA	55µA	60µA	50µA	50µA	55µA	50µA	50µA	50µA	50µA	50µA	20µA	600µA

Table 2. LDO operation overview

Regulator	Names	Current Rating (mA)	Voltage (Typ) Or Range	Program steps	Step size (mV)	Default	Cout
LDO1a	Baseband VDD	150	2.90V	N/A	N/A	-	2.2µF
LDO1b	Baseband VDD sub	1	2.87V	N/A	N/A	-	2.2µF
LDO2a	Baseband AVDD	50	2.36V~2.66V	16	20	2.52V	1µF
LDO2b	Baseband AVDD sub	0.3	2.33V~2.63V	16	20	2.49V	1µF
LDO3a	RTC/Coin Cell	50	3.0V	N/A	N/A	-	1µF
LDO3b	RTC/Coin Cell sub	1	2.97V	N/A	N/A	-	1µF
LDO4	Audio	180	2.9V	N/A	N/A	-	2.2µF
LDO5	Vibrator	150	2.9V	N/A	N/A	-	2.2µF
LDO6a	Baseband Core	50	2.6V	N/A	N/A	-	1µF
LDO6b	Baseband Core sub	0.3	2.57V	N/A	N/A	-	1µF
LDO7	RF Rx1	100	2.9V	N/A	N/A	-	2.2µF
LDO8	RF Tx	150	2.9V	N/A	N/A	-	2.2µF
LDO9	RF Rx2	50	2.9V	N/A	N/A	-	1µF
LDO10	RF Option	50	2.9V	N/A	N/A	-	1µF
LDO11	Option	100	1.5V	N/A	N/A	-	2.2µF

1.2 BATTERY CHARGER

1.2.1. Block Diagram

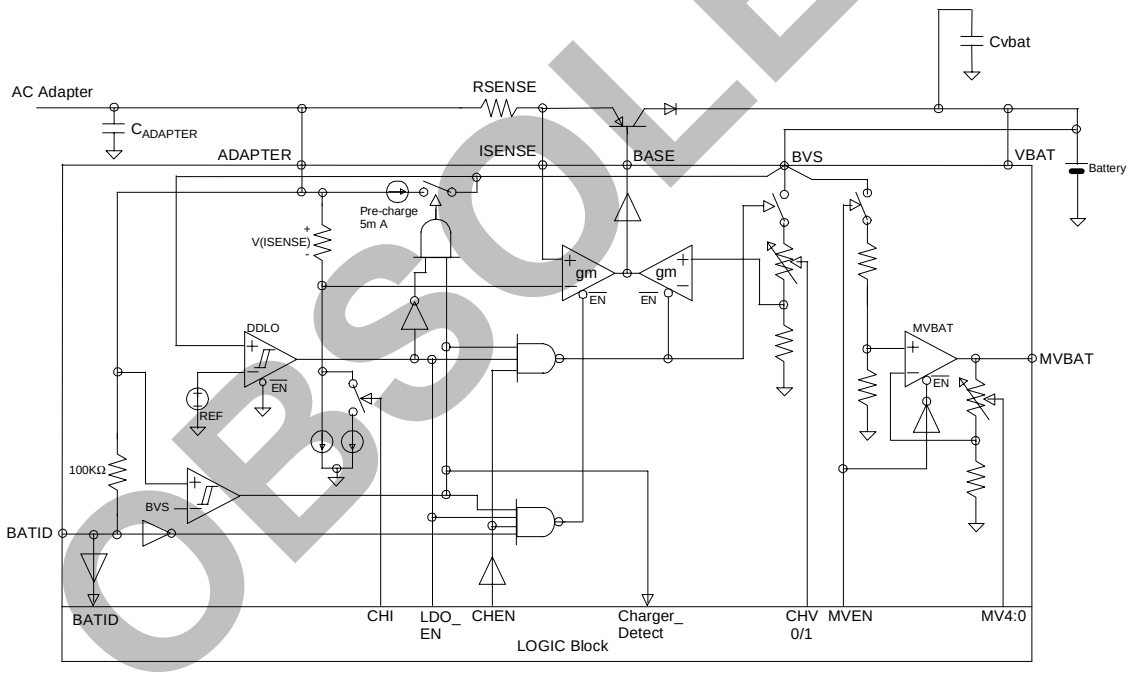


Figure 5. Battery charger block diagram

1.2.2. Flow Chart

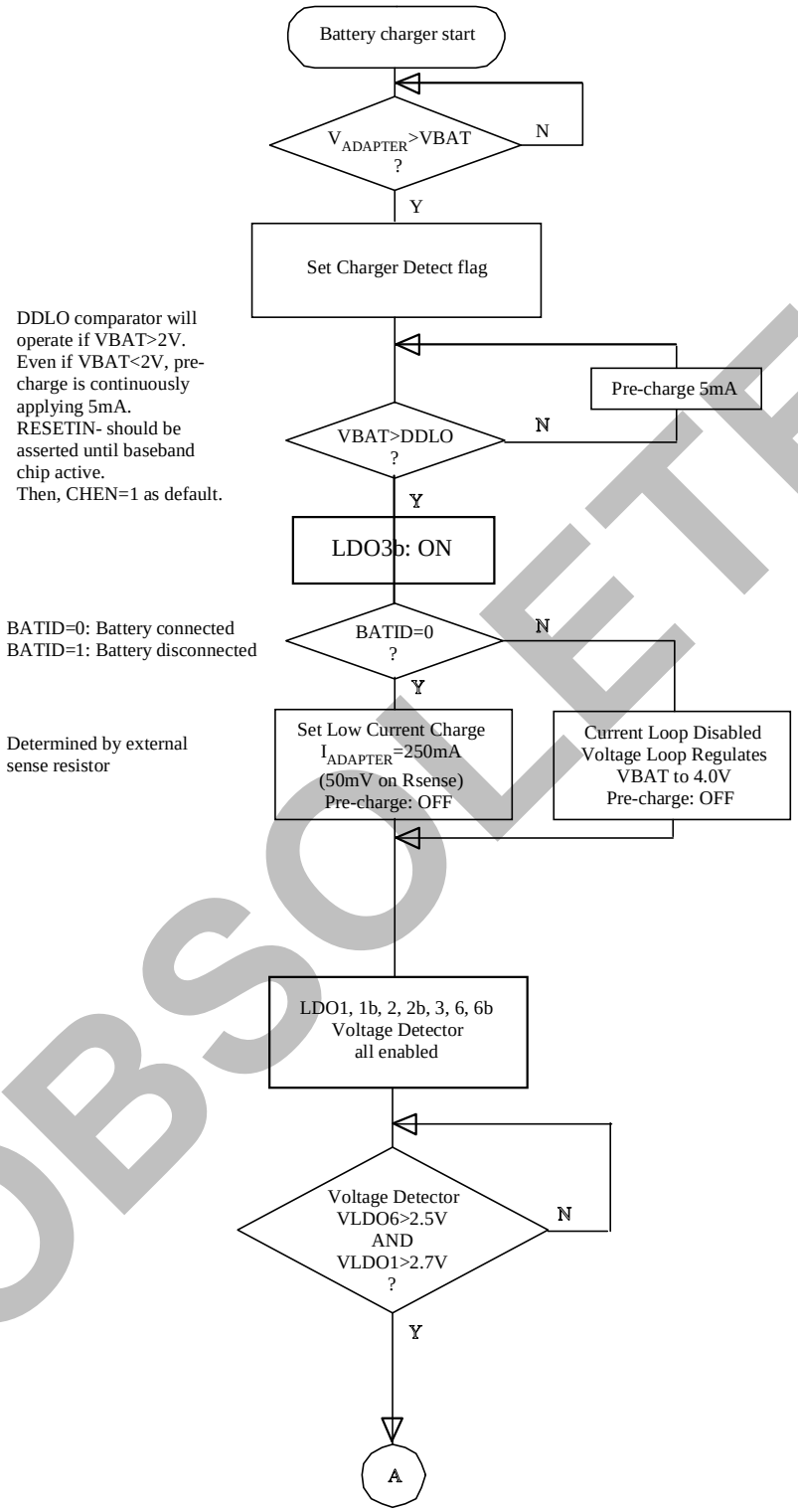


Figure 6. Charger flow chart A

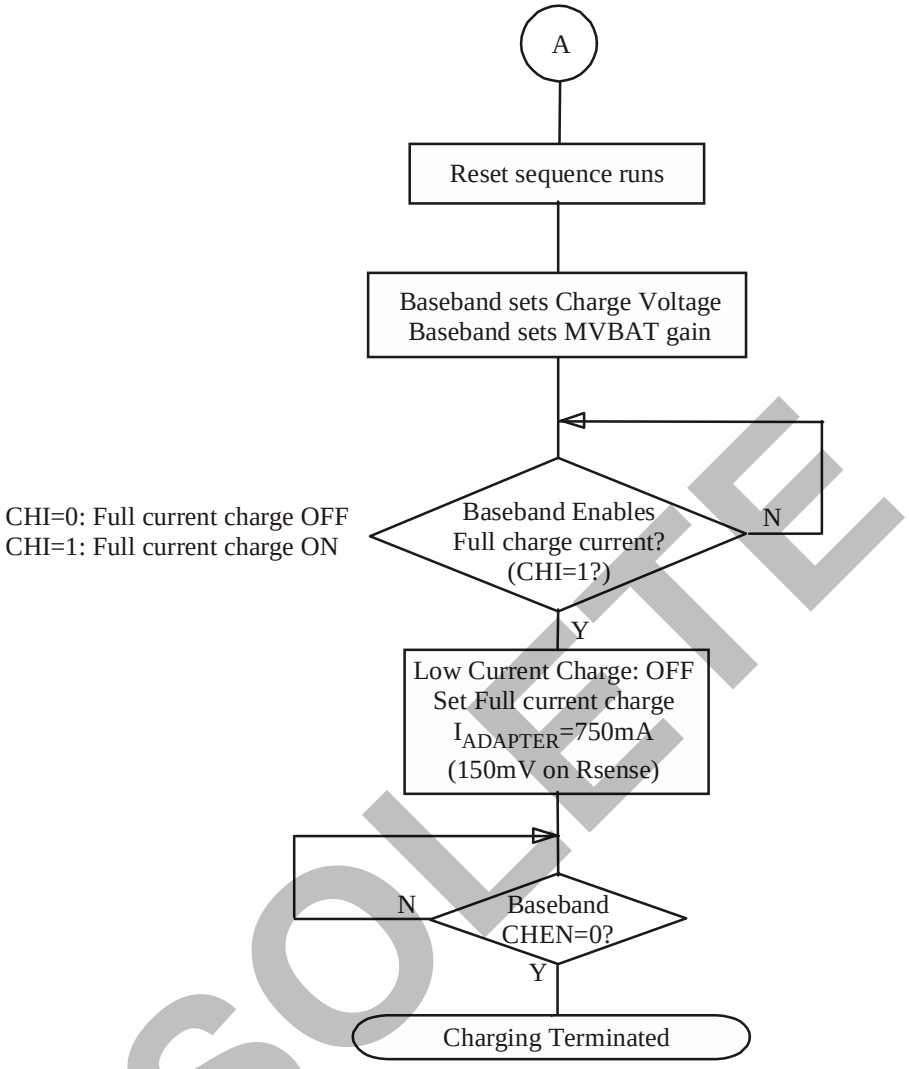


Figure 7. Charger flow chart B

1.2.3. Charger Detect function

The ADP3500 will detect that a charging adapter has been applied when the voltage at the ADAPTER pin exceeds the voltage at BATSNS. The ADAPTER pin voltage must exceed the BVS voltage by a small positive offset. This offset has hysteresis to prevent jitter at the detection threshold. The charger detection comparator will set the Charger_Detect flag in the 20h register and generate an interrupt to the system. If the ADAPTER input voltage drops below the detection threshold, charging will stop automatically and the Charger_Detect flag will be cleared and generate an interrupt also.

1.2.4. DDLO function and operation

The ADP3500 contains a comparator that will lock out system operation if the battery voltage drops to the point of deep discharge. When the battery voltage exceeds 2.675 V, the reference will start as will the sub-LDO 3b. If the battery voltage drops below the hysteresis level, the reference and LDO's will be shut down, if for some reason they are still active. Since LDO1 will be in deep dropout and well below the voltage detector threshold at this point, the reset generator will have already shut down the rest of the system via RESET+, RESETOUT-, and RSTDELAY-.

If a charging adapter has been applied to the system, the DDLO comparator will force the charging current to trickle charge if the battery is below the DDLO threshold. During this time, the charging current is limited to 5 mA. When the battery voltage exceeds the upper threshold, the low current charging is enabled, which allows 55 mV (typical) across the external charge current sense resistor. See also Figure 6, the Battery Charger Flowchart.

1.3 MVBAT

The ADP3500 provides a scaled buffered output voltage for use in reading the battery voltage with an A/D converter. The battery voltage is divided down to be nominally 2.600 V at full scale battery of 4.35 V. To assist with calibrating out system errors in the

ADP3500 and the external A/D converter, this full scale voltage may be trimmed digitally with 5 bits stored in register 12h. At full scale input voltage, the output voltage of MVBAT can be scaled in 6 mV steps, allowing a very fine calibration of the battery voltage measurement. The MVBAT buffer is enabled by the MVEN bit of register 11h, and will consume less than 1 uA of leakage current when disabled.

1.4 REFERENCE

The ADP3500 has an internal, temperature compensated and trimmed band-gap reference. The battery charger and LDO's all use this system reference. This reference is not available for use externally. However, to reduce thermal noise in the LDOs, the reference voltage is brought out to the NRCAP pin through a 50kohm internal resistor. A cap on the NRCAP pin will complete a low pass filter that will reduce the noise on the reference voltage. All the LDO's, with the exception of LDO3, use the filtered reference.

Since the reference voltage appears at NRCAP through a 50kohm series internal impedance, it is very important to never place any load current on this pin. Even a volt meter with 10 megohm input impedance will affect the resulting reference voltage by about 6 or 7 mV, affecting the accuracy of the LDO's and charger. If for some reason the reference must be measured, be certain to use a high impedance range on the volt meter or a discrete high impedance buffer prior to the measurement system.

2. LOGIC BLOCKS

ADP3500 has following logic functions.

- Three wire Serial Interface (CS, CLK, DATA)
- RTC counter section has Year, Month, Day, Week, Hour, Minute, and Second, and controls Leap year, and days in month automatically.
- Detect Alarms based on RTC counter.
- Periodically constant interrupt feature. (2Hz, 1Hz, 1/60Hz, 1/3600Hz, Once a months)
- GPIO and INT ports control
- Key-pad interface
- LED light control
- LDO functions
- Clock and Reset output control
- Stay-Alive timer

Following is a block diagram based on Logic circuit.

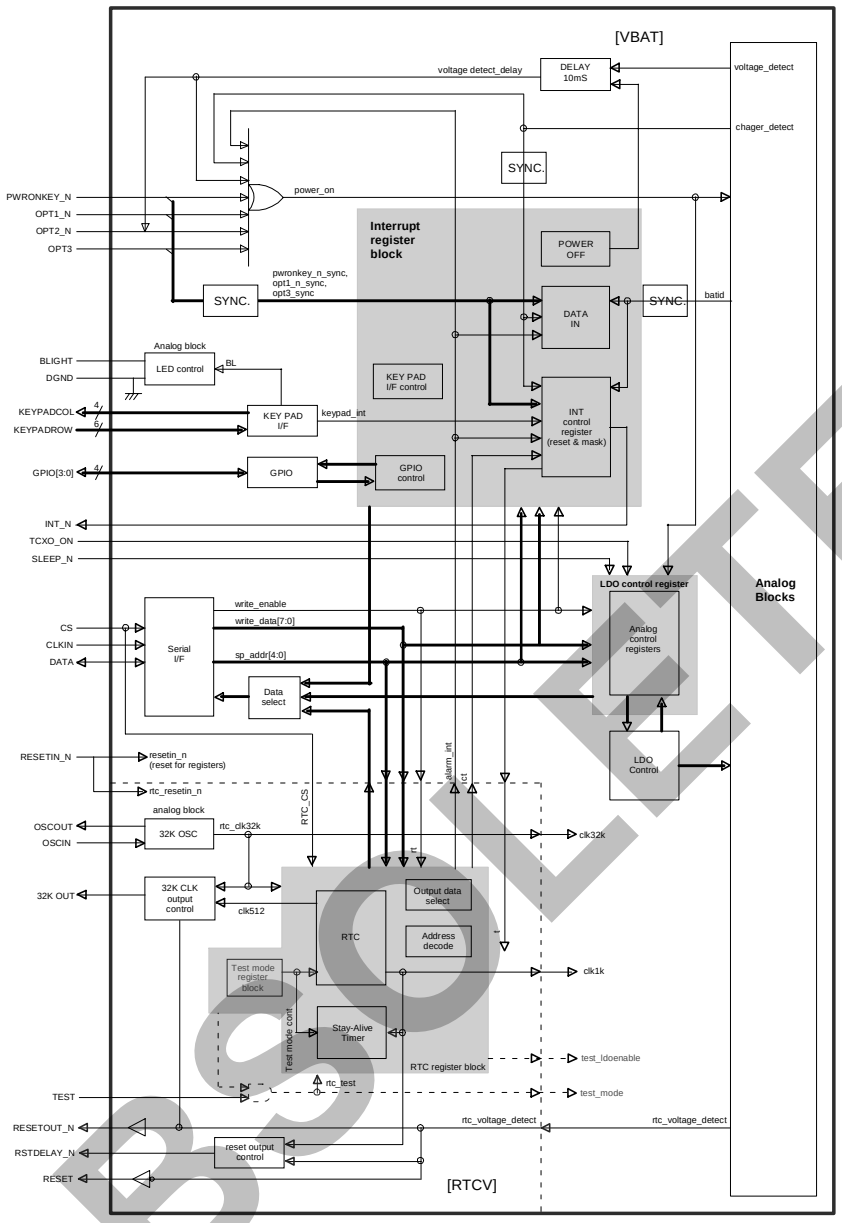


Figure 8. LOGIC block diagram

2.1 RESET

2.1.1 RESETIN- signal

The internal reset function is activated by external reset input, RESETIN-, and this is an asynchronous signal. The internal reset signal is used in the following blocks.

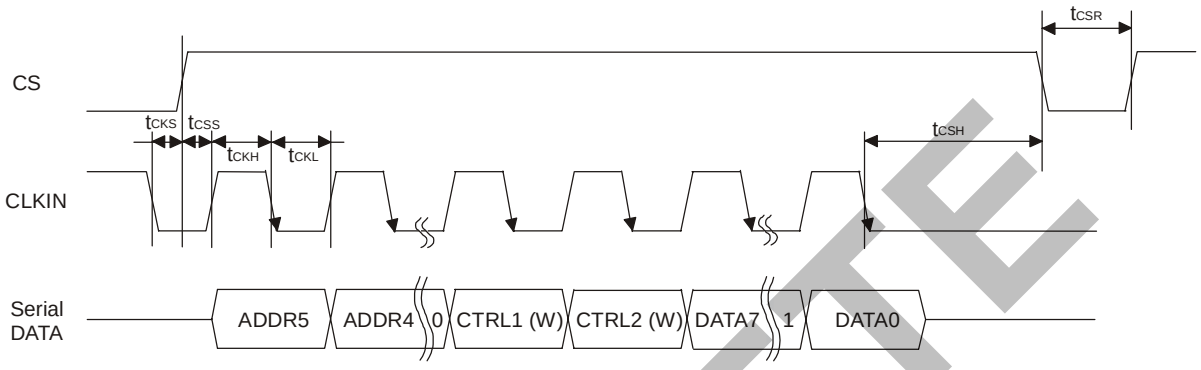
- Serial I/F
- Interrupt control
- Stay-Alive timer
- Registers (refer to the Register section for detail).

LDOs, controlled by Serial I/F, are applied "RESET" by RESETIN-. LDO4, LDO5, LDO7, LDO8, LDO9, LDO10, LDO11 and REF0 are set to "0". In case RESETIN- has noise, the internal circuit may be in reset and cause the system unexpected result. Please take enough treatment. RESETIN- is level translated from LDO1 to both VBAT and RTCV supplies.

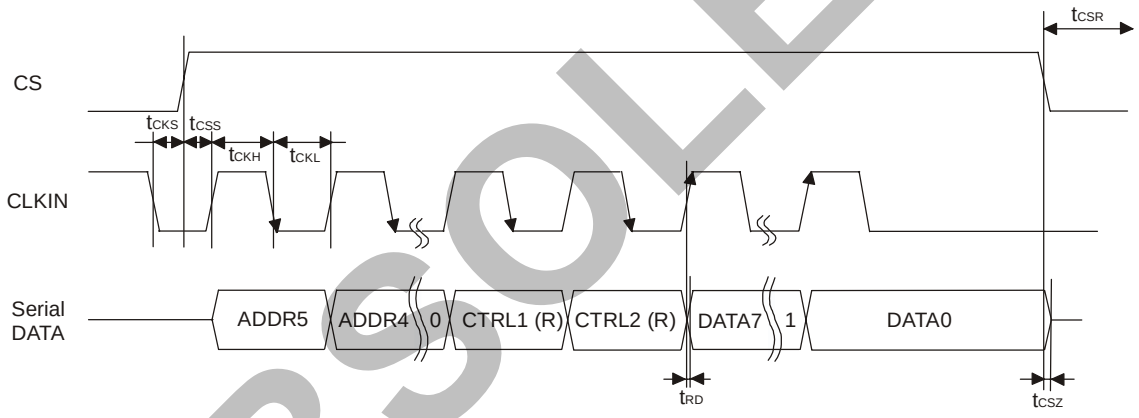
2.1.2 RESET output control and 32KHz output control

Using Voltage Detect signal, device generates 32K OUT, RSTDELAY-, RESETOUT-, and RESET signals. About 32mS after rtc_voltage_detect (Voltage Detect signal in RTCV supply) signal goes from "0" to "1", 32K OUT signal is generated from internal RTC_CLK32K signal. RSTDELAY_N (RSTDELAY-) goes to "0" when rtc_voltage_detect is "0", and it goes to "1" at 50mS after the "0" to "1" transition of rtc_voltage_detect. RESETOUT_N (RESETOUT-) and RESET toggle their states. Signal clk512 is a 512Hz, which generated in USEC counter block.

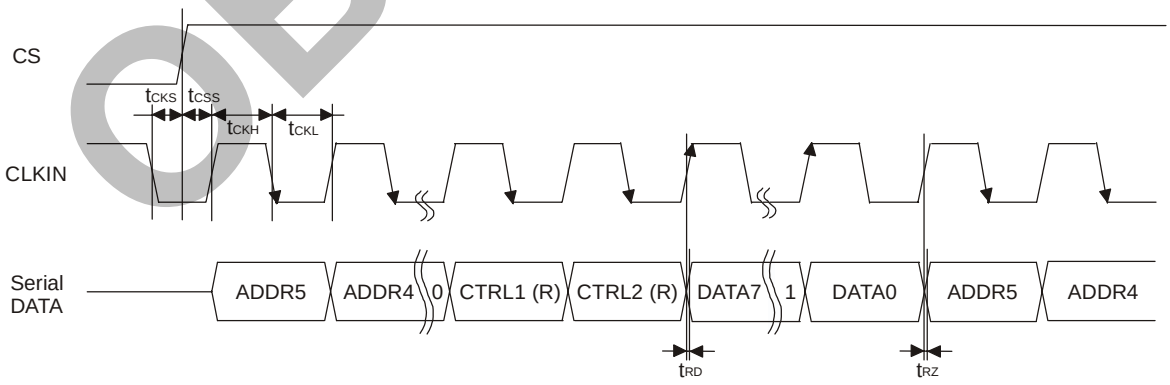
2.2 SERIAL INTERFACE



Serial I/F WRITE Timing



Serial I/F READ Timing Single Mode



Serial I/F READ Timing Continuous Mode

Figure 9. Serial Interface signal

Table 3. Set up and Hold Specifications

Parameter	Min.	Typ.	Max	Units	Test Condition/Comments

t_{CKS}	200			nS	CLK set-up time
t_{CSS}	400			nS	CS set-up time
t_{CKH}	400			nS	CLK "High" Duration
t_{CKL}	400			nS	CLK "Low" Duration
t_{CSH}	500			nS	CS hold time
t_{CSR}	62			µS	CS recovery time
t_{DS}	200			nS	Input data set-up time
t_{DH}	200			nS	Input data hold time
t_{RD}			300	nS	Data output delay time
t_{RZ}			300	nS	Data output floating time
t_{CSZ}			300	nS	Data output floating time after CS goes low.

2.2.1. Function block

ADP3500 integrates the serial bus interface for easy communication with the system. The data bus consists of three wires, CLK, CS, and DATA, and is capable of Serial to Parallel / Parallel to Serial conversion of data, as well as clock transfer.

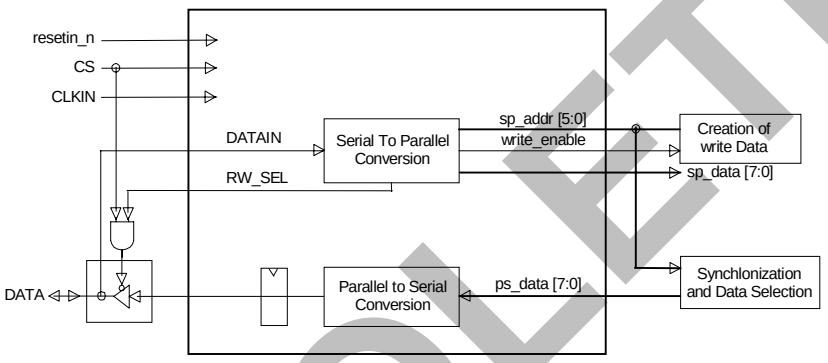


Figure 10. Serial Interface block diagram

Serial interface block works during the time period at CS signal enable. After the falling edge of CLKIN signal right after the rising edge of CS signal, Address, transfer control signal and write data are held in sequentially. In case DATA READ, each of data will be prepared by rising edge of CLKIN and baseband chip may want to read or latch the data at falling edge of CLKIN. While CS is not asserted, CLKIN is ignored. If CS goes "L" while CLKIN is continuously applied or input DATA, all data is canceled and DATA line would be High impedance. In this case, user needs to input the data again. Please note that CLKIN should be stayed "L" when CS goes H. RTC counter registers should be accessed at a certain time (>62µS) later after CS assertion. Asserting RESETIN_N (RESETIN-) signal resets the block..

Notes:

- CLKIN=10KHz to 1MHz, 20/80% duty cycle.
- CLKIN should be "L" when CS goes "H".
- In case of RTC counter access, the access should be approximately 62µS, (2 clock cycles of CLK32K) after the CS signal is asserted, to hold the RTC value.
- The CS should not be asserted for 62µS, (2 clock cycles of CLK32K) after the CS is released.
- CS signal should never be asserted for 1 sec or longer, otherwise RTC counter makes error.

2.2.2 Data input/output timing

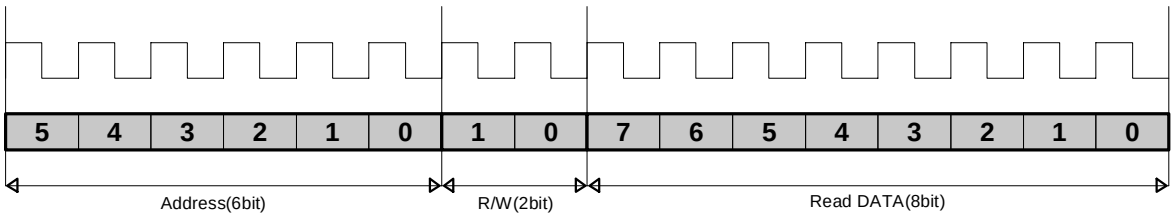


Figure 11. Serial I/F Data read/write timing

SP_ADDR[5:0] : 6bit address
SP_CTRL[1:0] : 2bit Read/Write control (01: Write, 10: Read)
SP_DATA[7:0] : 8bit Input/Output Data
* All transfer will be done MSB first.

2.3 GPIO+INT

GPIO block has 4 channel I/O function and interrupt. With GPIO CONTROL register (1Ah), it is possible to control Input or Output setting of each channel individually. The output data is set in GPIO register (1Ch). When the port is set as input mode, the input signal transition from "1" to "0" and from "0" to "1", then generate interrupt signal with Edge detection. The held interrupt signals are reset by GPIO INT RESET register (1Dh). Setting GPIO MASK register (1Bh) to "1" enables the interrupt of GPIO. (Not MASKED, "1" at default in reset.)

2.4 INT REGISTER

In case the interrupt event has occurred, "1", the signal is held in this register. INT detect and Reset are synchronized at the rising edge of CLK32K. In case the interrupt event and reset signal are occurred at same time, interrupt event has priority. RESETIN_N signal resets INT register (1Eh) to "0" (No INT detected), except alarm_int and ctfg_int. INT MASK register (1Fh) to "1" (not masked). This block masks alarm_int and ctfg_int, which generated in RTCV block, but these signals are reset with ALARM CONTROL register (0Dh) and CTFG CONTROL register (0Eh). The interrupt signal, INT_N, is an "inverted OR" signal of value in INT register and GPIO register.

DATA-IN register is a port to read an interrupt status. The input data are through SYNC block except Alarm signal. Since this is for just read back purpose, user cannot write any data.

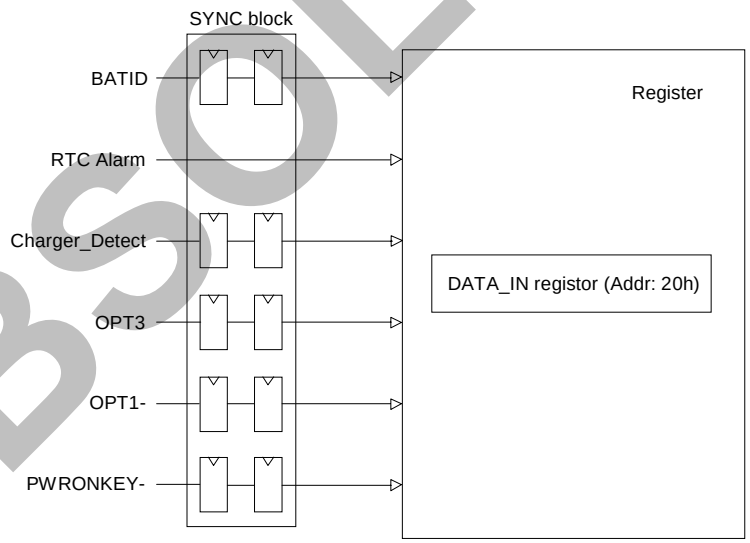


Figure 12. DATA-IN block

2.5 KEYPAD CONTROL & LED DRIVE

KEYPADCOL[3:0] are Open Drain output. The KEYPADROW[5:0] are Falling edge trigger input (input state transition from "1" to "0") and generate Interrupt signal, and are pulled up to LDO1. By providing 4 keypad-column outputs and 6 keypad-row inputs the ADP3500 can monitor up to 24 keys with baseband chip. Writing Column outputs and Reading Row inputs are controlled through serial interface. The address of the KEYPADROW is 19h, and KEYPADCOL is 18h. Initial register value is "0" that means an output of KEYPADCOL is "High Impedance".

Back-light drive is an open drain output. Maximum current of internal FET is 100mA. Initial register value is "0" that means the output of BLIGHT is "High impedance".

2.6 POWER ON INPUT

PWRONKEY and OPT1 have pull-up resistors, and others are not. In addition to these inputs, other internal input signals such as charger_detect and Alarm signal (alarm_int) from RTC enable Main and Sub LDOs of LDO1, 2, 3 and LDO6. Power ON status is hold by a latch data in Delay circuit, called voltage_detect_delay (please see 4.8 for more detail). OPT3 has a lower voltage threshold. OPT2 is different structure to the other inputs, and is pulled down to zero by internal signal when phone is Power ON status, in order to make sure to have Power ON status even if short-term disconnection is happened. Following is a block diagram and Power on sequence.

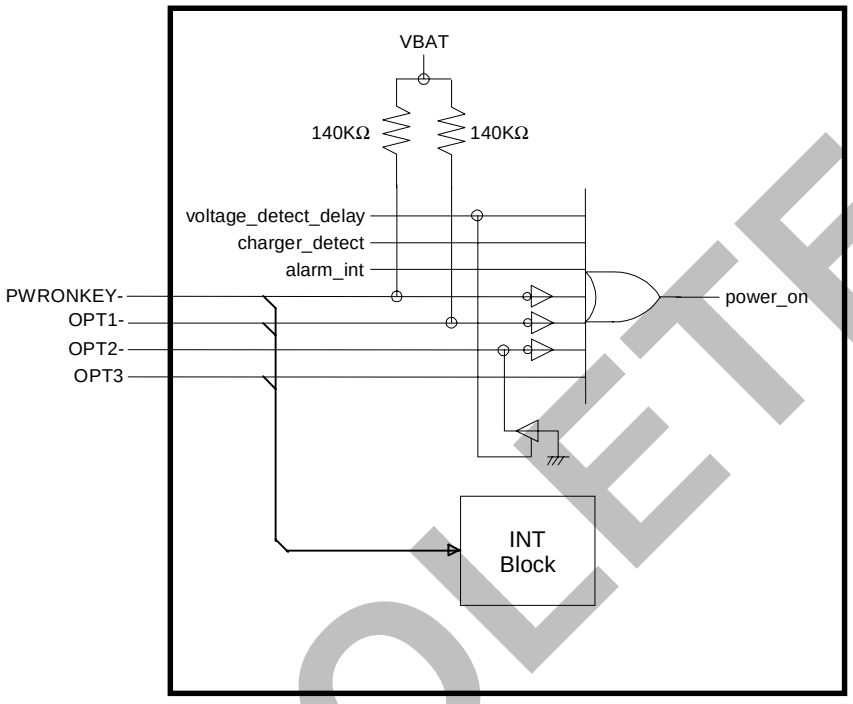


Figure 13. Power ON input block diagram

- Voltage_detect_delay : Voltage Detect Signal (10mS delay) (1: Assert)
- charger_detect : Charger Detect Signal (1: Assert)
- alarm_int : Alarm Detect Signal (Alarm 1 or 2) (1: Assert)
- PWRONKEY- : Power On key input (0: Assert)
- OPT1- : Power On signal (0: Assert)
- OPT2- : Power On signal (0: Assert)
- OPT3 : Power On signal (1: Assert)

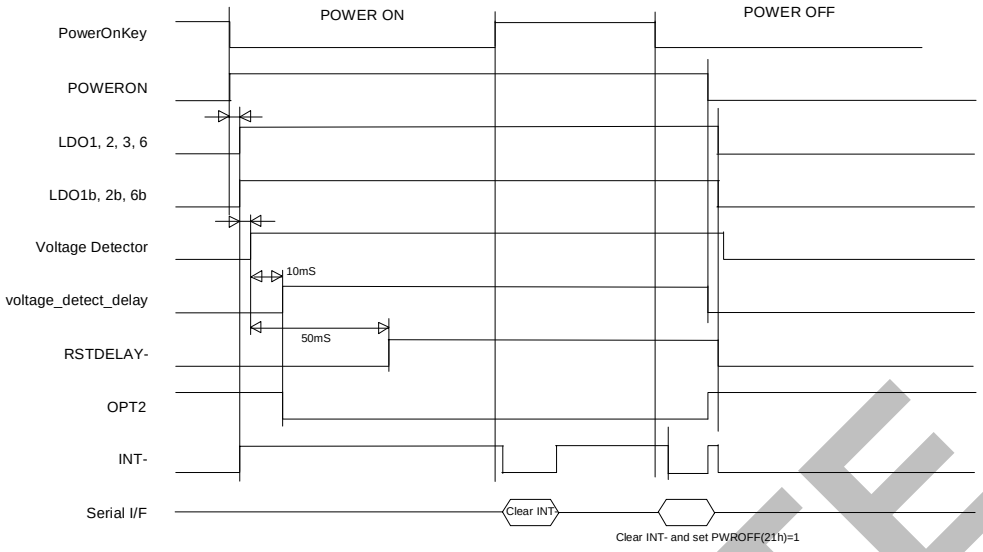


Figure 14. Power ON sequence

2.7 10 MILISECOND DELAY

This block generates a 10mS delayed signal after the reset of the voltage_detect signal is released. After 10mS (11 clocks of 1024Hz) since the voltage_detect signal is asserted, the voltage_detect_delay signal is asserted. If the duration of the voltage_detect signal is less than 10mS, voltage_detect_delay signal will not be asserted. When the voltage_detect signal is released, the voltage_detect_delay signal is also released simultaneously. The voltage_detect_delay signal can be reset with writing "1" in POWER OFF register (21h).

* User just need to write "1" in the POWER OFF register to reset voltage_detect _delay, and not need to over-write it with "0".

2.8 LDO CONTROL

The LDO control block controls Power ON/OFF of LDO block. The function in this block has:

- Hardware control using external signals
- Software control using serial interface
- Mixture of hardware and software above

LDO1, LDO2, LDO3, and LDO6 are structured with Main and Sub LDOs. LDO4, LDO5, LDO7, LDO8, LDO9, LDO10, and LDO11 are set through serial interface but LDO7 and LDO9 are gated (AND gate) with SLEEP- signal, in order to get into Sleep mode. If the SLEEP- signal is enabled (goes "Low"), the outputs of LDO7 and LDO9 are turned OFF. Remainder of LDOs as LDO1, LDO2, and LDO6 is controlled by "Power On Logic". A Sub LDO called "LDO3b" is independent control and this LDO control block doesn't control LDO3b. And Main LDO3 called "LDO3a" is turned on by power_on signal, but Sub LDO3 called "LDO3b" is always ON while Battery supplies and LDO3b is only controlled by DDLO. A DDLO is control signal from Battery charger block and is monitoring Battery voltage. When VBAT is under 2.5V (200mV hysteresis from VBAT=2.7V), DDLO minimizes (DDLO enable) current flow from Li-Ion battery.

Main LDOs : LDO1a, LDO2a, LDO3a, LDO6a
Sub LDOs : LDO1b, LDO2b, LDO3b, LDO6b

Table 4a. DDLO status table

Status	LDO1a	LDO1b	LDO2a	LDO2b	LDO3a	LDO3b	LDO4	REFO	LDO5	LDO6a	LDO6b	LDO7	LDO8	LDO9	LDO10	LDO11
	Baseband VDD		Baseband AVDD		Coin cell		Audio	REFO	Vibrator	Baseband Core		Rx1	Tx	Rx2	RF Option	Option
DDLO Enable	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DDLO Disable	X	X	X	X	X	ON	X	X	X	X	X	X	X	X	X	X

Note

1. "X" means a status of LDO depends on other conditions.

Table 4b. LDO Control Event Table

Event	LDO1a	LDO1b	LDO2a	LDO2b	LDO3a	LDO3b	LDO4	REFO	LDO5	LDO6a	LDO6b	LDO7	LDO8	LDO9	LDO10	LDO11
	Baseband VDD		Baseband AVDD		Coin cell		Audio	REFO	Vibrator	Baseband Core		Rx1	Tx	Rx2	RF Option	Option
POWER ON (Note 2)	ON	ON	ON	ON	ON					ON	ON					
TCXO_ON (Note 3)	ON/ OFF		ON/ OFF		ON/ OFF					ON/ OFF						
SLEEP- (Note 4)												ON/ OFF		ON/ OFF		
RESETIN-							OFF	OFF	OFF			OFF	OFF	OFF	OFF	OFF
"ALLOFF" bit goes "H"							OFF	OFF	OFF			OFF	OFF	OFF	OFF	OFF
"PWROFF" bit goes "H"	OFF	OFF	OFF	OFF	OFF		OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Notes

1. This table only indicate the change of status caused by an event. Blank cells means "no change" and keep previous status
2. Power ON Event: Indicating a status just after the power ON event. After the event, a status of LDO1a, 2a, 3a, and LDO6a are changed by TCXO_ON signal.
3. TCXO_ON: Hardware control, change all Main-LDO' ON/OFF status.
4. SLEEP-: The LDO7 and LDO9 are able to be controlled by software if SLEEP="H" level. If SLEEP- goes "L", these LDOs are turned OFF immediately.

Table 4c. Software Controllability of LDOs

LDO description	LDO1a	LDO1b	LDO2a	LDO2b	LDO3a	LDO3b	LDO4	REFO	LDO5	LDO6a	LDO6b	LDO7	LDO8	LDO9	LDO10	LDO11
	Baseband VDD		Baseband AVDD		Coin cell		Audio	REFO	Vibrator	Baseband Core		Rx1	Tx	Rx2	RF Option	Option
Software Turn ON							√	√	√			√ (Note1)	√	√ (Note1)	√	√
Software Turn OFF	√	√	√	√	√		√	√	√	√	√	√	√	√	√	√

Note

1. LDO7 and LDO9 have a gate with SLEEP-. If SLEEP- is in "L" (active) status, user cannot control and both LDOs are kept to "OFF" status. User may want to use this function as immediate control to get OFF status by using SLEEP- hardware control while set register "1" to the LDO control register.

2.9 RTC BLOCK

The Calendar registers are set through serial interface.

2.9.1 Function

- RTC counter using binary
- Reading out and writing setting s of Year, Month, Day, Week, Hour, Minute, and second data.
- Leap year controls, Number of days in a month control
- Alarm function (Weak, Hour, Minute)
- Periodic Interrupt function - 2Hz, 1Hz, 1/60Hz, 1/3600Hz, Each month (First day of each month)
- Protection of wrong data readout during RTC data update.

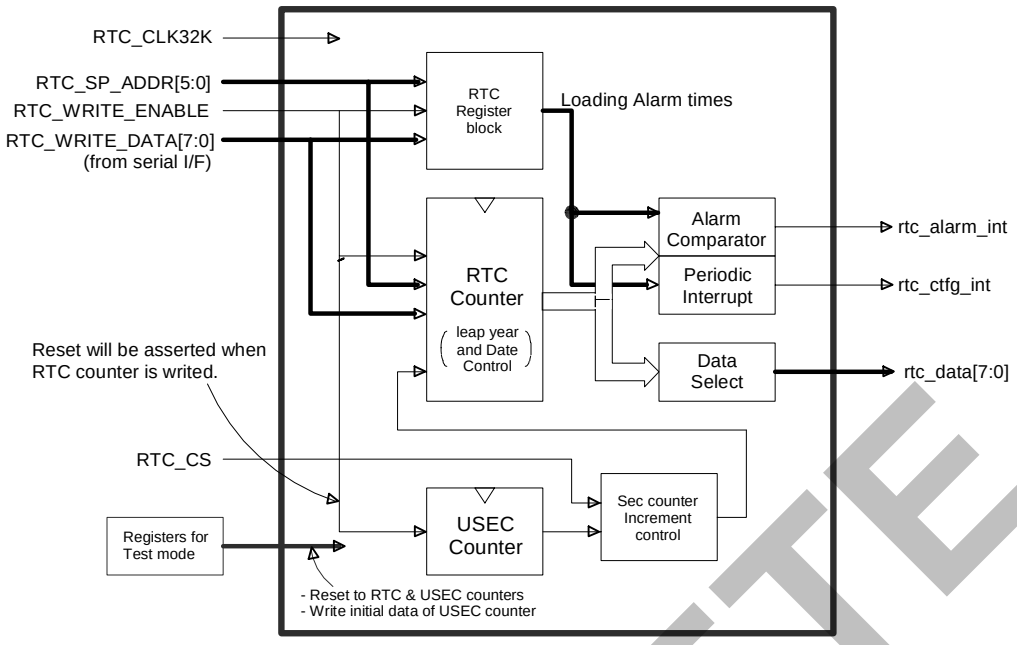


Figure 15. RTC counter block

2.9.2 Operation

Synchronizing with RTC_CLK32K clock, USEC counter generates 1sec timing clock and the clock hits RTC counter. Through the serial interface, CPU can write setting value and read RTC counter value. In case the RTC counter toggles during the serial interface access to RTC counter, the wrong data can be read/write between RTC counter and interface. CS signal stops the clocking to RTC counter until CS signal is released. In case CPU writes data into SEC counter, USEC counter is reset to zero.

Note

- In case of RTC counter access, the access should be waited approximately 62µS, (2 clock cycles of CLK32K) after the CS signal is asserted, to hold the RTC value.
- CS signal should never be asserted 1sec or longer, this affects counter operation.

2.9.3 Operation of USEC counter

USEC counter counts up synchronizing with RTC_CLK32K clock. It generates 1sec timing signal and it is used as an increment clocking of RTC counter. In case the 1sec signal is generated during CS signal asserted, the increment clock is delayed until CS signal is released.

2.9.4 Operation of RTC counter

RTC counter uses the increment signal from USEC counter to control counting operation including the leap year control and numbers of days in a month control.

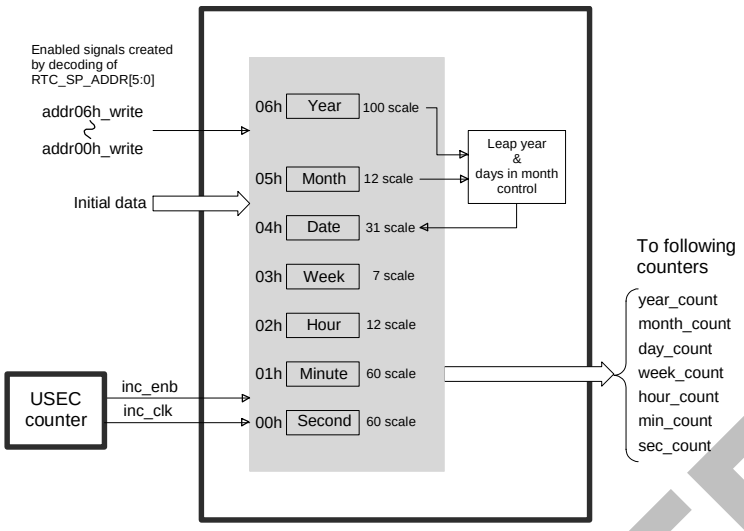


Figure 16. RTC counter block diagram

Definition of Leap year
The definition of a leap year is, "a year which can be divided by 4 and can not be divided by 100" and "a year which can be divided by 400." For this device, the following definition is used instead.

"A year which can be divided by 4"

Note - Year counter = "00" means year 2000, and is a leap year because it can be divided by 400.
- Actual covered year period is from 1901 to 2099.

Number of days of month control
Months 1, 3, 5, 7, 8, 10, 12 have 31days.
Months 4, 6, 9, 11 have 30days.
Month 2 has 28days, but has 29 in leap year.

2.9.5 Alarm Function
Comparing the RTC counter value with the seting value in alarm_setting register (07h-09h), alarm condition is detected. Setting of week uses 7bits for each day in a week, and works with multiple days setting. There is a delay of 62µS from Alarm detection to setting up to AOUT/BOUT registers.

ALA_EN flag in ALARM CONTROL register (0Dh) sets Enable/Disable of alarm detection. INT register (1Eh) indicates the interrupt signals, alarm_int of ALA or/and ALB. INT MASK register (1Fh) do mask of alarm interrupt signal. Alarm detection state is indicated as AOUT of ALARM CONTROL register (0Dh), and the alarm can be released by writing "1" at the bit. Alarm B is also controlled as same as Alarm A is.

Note: User just need to write "1" to release the alarm, and not need to write "0" after "1". User doesn't need to wait 62µS from CS assertion.

2.9.6 Periodic Interrupt function
This is a function, which generates interrupt periodically. The timing of cycle can be selected from 2Hz (0.5sec clock pulse), 1Hz (1sec clock pulse), 1/60Hz (minutes), 1/3600Hz (hour), and month (first day of each month).

The cycle is set using CT2-CT0 value in CTFG CONTROL register (0Eh). The state when interrupt is generated is indicated at INTRA bit of CTFG CONTROL register (0Eh). INT MASK register (1Fh) only does mask of periodic interrupt signal. There are two kinds of pattern of CTFG Interrupt signal output.

- Hold the value when the interrupt is occurred (level).
- After the interrupt event is happened, assert interrupt signal in certain time period then release it (pulse).

In level case, interrupt is occurred at each 0 min (1/60Hz), 0 o'clock (1/3600Hz) or at first day of month. Because they are happened in long cycle, the value is held at register. After the CPU checks the state, it is released by writing "1" at CTFG bit of CTFG CONTROL register. In case of 2Hz and 1Hz, the interrupt is not held because the event happens in short cycle. These event signal output pulse signal of 2Hz or 1Hz in RTC counter directly. Interrupt release operation doesn't affect on the interrupt signal in the case.

2.10 STAY-ALIVE TIMER

This is a counter, which increments each 250mS after RTC_RESETIN_N is asserted. It holds its value when the counter counts full up. Signal clk4 is a 4Hz (250mS) clock which generated in USEC counter. The counter can be reset by writing "1" at CLR of Stay-Alive TIMER CONTROL register (0Fh). The RTC_RESETIN_N signal is transferred from a logic input circuit, that is supplied by VBAT, of RESETIN_N.

Note : User just need to write "1" to release the interrupt, and not need to write "0" after "1".

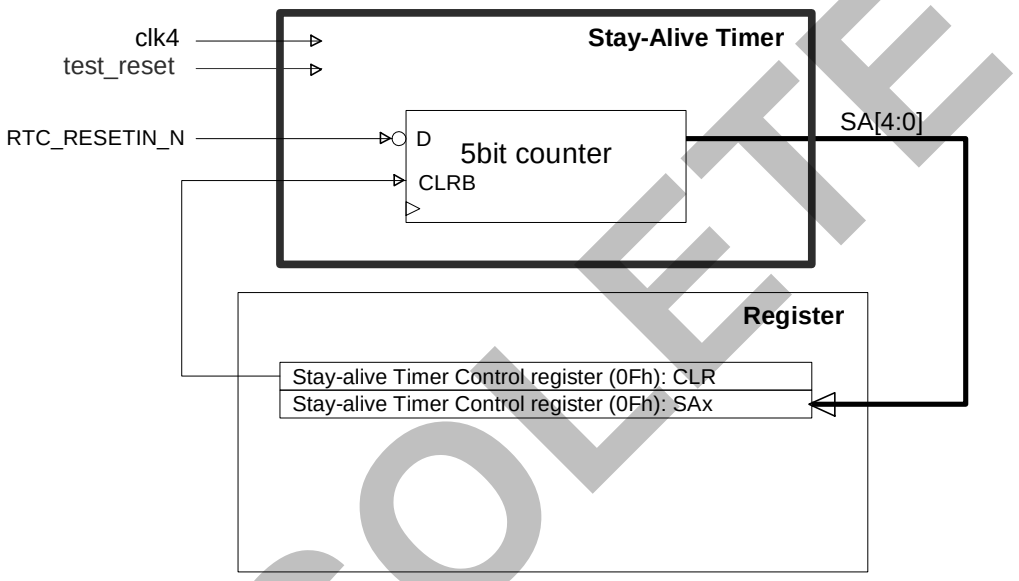


Figure 17. Stay-Alive Timer block diagram

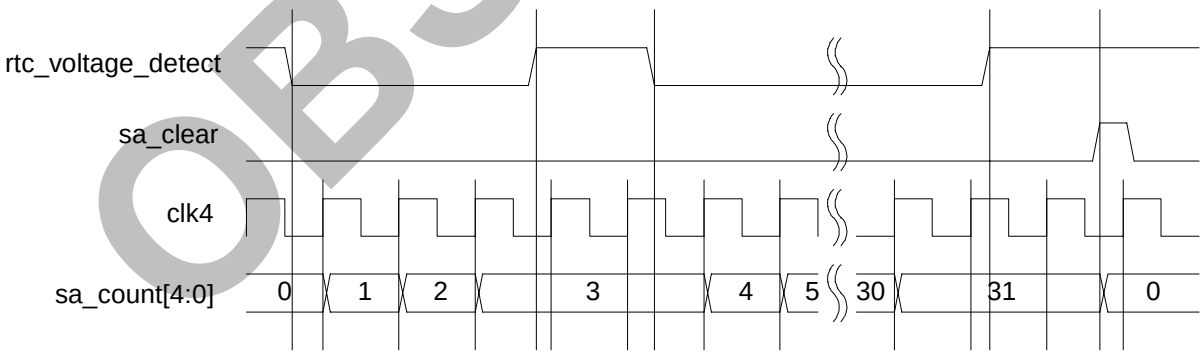


Figure 18. Stay-Alive Timer operation timing

2.11 REGISTERS

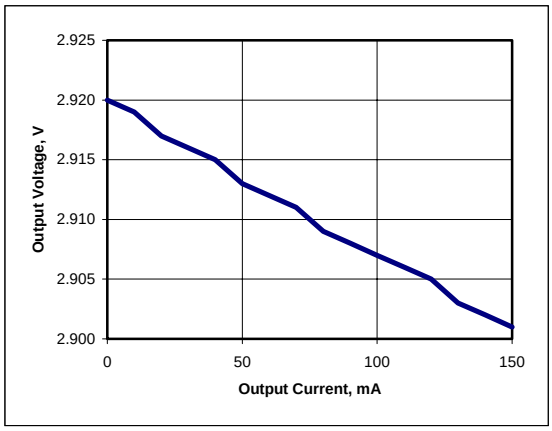
ADDR	Description	D7	D6	D5	D4	D3	D2	D1	D0	Comment
00h	Sec. Counter			S5	S4	S3	S2	S1	S0	Note 1,5
01h	Min. Counter			M5	M4	M3	M2	M1	M0	Note 1,5
02h	Hour Counter				H4	H3	H2	H1	H0	Note 1,5
03h	Week Counter						W2	W1	W0	Note 1,5
04h	Day Counter				D4	D3	D2	D1	D0	Note 1,5
05h	Month Counter					MO3	MO2	MO1	MO0	Note 1,5
06h	Year Counter		Y6	Y5	Y4	Y3	Y2	Y1	Y0	Note 1,5
07h	Alarm_A Min Register			AM5	AM4	AM3	AM2	AM1	AM0	Note 5
08h	Alarm_A Hour Register				AH4	AH3	AH2	AH1	AH0	Note 5
09h	Alarm_A Week Register		AW6	AW5	AW4	AW3	AW2	AW1	AW0	Note 5
0Ah	Alarm_B Min Register			BM5	BM4	BM3	BM2	BM1	BM0	Note 5
0Bh	Alarm_B Hour Register				BH4	BH3	BH2	BH1	BH0	Note 5
0Ch	Alarm_B Week Register (Option)		BW6	BW5	BW4	BW3	BW2	BW1	BW0	Note 5
0Dh	Alarm Control					ALA_EN	Aout	ALB_EN	Bout	Note 5
0Eh	Periodic Interrupt Control					CTFG	CT2	CT1	CT0	Note 5
0Fh	Stay-Alive Timer Control			CLR	SA4	SA3	SA2	SA1	SA0	Note 5
10h	Charger Control							CHI	CHEN	Note 4
11h	Charger MVBAT Control							REF0	MVEN	Note 4
12h	Charger MVBAT		CHV1	CHV0	MV4	MV3	MV2	MV1	MV0	Note 4
13h	LDO Control 1						LDO11	LDO5	LDO4	Note 4
14h	Not available									Note 7
15h	LDO Control 2					LDO10	LDO9	LDO8	LDO7	Note 4
16h	LDO Control 3								ALLOFF	Note 4
17h	LDO2 Gain					G23	G22	G21	G20	Note 4
18h	Keypad Column/B-light Register				BL	KO3	KO2	KO1	KO0	Note 6
19h	Keypad Row			KI5	KI4	KI3	KI2	KI1	KI0	Note 6
1Ah	GPIO Control Register					GPC3	GPC2	GPC1	GPC0	Note 6
1Bh	GPIO MASK					GPMSK3	GPMSK2	GPMSK1	GPMSK0	Note 6
1Ch	GPIO Register					GPI3 GPO3	GPI2 GPO2	GPI1 GPO1	GPI0 GPO0	Note 6
1Dh	GPIO INT					GPINT3 GPRST3	GPINT2 GPRST2	GPINT1 GPRST1	GPINT0 GPRST0	Note 2,6
1Eh	INT Register	INT7 IRST7	INT6 IRST6	INT5	INT4	INT3 IRST3	INT2 IRST2	INT1 IRST1	INT0 IRST0	Note 2,6
1Fh	INT MASK	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	Note 6
20h	DATA IN		DI6	DI5	DI4	DI3	DI2	DI1	DI0	Note 6
21h	Power OFF								PWROFF	Note 6
3Fh	TEST register (option)						LDOENB	USENB	TEST	Note 3,5

Notes:

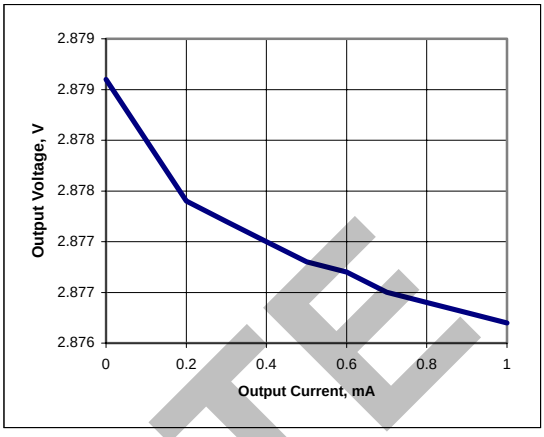
1. For the RTC counter data protection, the access should be waited for certain time (62µS) period after CS signal assertion. (Refer to RTC counter section for the wait time).
2. The INT reset operation will be valid at 62µS or later after its setting.
3. This is a set register for internal test, and should not be accessed at normal operation.
4. Analog block control registers. They control LDO etc. They are powered by VBAT.
5. Registers regarding RTC counter. They are powered by RTCV.
6. Registers for INT, GPIO, KEYPAD I/F etc. They are powered by VBAT.
7. Not available.

Typical Performance Characteristics

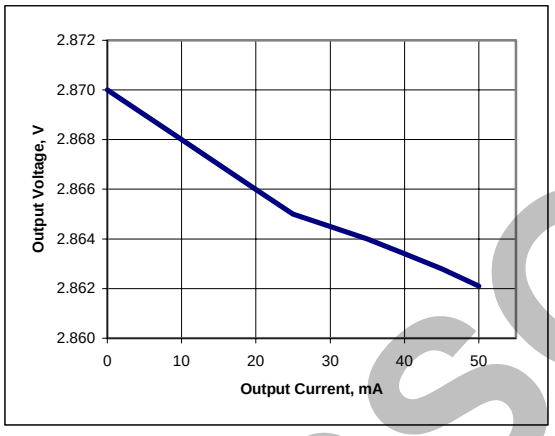
(Vin = 4.2 V, TA = 25 C)



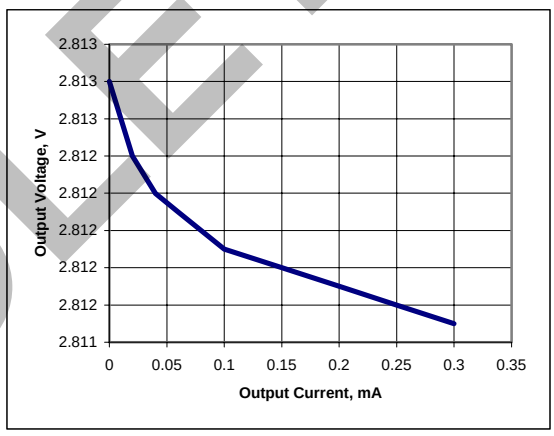
TPC1, LDO1a load regulation



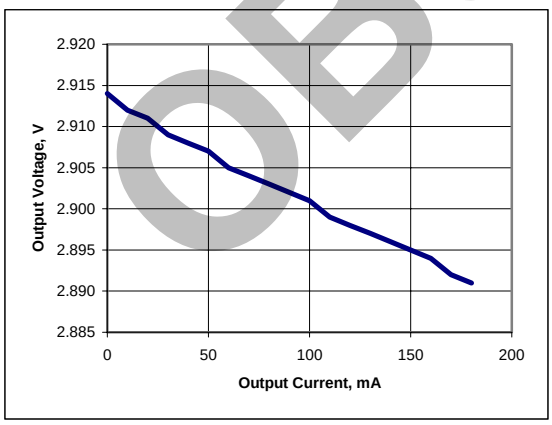
TPC2, LDO1b load regulation



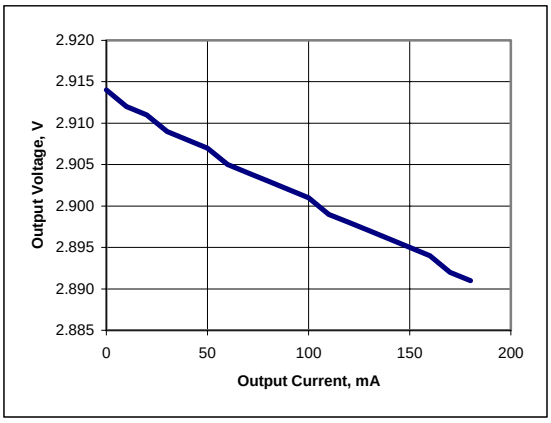
TPC3, LDO6a load regulation



TPC4, LDO6b load regulation



TPC5, LDO4 load regulation



TPC6, LDO7 load regulation

PACKAGE DIMENSION

ST-64A
64-Lead Thin Plastic Quad Flatpack [LQFP]
7 X 7mm Body, 1.4mm Thick