

## FEATURES

### Analog I/O

#### 6-channel, 12-bit SAR ADC

Single-ended and differential inputs

Programmable data rate of up to 167 kSPS

On-chip voltage reference

Supply range: 2.2 V to 3.6 V

#### Power consumption

280 nA in power-down mode, nonretained state

1.9  $\mu$ A in power-down mode, processor memory and transceiver memory retained

210  $\mu$ A/MHz, Cortex-M3 in active mode

12.8 mA transceiver in receive mode, Cortex-M3 in power-down mode

9 mA to 32 mA transceiver in transmit mode, Cortex-M3 in power-down mode

### RF transceiver

#### Frequency bands

862 MHz to 928 MHz

431 MHz to 464 MHz

#### Multiple configurations supported

Receiver sensitivity, bit error rate (BER)

–107.5 dBm at 38.4 kbps, 2FSK

Single-ended and differential power amplifier (PA)

Low external bill of materials (BOM)

### Microcontroller

32-bit ARM Cortex-M3 processor

Serial wire download and debug

External watch crystal for wake-up timer

16 MHz internal oscillator with 8-way, programmable divider

### Memory

128 kB Flash/EE memory, 16 kB SRAM

10,000-cycle Flash/EE endurance

10-year Flash/EE retention

In-circuit download via serial wire and UART

### On-chip peripherals

UART, I<sup>2</sup>C, and SPI serial I/O

28-pin GPIO port

2 general-purpose, 16-bit timers

32-bit wake-up timer

16-bit watchdog timer

8-channel pulse-width modulation (PWM)

### Package

64-lead, 9 mm  $\times$  9 mm LFCSP

Temperature range: –40°C to +85°C

### Tools

Low cost development system

Third-party compiler and emulator tool support

## APPLICATIONS

Battery-powered wireless sensors

Medical telemetry systems

Industrial and home automation

Asset tracking

Security systems (access systems)

Health and fitness applications

For more information, email [ADuCRF101@analog.com](mailto:ADuCRF101@analog.com).

## FUNCTIONAL BLOCK DIAGRAM

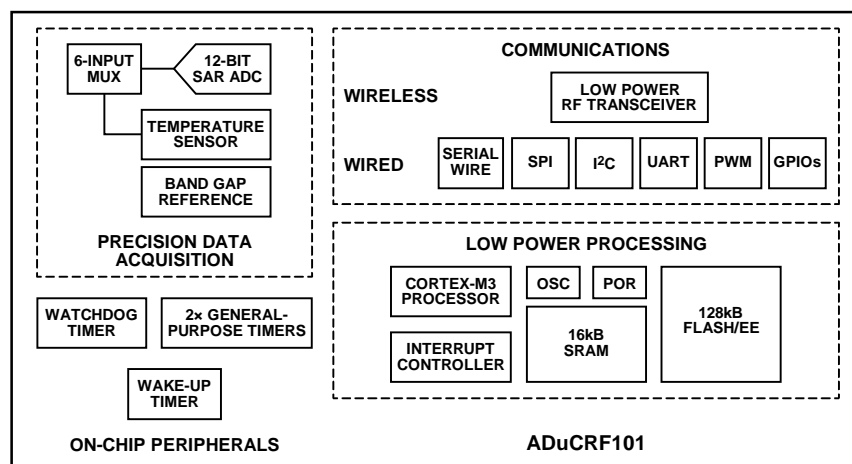


Figure 1.

Rev. Sp0

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**NOTES**

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).