REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. - ro	12-08-01	C. SAFFLE

REV																				
SHEET																				
REV	A	A	A	A	A	A														
SHEET	15	16	17	18	19	20														

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
10-02-17

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, RADIATION HARDENED, DIFFERENTIAL AMPLIFIER, MONOLITHIC SILICON

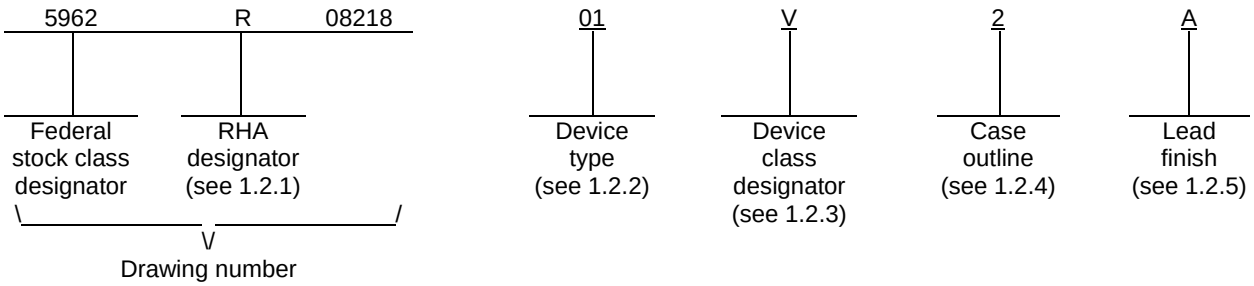
SIZE	CAGE CODE	
A	**67268**	**5962-08218**

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	AD8351	Radiation hardened differential amplifier
02 1/	AD8351	Radiation hardened differential amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Meets the performance requirements of Table I as long as section 6.7 is followed.

1.3 Absolute maximum ratings. 2/

Positive supply voltage (VPOS) ..... 6 V
Power up voltage (PWUP) ..... VPOS
Internal power dissipation (P_D) ..... 320 mW
Maximum junction temperature (T_J) ..... +175°C
Operating temperature range (T_A) ..... -55°C to +125°C
Storage temperature range ..... -65°C to +150°C
Lead temperature range (soldering, 60 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 97°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 110°C/W 4/

1.4 Recommended operating conditions.

Positive supply voltage (VPOS) ..... 3 V to 5.5 V
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1.4.1 Operating performance characteristics. 5/

Input resistance (R_{IN}) ..... 5 kΩ
Input capacitance (C_{IN}) ..... 0.8 pF
Output resistance (R_{OUT}) ..... 150 Ω
Output capacitance (C_{OUT}) ..... 0.8 pF
Slew rate (SR) ..... 13000 V / µs
Second harmonic distortion (R_L = 150 Ω, f = 10 MHz) ..... -80 dBc
Third harmonic distortion (R_L = 150 Ω, f = 10 MHz) ..... -61 dBc
Third order intermodulation distortion (IMD) (R_L = 150 Ω, f1 = 9.5 MHz, f2 = 10.5 MHz) ..... -68 dBc
Noise spectral density (RTI) (f = 10 MHz) ..... 2.65 nV/$\sqrt{Hz}$
Second harmonic distortion (R_L = 150 Ω, f = 70 MHz) ..... -62 dBc
Third harmonic distortion (R_L = 150 Ω, f = 70 MHz) ..... -66 dBc
Third order intermodulation distortion (IMD) (R_L = 150 Ω, f1 = 69.5 MHz, f2 = 70.5 MHz) ..... -64 dBc
Noise spectral density (RTI) (f = 70 MHz) ..... 2.7 nV/$\sqrt{Hz}$
Second harmonic distortion (R_L = 150 Ω, f = 140 MHz) ..... -51 dBc
Third harmonic distortion (R_L = 150 Ω, f = 140 MHz) ..... -52 dBc
Third order intermodulation distortion (IMD) (R_L = 150 Ω, f1 = 139.5 MHz, f2 = 140.5 MHz) ..... -64 dBc
Noise spectral density (RTI) (f = 140 MHz) ..... 2.75 nV/$\sqrt{Hz}$
Second harmonic distortion (R_L = 150 Ω, f = 240 MHz) ..... -38 dBc
Third harmonic distortion (R_L = 150 Ω, f = 240 MHz) ..... -49 dBc
Third order intermodulation distortion (IMD) (R_L = 150 Ω, f1 = 239.5 MHz, f2 = 240.5 MHz) ..... -61 dBc
Noise spectral density (RTI) (f = 240 MHz) ..... 2.9 nV/$\sqrt{Hz}$

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Measurement taken under absolute worst case conditions. Data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package thermal numbers.
4/ Measurement taken under absolute worst case conditions. Data taken with a thermal camera for highest power density location.
5/ Unless otherwise specified, VPOS = 5 V, PWUP = VPOS, load resistance (R_L) = 1 kΩ, gain resistance (R_G) = 200 Ω, gain (A_V) = 10 dB, f = 70 MHz, and T_A = +25°C.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device type 01 ..... 100 krads(Si) 6/
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s):
Device type 02 ..... 50 krads(Si) 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

6/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.
7/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883 method 1019, condition D.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 49 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ 6/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input / output characteristics section								
Input common mode voltage adjustment range	V_{ICMR}			1,2,3	01, 02	1.1	3.9	V
			M,D,P,L,R	1	01	1.1	3.9	
			M,D,P,L	1	02	1.1	3.9	
Maximum output voltage swing	$\pm V_{OUT}$	1 dB compressed		4,6	01, 02	4.5		V_{PP}
				5		4		
Output common mode offset voltage	$V_{OS}CM$			1,2,3	01, 02		150	mV
			M,D,P,L,R	1	01		150	
			M,D,P,L	1	02		150	
Output common mode offset drift	$V_{OS}CM$ drift	7/		2,3	01, 02		0.5	mV/°C
Output differential offset voltage	$V_{OS}DIFF$			1,2,3	01, 02		100	mV
			M,D,P,L,R	1	01		100	
			M,D,P,L	1	02		100	
Output differential offset drift	$V_{OS}DIFF$ drift	7/		2,3	01, 02		0.3	mV/°C
Input bias current	I_{IB}			1,2,3	01, 02		20	µA
			M,D,P,L,R	1	01		20	
			M,D,P,L	1	02		20	
Common mode rejection ratio	CMRR	V_{IN} = 2.8 V and 0.7 V		1,2,3	01, 02	35		dB
			M,D,P,L,R	1	01	35		
			M,D,P,L	1	02	35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ 6/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power interface section.								
Power up threshold voltage PWUP	V_{IH}			1,2,3	01, 02	1.5	VPOS	V
			M,D,P,L,R	1	01	1.5	VPOS	
			M,D,P,L	1	02	1.5	VPOS	
	V_{IL}			1,2,3	01, 02	0	0.8	
			M,D,P,L,R	1	01	0	0.8	
			M,D,P,L	1	02	0	0.8	
Power up input bias current	I_{IH}	PWUP at 5 V		1,2,3	01, 02		120	µA
			M,D,P,L,R	1	01		120	
			M,D,P,L	1	02		120	
	I_{IL}	PWUP at 0V		1,2,3	01, 02	-30		
			M,D,P,L,R	1	01	-40		
			M,D,P,L	1	02	-40		
Quiescent current	I_Q	VPOS = 5.5 V, 5 V, 3 V		1,3	01, 02		33	mA
				2			44	
			M,D,P,L,R	1	01		33	
			M,D,P,L	1	02		33	
	I_{QZ}	PWUP at 0 V		1,2,3	01, 02		6	
			M,D,P,L,R	1	01		6	
			M,D,P,L	1	02		6	
Dynamic performance section								
-3 dB bandwidth	BW	GAIN = 6 dB, 7/ 8/ $V_{OUT} \le 1.0\ V_{PP}$		4,5,6	01, 02	450		MHz
		GAIN = 12 dB, 7/ 8/ $V_{OUT} \le 1.0\ V_{PP}$				290		
		GAIN = 18 dB, 7/ 8/ $V_{OUT} \le 1.0\ V_{PP}$				210		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ 6/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance section – continued.							
Gain flatness	GF	GAIN = 10 dB, 8/ $f \le 200$ MHz, $V_{OUT} \le 1.0\ V_{PP}$	4,5,6	01, 02		0.6	dB
		GAIN = 10 dB, 7/ 8/ $f \le 400$ MHz, $V_{OUT} \le 1.0\ V_{PP}$				1	
		GAIN = 6 dB, 7/ 8/ $f \le 200$ MHz, $V_{OUT} \le 1.0\ V_{PP}$				0.26	
		GAIN = 6 dB, 7/ 8/ $f \le 300$ MHz, $V_{OUT} \le 1.0\ V_{PP}$				0.6	
		GAIN = 12 dB, 7/ 8/ $f \le 75$ MHz, $V_{OUT} \le 1.0\ V_{PP}$				0.26	
		GAIN = 12 dB, 7/ 8/ $f \le 140$ MHz, $V_{OUT} \le 1.0\ V_{PP}$				0.8	
		GAIN = 18 dB, 7/ 8/ $f \le 60$ MHz, $V_{OUT} \le 1.0\ V_{PP}$				0.26	
		GAIN = 18 dB, 7/ 8/ $f \le 100$ MHz, $V_{OUT} \le 1.0\ V_{PP}$				0.8	
Gain accuracy	A_V	R_G ±1 % tolerance, 8/ GAIN = 10 dB, VPOS = 5.5 V, 5 V, 3.3 V	4,5,6	01, 02	-1.1	+1.1	dB
		R_G ±1 % tolerance, 7/ 8/ GAIN = 6 dB, 12 dB, 18 dB	4,5,6		-1.5	+1.5	
Gain supply sensitivity	A_{VSS}	VPOS = 5 V to 5.25 V, 8/ VPOS = 5 V to 4.75 V	4,5,6	01, 02		0.26	dB / V
Gain temperature sensitivity	A_{VTS}	7/ 8/	4,5,6	01, 02		5	mdB/°C
Settling time	t_S	1 V step to 1 %, 7/ 8/ see 4.4.1c	9,10,11	01, 02		7.5	ns
Overdrive recovery time	t_{OR}	V_{IN} = 4 V to 0 V step, 7/ 8/ $V_{OUT} \le \pm 10$ mV, see 4.4.1c	9,10,11	01, 02		3.8	ns
Reverse isolation	S12	7/ 8/	4,5,6	01, 02		-67	dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ 6/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Noise / distortion section.		10 MHz characteristics					
Second harmonic distortion	HD2	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4,5	01, 02		-89	dBc
			6			-82	
Third harmonic distortion	HD3	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4	01, 02		-83	dBc
			5			-82	
			6			-88	
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 9.5 MHz, f2 = 10.5 MHz, 7/ 8/ V_{OUT} = 2 V_{PP} composite	4	01, 02		-88	dBc
			5			-85	
			6			-86	
Output third order intercept	OIP3	f1 = 9.5 MHz, 7/ 8/ f2 = 10.5 MHz,	4	01, 02		33	dBm
1 dB compression point	1 dB COMPR	8/ 9/	4,6	01, 02	8		dBm
			5		6.4		
Noise / distortion section.		70 MHz characteristics					
Second harmonic distortion	HD2	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4	01, 02		-76	dBc
			5			-80	
			6			-70	
Third harmonic distortion	HD3	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4,5	01, 02		-74	dBc
			6			-78	
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 69.5 MHz, f2 = 70.5 MHz, 7/ 8/ V_{OUT} = 2 V_{PP} composite	4	01, 02		-86	dBc
			5			-80	
			6			-83	
Output third order intercept	OIP3	f1 = 69.5 MHz, 7/ 8/ f2 = 70.5 MHz,	4,5,6	01, 02		30	dBm
1 dB compression point	1 dB COMPR	8/ 9/	4,6	01, 02	8		dBm
			5		7		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ 5/ 6/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Noise / distortion section.		140 MHz characteristics					
Second harmonic distortion	HD2	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4	01, 02		-63	dBc
			5			-76	
			6			-55	
Third harmonic distortion	HD3	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4	01, 02		-72	dBc
			5,6			-69	
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 139.5 MHz, f2 = 140.5 MHz, 7/ 8/ V_{OUT} = 2 V_{PP} composite	4	01, 02		-76	dBc
			5			-73	
			6			-68	
Output third order intercept	OIP3	f1 = 139.5 MHz, 7/ 8/ f2 = 140.5 MHz,	4,5,6	01, 02		26	dBm
1 dB compression point	1 dB COMPR	7/ 8/ 9/	4	01, 02	7.5		dBm
			5		5.5		
			6		8		
Noise / distortion section.		240 MHz characteristics					
Second harmonic distortion	HD2	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4	01, 02		-52	dBc
			5			-62	
			6			-43	
Third harmonic distortion	HD3	R_L = 1 kΩ, 7/ 8/ V_{OUT} = 2 V_{PP}	4,5	01, 02		-67	dBc
			6			-59	
Third order intermodulation distortion	IMD	R_L = 1 kΩ, f1 = 239.5 MHz, f2 = 240.5 MHz, 7/ 8/ V_{OUT} = 2 V_{PP} composite	4	01, 02		-76	dBc
			5			-73	
			6			-68	
Output third order intercept	OIP3	f1 = 239.5 MHz, 7/ 8/ f2 = 240.5 MHz	4,5,6	01, 02		19	dBm
1 dB compression point	1 dB COMPR	7/ 8/ 9/	4	01, 02	7.2		dBm
			5		5.7		
			6		7.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Device type 01 supplied to this drawing has been characterized through all levels P, L, and R of irradiation. Device type 02 supplied to this drawing has been characterized through levels P and L of irradiation. However, device type 01, is only tested at the “R” level and device type 02 is only tested at the ”L” level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A for device type 01 and condition D for device type 02. Device type 02 is tested at low dose rate.

3/ Unless otherwise specified, VPOS = 5 V, PWUP = VPOS, load resistance (R_L) = 150 Ω, gain resistance (R_G) = 100 Ω, gain (A_V) = 10 dB, and f = 70 MHz.

4/ Values are specified differentially.

5/ For optimal AC performance and stability, 25 Ω parasitic suppression resistors should be added to the input pins and a RC low pass filter on the output pins where R = 25 Ω and C = 5 pF (see section 6.7).

6/ This device is recommended for driving a differential load only. For single ended to differential applications, a balun transformer must be incorporated on the inputs to provide a differential signal to the amplifier (see section 6.7).

7/ Parameter is guaranteed by engineering characterization, not production tested. Characterization repeated after major design or process changes.

8/ Parameter not tested postirradiation.

9/ 1 dB compression point is measurement of maximum input range.

Device types	01, 02
Case outline	2
Terminal number	Terminal symbol
1	NC
2	PWUP
3	NC
4	NC
5	RGP1
6	INHI
7	INLO
8	RGP2
9	NC
10	NC
11	NC
12	NC
13	NC
14	COM
15	OPLO
16	OPHI
17	VPOS
18	NC
19	NC
20	VOCM

FIGURE 1. Terminal connections.

Terminal symbol	Type	Pin description
NC	No connect	No connection.
PWUP	Digital input	Apply a positive voltage ($1.3 \leq V_{PWUP} \leq$ +VPOS) to activate device.
RGP1	Analog output	Gain resistor input 1.
INHI	Analog input	Balanced differential input. Biased to mid supply, normally ac coupled.
INLO	Analog input	Balanced differential input. Biased to mid supply, normally ac coupled.
RGP2	Digital input	Gain resistor input 2.
COMM	Power	Device common. Connect to low impedance ground.
OPLO	Analog output	Balanced differential output. Biased to VOCM, normally ac coupled.
OPHI	Analog output	Balanced differential output. Biased to VOCM, normally ac coupled.
VPOS	Power	Positive supply voltage. 3 V to 5.5 V
VOCM	Analog I/O	Voltage applied to this pin sets the common mode voltage at both the input and output. Normally decoupled to ground with a 0.1 μF capacitor.

FIGURE 1. Terminal connections – continued.

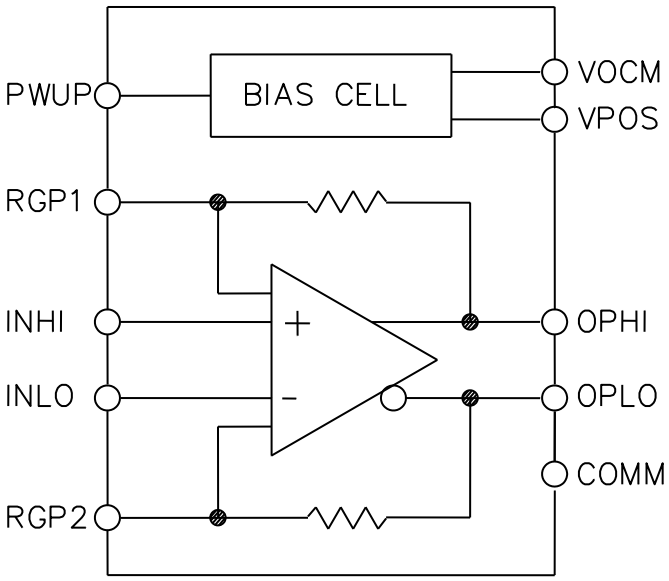


FIGURE 2. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 5, 6, 9, 10, and 11 are tested as part of device initial characterization and after design and process changes or with subsequent wafer lots as indicated in Table I.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3,4,5,6 1/	1,2,3, 1/ 2/ 3/ 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6 3/
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1 ,2,3 2/
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table I).
3/ See Table I for parameters tested or characterized for subgroups 4, 5, and 6.

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/

Parameters	Symbol	Delta limits		Units
		Min	Max	
Quiescent current, VPOS = 5 V	I_Q	-3	+3	mA
Output common mode offset voltage	$V_{OS}CM$	-20	+20	mV
Output differential offset voltage	$V_{OS}DIFF$	-19	+19	mV
Input bias current	I_{IB}	-0.2	+0.2	μA

1/ 240 hour burn in and group C end point electrical parameters. Deltas are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B . The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and condition D for device type 02 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

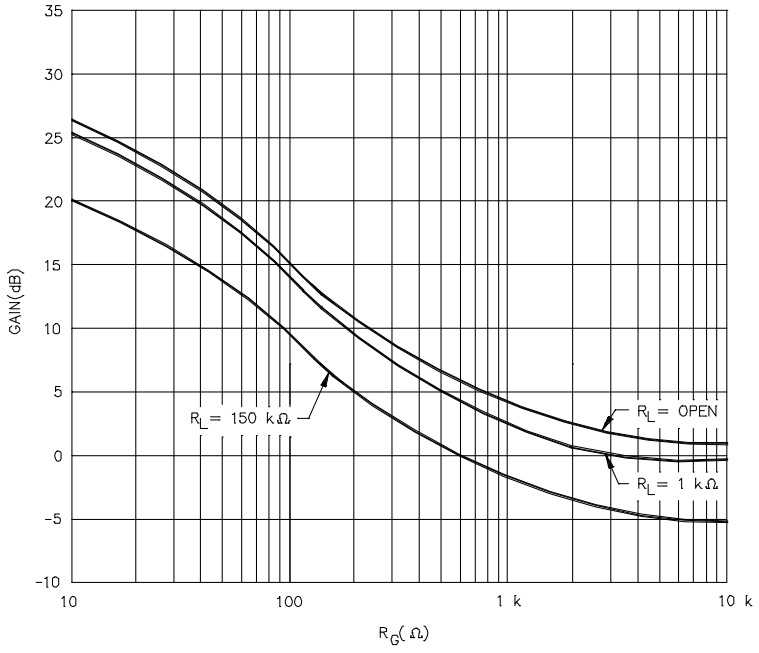
6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Application notes. The differential gain of the device is set using a single external resistor, R_G, which is connected between pins 2 and 5. The gain can be set to any value between 0 dB and 26 dB using the resistor values specified in figure 3, with common gain values provided in the corresponding table.



R_L = 1kΩ	
GAIN, Av	RG
0	2000
6	422
10	200
12	143
18	52
20	35

FIGURE 3. Gain versus gain resistor (RG). (R_L = 150 Ω, 1 kΩ, and open)

6.7 Application notes - continued.

The device can demonstrate sensitivity to parasitic capacitance on the gain resistor (R_G) pins. The sensitivity may be observed as an oscillation on the output if proper layout techniques are not observed. Layout is critical to the performance of the part because excessive parasitic capacitance on the inputs, outputs, and especially on the R_G pin traces could cause oscillations. Therefore it is recommended that the following layout guidelines be followed to minimize stray capacitance on the printed circuit board.

Ensure that all I/O, ground, and RG traces are kept as short as possible.
The output single-ended source impedance of the device is dynamically set to a nominal value of 75Ω. Therefore, for a matched load termination, the characteristic impedance of the output transmission lines should be designed to be 75 Ω. In many situations, the final load impedance may be relatively high, greater than 1 kΩ. It is recommended that the board be designed as shown in figure 4 for high impedance load conditions.
The printed-circuit board traces should be dimensioned to a small width (~5 mils).
Remove underlying ground planes near the signal traces and around package.
Keep all supporting components as close to the device as possible.
Do not tie any components to the no connect pins.

Observing the guidelines outlined above and following precautions described in the layout of figure 4 will reduce parasitic board capacitance allowing the device to achieve the specified bandwidth and decrease the potential for gain-peaking or oscillation. The R_T resistors in figure 4 are termination resistors which are used to prevent input reflections from a driving source impedance which is normally low. The footprint for the R_T, RIP, and ROP resistors in the layout of figure 4 correspond to resistors R2 and R3, R4 and R5, and R6 and R7 in schematics of figures 5 and 6 respectively.

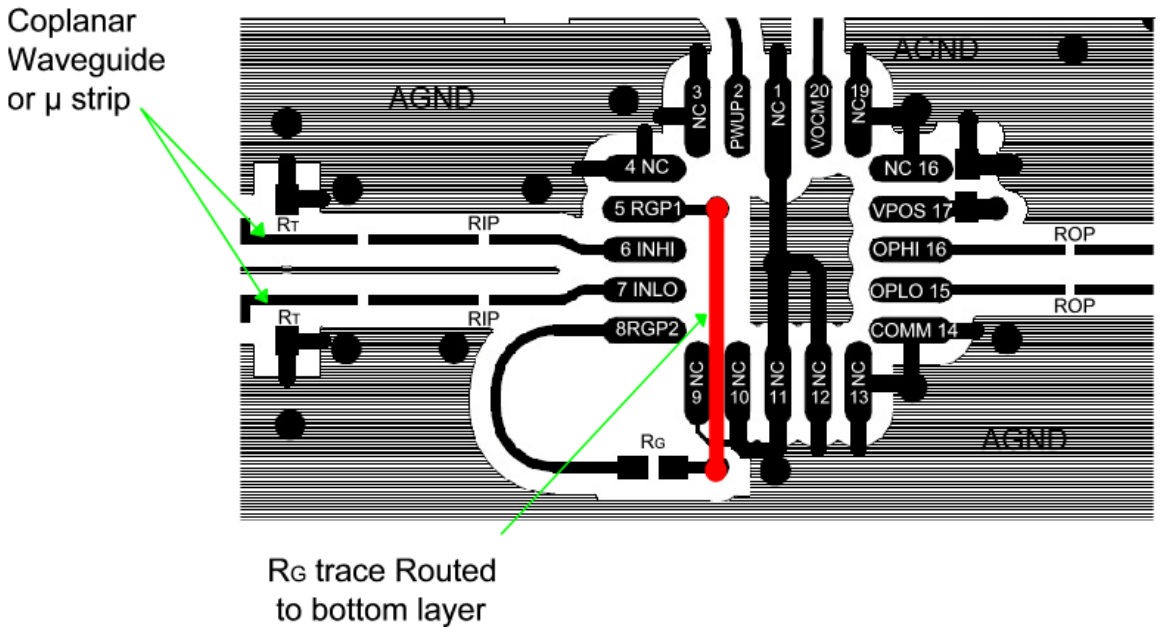


FIGURE 4. General description of recommended board layout.

6.7 Application notes - continued.

Excessive package parasitic capacitance can cause the device to become unstable and cause bandwidth degradation due to the resonant circuit ($f_O = 1 / (2\pi\sqrt{LC})$) formed from the parasitic inductance and capacitance loading. The capacitive load in parallel with the package inductance creates a resonant circuit and peaking in the gain response. Under these circumstances, a transient event may place the device in an abnormal operating state. This effect can be suppressed by adding additional load resistors for the purpose of capacitive parasitic suppression. To further optimize performance and stability, it is recommended that 25 Ω resistors are added to the input signal traces (R4 and R5 in figure 5). As well, a lowpass filter is required on the output where R6 and R7 are 25 Ω and C3 and C4 are 5 pF. The lowpass filter takes advantage of the package inductance and forms a notch filter. The notch filter desensitizes the resonant effects of the device in the gain response at higher frequencies while increasing the operating bandwidth, improving gain flatness, and providing further stability for the part.

Figure 5 is the recommended circuit for evaluating applications where the amplifier drives an ADC with a 1 kΩ load differentially. This device is not recommended for driving a single ended load. For single-ended to differential applications where the source is single-ended, a balun transformer must be incorporated on the input to provide a differential signal to the amplifier as indicated in figure 6. Grounding either input terminals for single-ended to differential applications is not recommended. The output baluns in figure 6 is for evaluation purposes only where it is required to interface the outputs of the amplifier to a single-ended test equipment. The balun transformer will balance the I/O signals and help reduce any common-mode events that may occur on these signal traces. It is important to note that if an output balun is used for evaluation purposes dynamic and distortion/noise performance cannot be guaranteed. The circuits in figures 5 and 6 are designed for interfacing with signal sources and test equipment that are terminated internally to 50 Ω. Resistors R4 and R5 are the input parasitic suppression resistors. Resistors R6 and R7 and capacitors C3 and C4 compose the RC lowpass filter. The filter values are such that 0.6 dB gain flatness up to 200 MHz and 1dB gain flatness up to 400 MHz can be maintained for A_V = 10 dB driving a 1 kΩ load at 25°C for differentially. Adjusting the filter values may degrade gain flatness, bandwidth and stability.

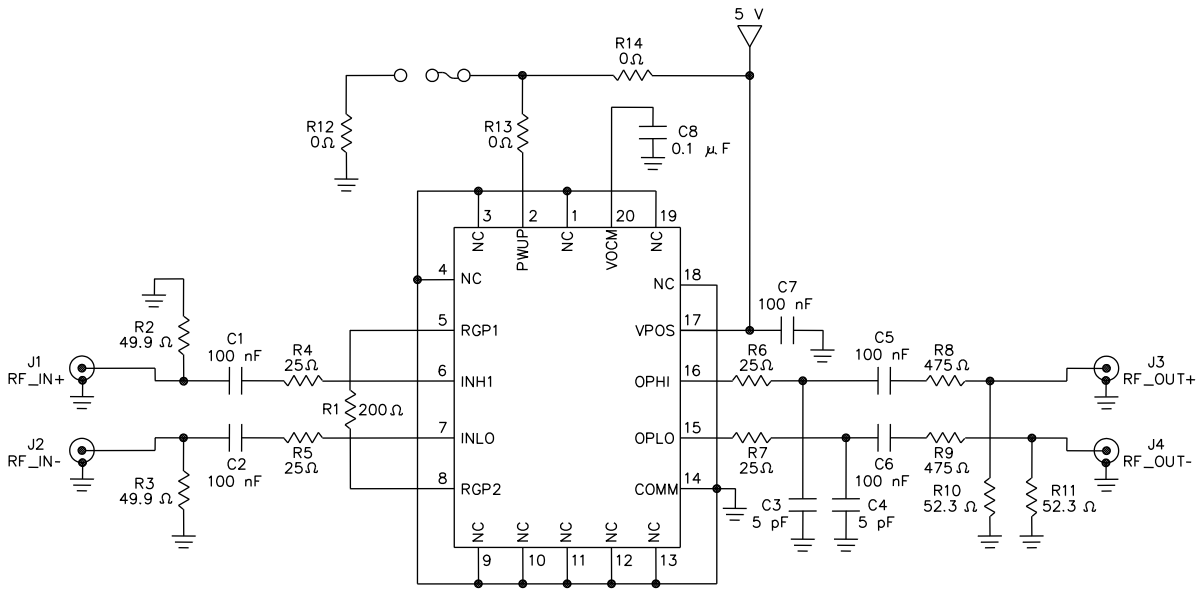


Figure 5. Recommended evaluation circuit configuration for driving a differential load.

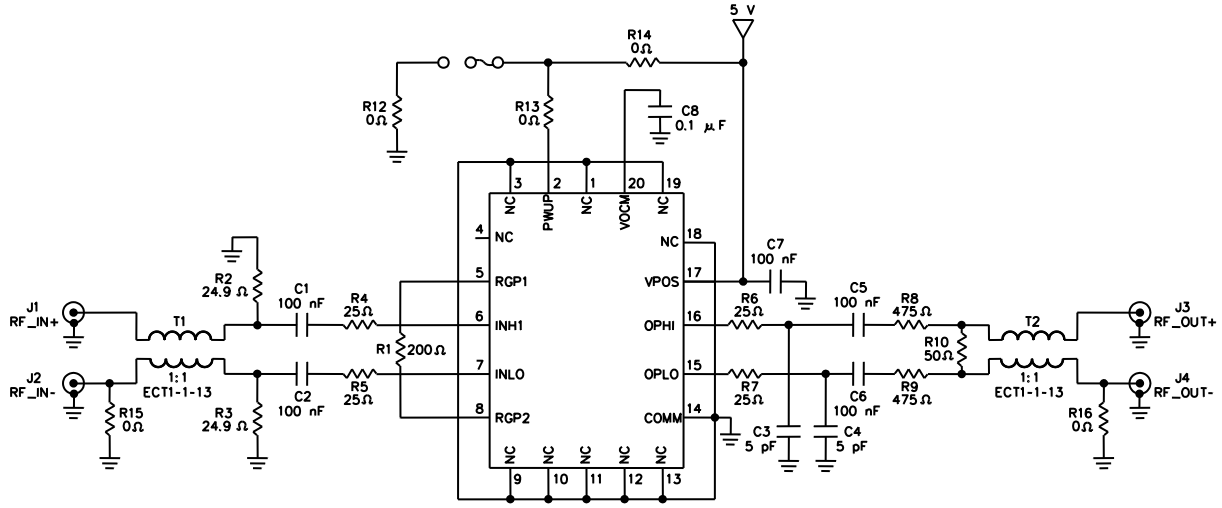


FIGURE 6. Recommended evaluation circuit configuration for single ended input to drive a differential load.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-08-01

Approved sources of supply for SMD 5962-08218 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0821801V2A	24355	AD8351ARC/QMLR
5962L0821802V2A	24355	AD8351ARC/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Greensboro, NC 27409-9605