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А	Chan	nges in a	ccorda	ance w	/ith NO	R 5962	-R213-	·92.					92-06-19		M. A. Frye					
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С	Chan	nge to the	e input	bias c	current	test an	d input	resista	ance tes	st in tab	le I. –r	rp		99-0	)8-13			Raymo	nd Mon	nin
D	Add footnote to ta			ut bias current test and input resistance test in table I. –rrp ole I. Editorial changes throughout. – drw				•		01-1	11-14				nd Mon					
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				THE	ORIGI	NAL FI	RST P/	AGE OI	F THIS	DRAW	ING H	AS BER	EN REF		D.					
SHEET				THE	ORIGI	NAL FI	RST P/		F THIS	DRAW	ING H.	AS BER	EN REF		D.					
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SHEET REV SHEET REV STATUS OF SHEETS PMIC N/A STA MICRO DR THIS DRAW	ANDAF OCIRC AWING ING IS A USE BY / ARTMEN	CUIT G VAILABI ALL ITS		REV SHE PREI	ZET PAREI CKED C	D BY Joseph BY	D 1 A. Kert	D 2 Dy Dre	D	D 4	D 5 DI	D 6 EFEN	SE SI COL http	UPPL UPPL UMBI o://ww	P 9 Y CE US, O vw.ds	NTEF HIO scc.dl	4321 a.mil SPE	6 ED 8	BIT /	A/D
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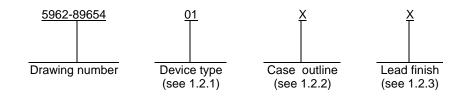
DSCC FORM 2233 APR 97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE
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1.1 <u>Scope</u>. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



# 1.2.1 <u>Device types</u>. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD9012S	8 Bit A/D
02	AD9012T	8 Bit A/D

1.2.2 <u>Case outlines</u>. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
Х	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

# 1.3 Absolute maximum ratings.

Positive supply voltage ( $V_S$ +) Negative supply voltage ( $V_S$ -) Analog input voltage Power dissipation ( $P_D$ ) ( $T_A$ = +25°C):	-6 V dc
Case outline X Case outline 3	1.8 W
Storage temperature range Lead temperature (soldering, 10 seconds) Junction temperature (T <sub>J</sub> )	+300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) Thermal resistance, junction-to-case ( $\theta_{JC}$ )	
Case outline X Case outline 3	
ENCODE input voltage OVERFLOW INH input voltage Reference input voltage (+V <sub>REF</sub> -V <sub>REF</sub> )	0 V to -5.2 V dc
	±4 mA 30 mA

<u>1</u>/ +V<sub>REF</sub>  $\geq$  -V<sub>REF</sub> under all circumstances.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89654
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		D	2

## 1.4 Recommended operating conditions.

Ambient operating temperature range (T <sub>A</sub> )	-55°C to +125°C
Positive supply voltage (V <sub>S</sub> +)	+5 V dc
Negative supply voltage (V <sub>S</sub> -)	-5.2 V dc

# 2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

# SPECIFICATION

## DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

### STANDARDS

### DEPARTMENT OF DEFENSE

MIL-STD-883	-	Test Method Standard Microcircuits.
MIL-STD-1835	-	Interface Standard Electronic Component Case Outlines.

## HANDBOOKS

# DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings. MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89654
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		D	3

# 3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 System timing diagram and load circuit. The system timing diagram and load circuit shall be as specified on figure 2.

3.2.3 <u>Case outlines</u>. The case outlines shall be in accordance with 1.2.2 herein.

3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 <u>Certification/compliance mark</u>. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 <u>Verification and review</u>. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89654
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		D	<b>4</b>

TABLE I. Electrical performance characteristics.							
Test	Symbol	$\begin{array}{l} Conditions \ \underline{1}/\\ -55^{\circ}C \leq T_A \leq +125^{\circ}C\\ unless \ otherwise \ specified \end{array}$	Group A subgroups	Device type	Li	imits	Unit
	<u>                                     </u>			<u> </u>	Min	Max	<u> </u>
Input bias current	I <sub>B</sub>	Analog input = 0 V	1, 2, 3	All	<u> </u>	200	μΑ
Input resistance	R <sub>IN</sub>		1	All	25		kΩ
Reference ladder resistance	R		1	All	40	110	Ω
Overflow inhibit 0 V input current	I <sub>IN</sub>		1, 2, 3	All		250	μΑ
High level output voltage	V <sub>OH</sub>	<u>2</u> /	1, 2, 3	All	2.4		V
Low level output voltage	V <sub>OL</sub>	<u>2</u> /	1, 2, 3	All		0.4	V
Positive supply current	+I <sub>CC</sub>	V <sub>S</sub> + = +5.0 V <u>3</u> /	1	All		45.0	mA
			2, 3	1'		48.0	1
Negative supply current	-Icc	V <sub>S</sub> - = -5.2 V <u>3</u> /	1	All		179	mA
			2, 3	1'		191	
Conversion rate	Fs		4	All	75		MSPS
Encode pulse width (low)	t <sub>PWL</sub>	<u>4</u> /	4	All	2.5		ns
Encode pulse width (high)	t <sub>PWH</sub>	<u>4</u> /	4	All	2.5		ns
Signal-to-noise ratio	SNR	<u>5</u> /	4	All	46		dB
Differential linearity	DNL		4	01		0.75	LSB
				02		0.5	1
		<u>6</u> /	5, 6	01		1.0	1
				02		0.75	1
Integral linearity	INL		4	01		1.0	LSB
	1			02		0.5	1
		<u>6</u> /	5, 6	All		1.2	1
Top of reference ladder			1	All		15	mV
			2, 3	1'		18	1
Bottom of reference ladder			4	All		10	mV
		<u>6</u> /	5, 6	1'		13	1
High level input voltage	VIH	<u>6</u> /	4, 5, 6	All	2.0		V
Low level input voltage	V <sub>IL</sub>	<u>6</u> /	4, 5, 6	All		0.8	V

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89654
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL D	SHEET 5

<u>6/</u> <u>6/</u> <u>3/, 7/</u> <u>8/</u>	4, 5, 6 4, 5, 6 4	AII AII AII	Min	Max 250 400	μA μA
<u>6</u> / <u>3</u> /, <u>7</u> /	4, 5, 6	All		400	•
<u>3</u> /, <u>7</u> /	4				μA
	-	All			
<u>8</u> /	4			2.5	mV/V
	4	All		18	pF
<u>2/, 9/, 10/</u>	9	All	4.0	11.0	ns
<u>2/, 10/</u>	9	All		8.0	ns
<u>2</u> /, <u>10</u> /	9	All		4.3	ns
Analog input signal = 1.23 MHz <u>11</u> /	4	All	48		dB
<u>1</u> / $V_{s}$ + = 5.0 V, $V_{s}$ - = -5.2 V, differential reference voltage = 2.0 V.					
i	Analog input signal = 1.23 MHz $\underline{11}$ / ial reference voltage = 2.0 V.	Analog input signal4= 1.23 MHz $\underline{11}/$ 4ial reference voltage = 2.0 V.	Analog input signal4All= 1.23 MHz11/	Analog input signal4All48= 1.23 MHz $\underline{11}/$ 4All48ial reference voltage = 2.0 V.	Analog input signal = 1.23 MHz4All48ial reference voltage = 2.0 V.

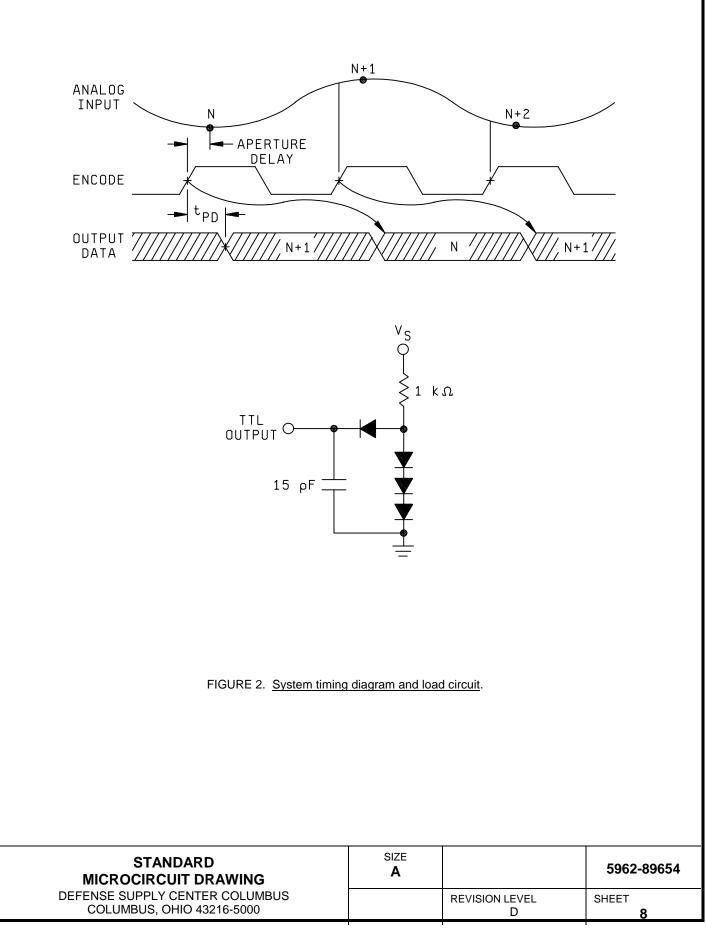
- $\underline{3}$ / Supplies should remain stable within  $\pm 5$  % for normal operation.
- <u>4</u>/ ENCODE signal rise/fall times should be less than 30 ns for normal operation.
- 5/ RMS signal to RMS noise, including harmonics with 1.23 MHz analog input signal.
- 6/ Subgroups 5 and 6 if not tested shall be guaranteed to the limits specified.
- $\underline{7}/$  Measured at -5.2 V ±5 % and +5.0 V ±5 %.
- 8/ Subgroup 4 (C<sub>IN</sub> measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
- <u>9</u>/ Measured from ENCODE into data out for LSB only.
- 10/ Guaranteed by design. Not tested.
- 11/ Measured at 75 MSPS encode rate. Harmonic data based on worst case harmonics.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89654
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		D	6

	1
Device types	01 and 02
Case outlines	X and 3
Terminal number	Terminal symbol
1	DIGITAL V <sub>S</sub> +
2	OVERFLOW INH
3	HYSTERESIS
4	+V <sub>REF</sub>
5	ANALOG INPUT
6	ANALOG GROUND
7	ENCODE
8	DIGITAL V <sub>S</sub> +
9	ANALOG GROUND
10	ANALOG INPUT
11	-V <sub>REF</sub>
12	REF mid
13	DIGITAL V <sub>S</sub> +
14	DIGITAL Vs-
15	D1 (LSB)
16	D2
17	D3
18	D4
19	D5
20	DIGITAL GROUND
21	ANALOG V <sub>S</sub> -
22	ANALOG V <sub>S</sub> -
23	DIGITAL GROUND
24	D6
25	D7
26	D8 (MSB)
27	OVERFLOW
28	DIGITAL V <sub>S</sub> -



STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89654
		REVISION LEVEL D	SHEET 7



# 4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, or C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}C$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

1	1
MIL-STD-883 test requirements	Subgroups
	(in accordance with
	MIL-STD-883, method 5005,
	table I)
Interim electrical parameters	1
(method 5004)	·
Final electrical test parameters	1*. 2. 3. 4
(method 5004)	г, 2, 0, т
Group A test requirements	1, 2, 3, 4, 5**, 6**, 9
(method 5005)	1, 2, 0, 7, 0, 0, 3
Groups C and D end-point	1
electrical parameters	
(method 5005)	

# TABLE II. Electrical test requirements.

\* PDA applies to subgroup 1.

\*\* Subgroups 5 and 6 if not tested shall be guaranteed to the limits specified in table I.

4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7, 8, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

STANDARD MICROCIRCUIT DRAWING	SIZE <b>A</b>		5962-89654
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		D	9

## 4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, or C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}C$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

# 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

# 6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractorprepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89654
		REVISION LEVEL D	SHEET 10

#### STANDARD MICROCIRCUIT DRAWING BULLETIN

## DATE: 01-11-14

Approved sources of supply for SMD 5962-89654 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-89654013A	<u>3</u> /	AD9012SE/883B
5962-8965401XA	24355	AD9012SQ/883B
5962-89654023A	<u>3</u> /	AD9012TE/883B
5962-8965402XA	24355	AD9012TQ/883B

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- <u>2</u>/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- $\underline{3}$ / Not available from an approved source.

Vendor CAGE <u>number</u>

24355

Vendor name and address

Analog Devices RT 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.