

# DATA SHEET

## **74ALVCHS162830**

18-bit to 36-bit address driver  
with bus hold (3-State)

Product data

2001 Sep 07

File under Integrated Circuits — ICL03

# 18-bit to 36-bit address driver with bus hold (3-State) 74ALVCHS162830

## FEATURES

- Output ports have equivalent 26  $\Omega$  series resistors, so no external resistors are required
- Diodes on inputs clamp overshoot
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Bus hold on data inputs eliminates the need for external pullup/pulldown resistors
- Packaged in thin very small-outline package (TVSOP) — 0.4 mm pitch
- Optimized for use with PCK953 in SDRAM module applications
- Balanced  $\pm 12$  mA output drive
- Low noise, low skew

## DESCRIPTION

The ALVCHS162830 address driver is designed for 2.3 V to 3.6 V  $V_{CC}$  operation.

Diodes to  $V_{CC}$  have been added on the inputs to clamp overshoot.

The bus hold feature retains the inputs' last state whenever the input bus goes to high impedance. This prevents floating inputs and eliminates the need for pull up or pull down resistors.

The outputs, which are designed to sink up to 12 mA, include equivalent 26  $\Omega$  series resistors to reduce overshoot and undershoot.

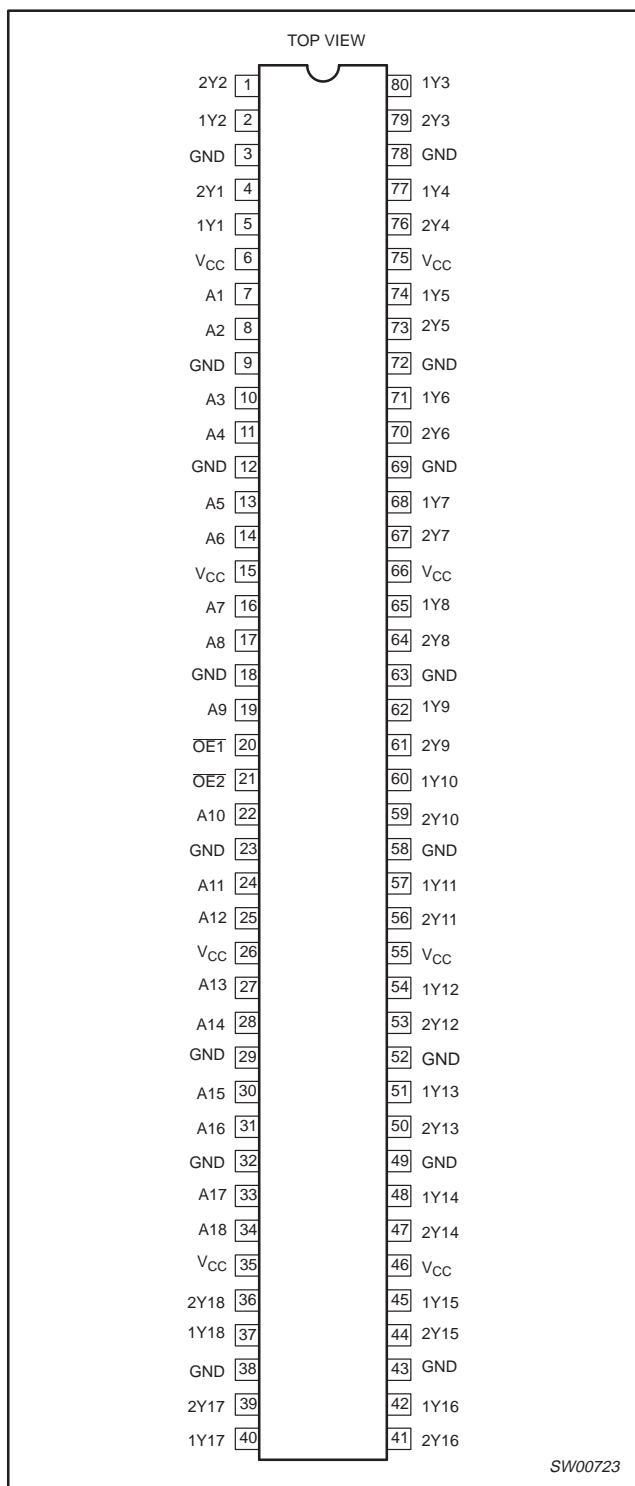
To ensure the high-impedance state during power up or power down, the output-enable (OE) input should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The 74ALVCHS162830 is characterized for operation from  $-40$  to  $+85$   $^{\circ}\text{C}$ .

## FUNCTION TABLE

Inputs			Outputs	
OE1	OE2	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

## PIN CONFIGURATION



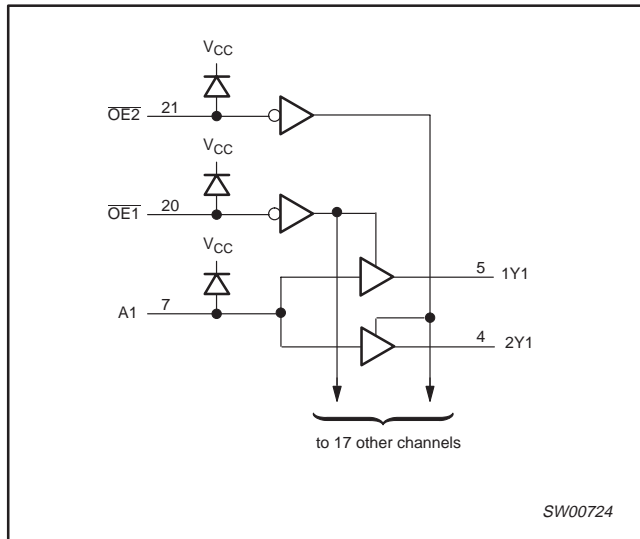
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
80-pin plastic thin very small outline (TVSOP)	$-40$ to $+85$ $^{\circ}\text{C}$	74ALVCHS162830DGB	SOT647-1

# 18-bit to 36-bit address driver with bus hold (3-State)

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## LOGIC DIAGRAM (POSITIVE LOGIC)



## PIN DESCRIPTION

PIN(S)	SYMBOL	FUNCTION
6, 15, 26, 35, 46, 55, 66, 75	V <sub>CC</sub>	Supply voltage
7, 8, 10, 11, 13, 14, 16, 17, 19, 22, 24, 25, 27, 28, 30, 31, 33, 34	A <sub>n</sub>	Inputs
1, 2, 4, 5, 36, 37, 39, 40, 41, 42, 44, 45, 47, 48, 50, 51, 53, 54, 56, 57, 59, 60, 61, 62, 64, 65, 67, 68, 70, 71, 73, 74, 76, 77, 79, 80	1Y <sub>n</sub> , 2Y <sub>n</sub>	Outputs
20, 21	OE1, OE2	Output enable
3, 9, 12, 18, 23, 29, 32, 38, 43, 49, 52, 58, 63, 69, 72, 78	GND	Ground

## ABSOLUTE MAXIMUM RATINGS

Over recommended operating free-air temperature range (unless otherwise noted).<sup>1</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	Supply voltage range		−0.5 to +4.6	V
V <sub>I</sub>	Input voltage range	See Note 2	−0.5 to +4.6	V
V <sub>O</sub>	Output voltage range	See Notes 2 and 3	−0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	−50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	−50	mA
I <sub>O</sub>	Continuous output current		± 50	mA
I <sub>CC</sub> , I <sub>GND</sub>	Continuous current through each V <sub>CC</sub> or GND		± 100	mA
Θ <sub>JA</sub>	Package thermal impedance	See Note 4	106	°C/W
T <sub>stg</sub>	Storage temperature range		−65 to +150	°C

### NOTES:

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- This value is limited to 4.6 V maximum.
- The package thermal impedance is calculated in accordance with JESD 51.

# 18-bit to 36-bit address driver with bus hold (3-State)

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## RECOMMENDED OPERATING CONDITIONS

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	Supply voltage		2.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.3 \text{ V}$		-6	mA
		$V_{CC} = 2.7 \text{ V}$		-8	
		$V_{CC} = 3 \text{ V}$		-12	
$I_{OL}$	Low-level output current	$V_{CC} = 2.3 \text{ V}$		6	mA
		$V_{CC} = 2.7 \text{ V}$		8	
		$V_{CC} = 3 \text{ V}$		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
$T_{amb}$	Operating free-air temperature		-40	+85	°C

# 18-bit to 36-bit address driver with bus hold (3-State)

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## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	$V_{CC}$	LIMITS			UNIT
				MIN	TYP <sup>1</sup>	MAX	
$V_{IK}$		$I_I = -18 \text{ mA}$	2.3 V			-1.2	V
		$I_I = 18 \text{ mA}$	2.3 V			$V_{CC}+1.2$	
$V_{OH}$		$I_{OH} = -100 \mu\text{A}$	2.3 V to 3.6 V	$V_{CC}-0.2$			V
		$I_{OH} = -4 \text{ mA}, V_{IH} = 1.7 \text{ V}$	2.3 V	1.9			
		$I_{OH} = -6 \text{ mA}$	$V_{IH} = 1.7 \text{ V}$	2.3 V	1.7		
			$V_{IH} = 2 \text{ V}$	3 V	2.4		
		$I_{OH} = -8 \text{ mA}, V_{IH} = 2 \text{ V}$	2.7 V	2			
		$I_{OH} = -12 \text{ mA}, V_{IH} = 2 \text{ V}$	3 V	2			
$V_{OL}$		$I_{OL} = 100 \mu\text{A}$	2.3 V to 3.6 V			0.2	V
		$I_{OL} = 4 \text{ mA}, V_{IL} = 0.7 \text{ V}$	2.3 V			0.4	
		$I_{OL} = 6 \text{ mA}$	$V_{IL} = 0.7 \text{ V}$	2.3 V		0.55	
			$V_{IL} = 0.8 \text{ V}$	3 V		0.55	
		$I_{OL} = 8 \text{ mA}, V_{IL} = 0.8 \text{ V}$	2.7 V			0.6	
		$I_{OL} = 12 \text{ mA}, V_{IL} = 0.8 \text{ V}$	3 V			0.8	
$I_I$		$V_I = V_{CC} \text{ or GND}$	3.6 V			$\pm 5$	$\mu\text{A}$
$I_{I(\text{hold})}$		$V_I = 0.7 \text{ V}$	2.3 V	45			$\mu\text{A}$
		$V_I = 1.7 \text{ V}$	2.3 V	-45			
		$V_I = 0.8 \text{ V}$	3 V	75			
		$V_I = 2 \text{ V}$	3 V	-75			
		$V_I = 0 \text{ to } 3.6 \text{ V}^2$	3.6 V			$\pm 500$	
$I_{OZ}$		$V_O = V_{CC} \text{ or GND}$	3.6 V			$\pm 10$	$\mu\text{A}$
$I_{CC}$		$V_I = V_{CC} \text{ or GND}, I_O = 0$	3.6 V			40	$\mu\text{A}$
$\Delta I_{CC}$		One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC} \text{ or GND}$	3 V to 3.6 V			750	$\mu\text{A}$
$C_i$	Control inputs	$V_I = V_{CC} \text{ or GND}$	3.3 V		3.5		pF
	Data inputs				7.64		
$C_o$	Outputs	$V_O = V_{CC} \text{ or GND}$	3.3 V		3.12		pF

### NOTES:

1. All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ .
2. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

# 18-bit to 36-bit address driver with bus hold (3-State)

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## SWITCHING CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	1.2	3.8		4	1.7	3.5	ns
$t_{en}$	$\overline{OE}$	Y	1	5.7		5.7	1	4.8	ns
$t_{dis}$	$\overline{OE}$	Y	1	4.9		5.4	1.7	5.2	ns
$t_{sk(o)}^1$	Output skew	–	–	–	–	–	–	500	ps

### NOTE:

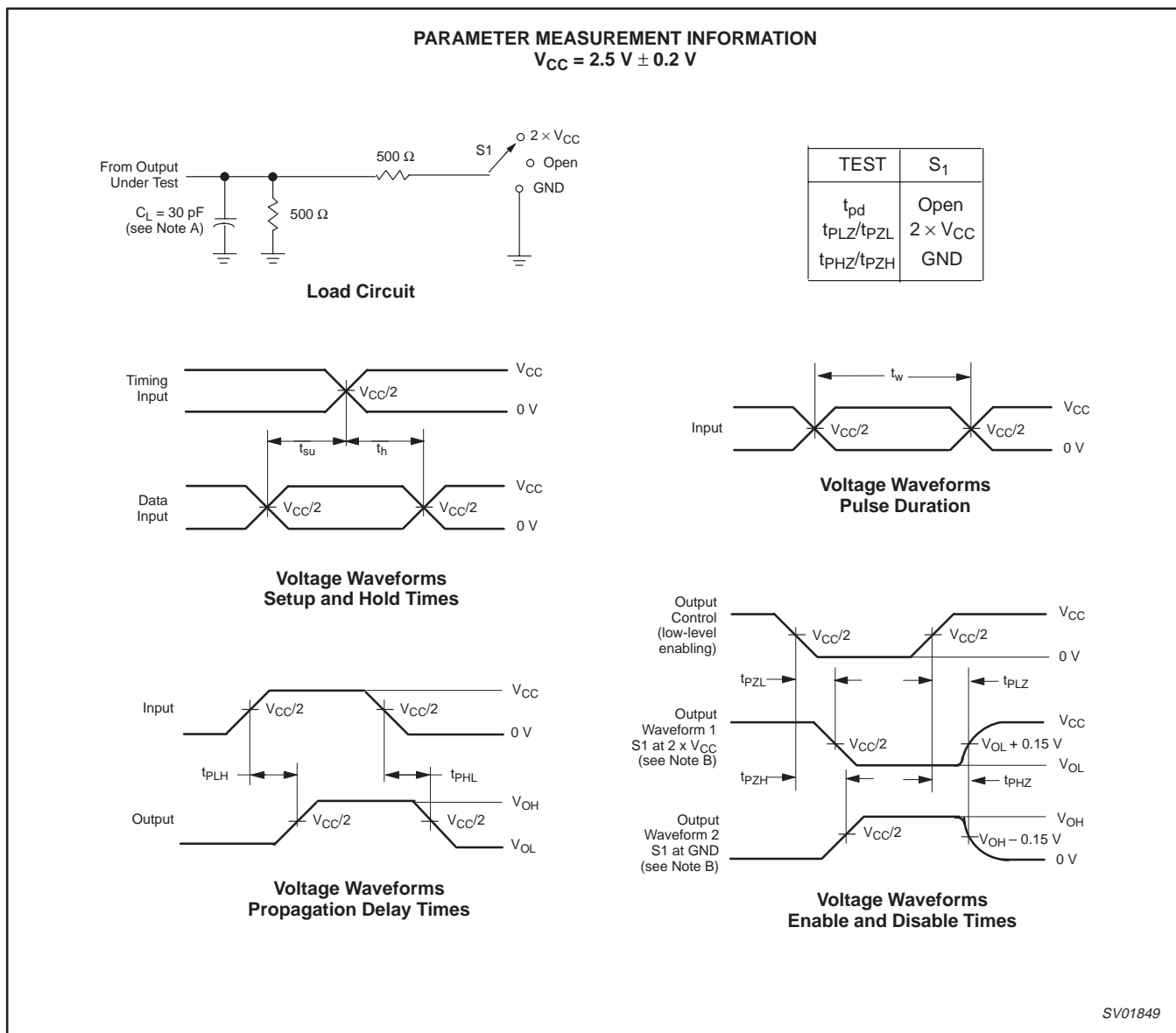
1. Output skew between any 2 outputs of same part switching in the same direction.

## OPERATING CHARACTERISTICS, $T_{amb} = 25^\circ\text{C}$

SYMBOL	PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
				TYP	TYP	
$C_{pd}$	Power dissipation capacitance per driver	All outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	49	53	pF
		All outputs disabled		6	7.5	

# 18-bit to 36-bit address driver with bus hold (3-State)

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**NOTES:**

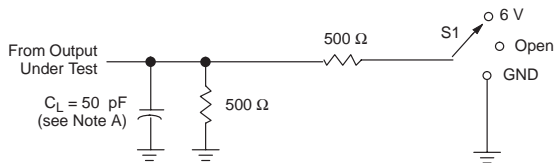
- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load circuit and voltage waveforms

# 18-bit to 36-bit address driver with bus hold (3-State)

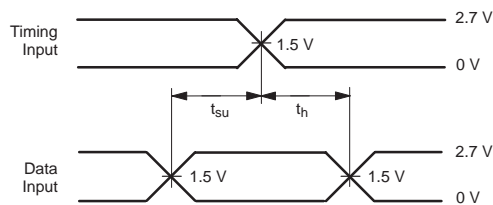
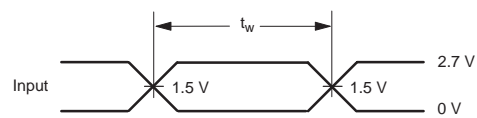
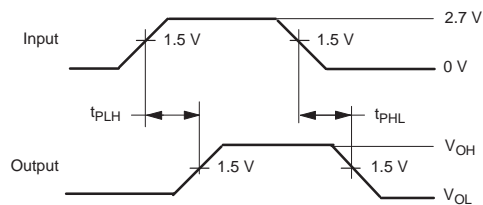
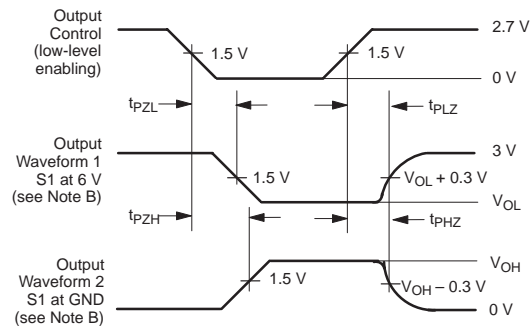
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## PARAMETER MEASUREMENT INFORMATION

 $V_{CC} = 2.7\text{ V and } 3.3\text{ V} \pm 0.3\text{ V}$ 


Load Circuit

TEST	S <sub>1</sub>
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

Voltage Waveforms  
Setup and Hold TimesVoltage Waveforms  
Pulse DurationVoltage Waveforms  
Propagation Delay TimesVoltage Waveforms  
Enable and Disable Times

SV01850

### NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- The outputs are measured one at a time with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

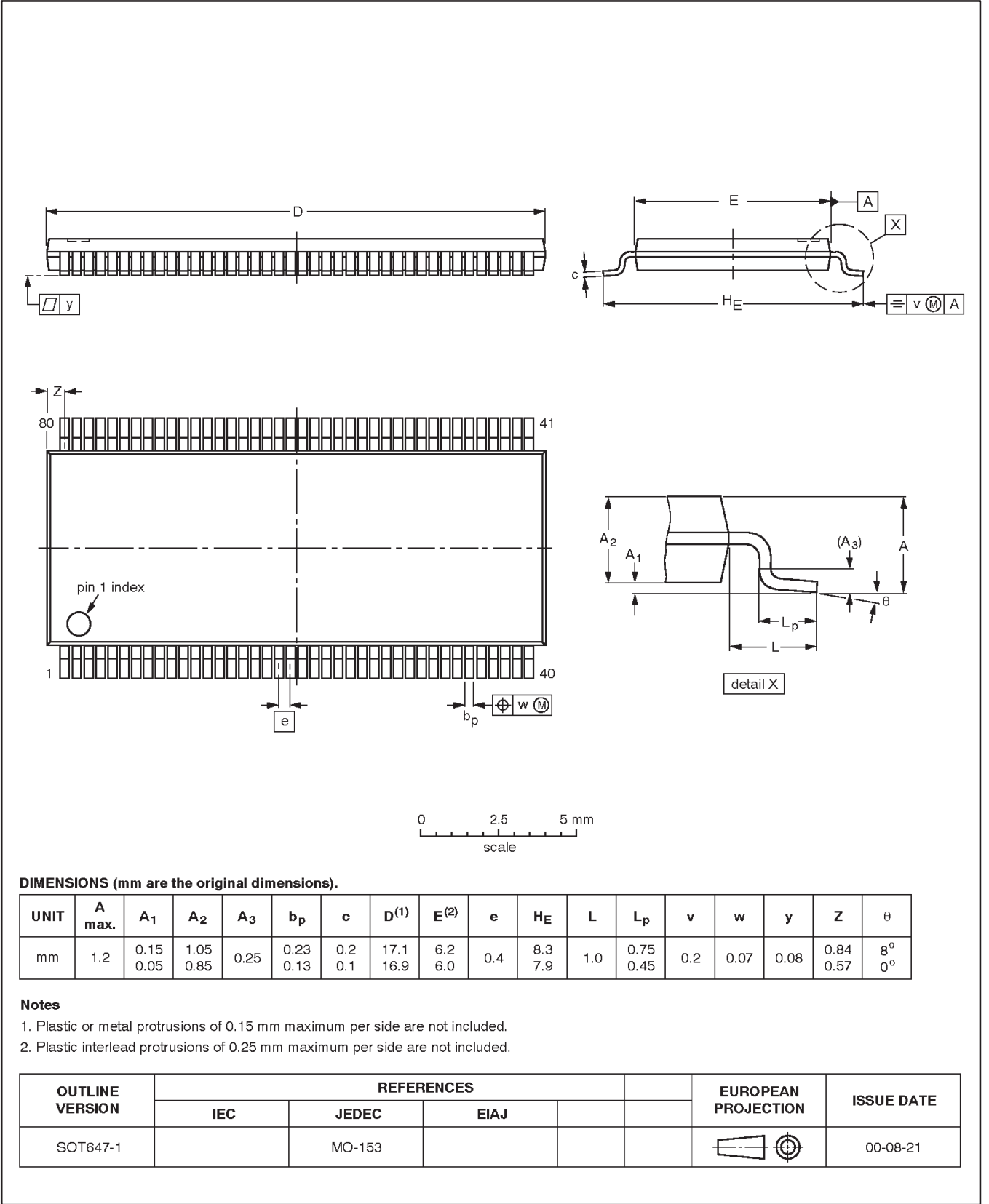
Figure 2. Load circuit and voltage waveforms

18-bit to 36-bit address driver with bus hold  
(3-State)

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TSSOP80: plastic thin shrink small outline package; 80 leads; body width 6.1 mm

SOT647-1



# 18-bit to 36-bit address driver with bus hold (3-State)

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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
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