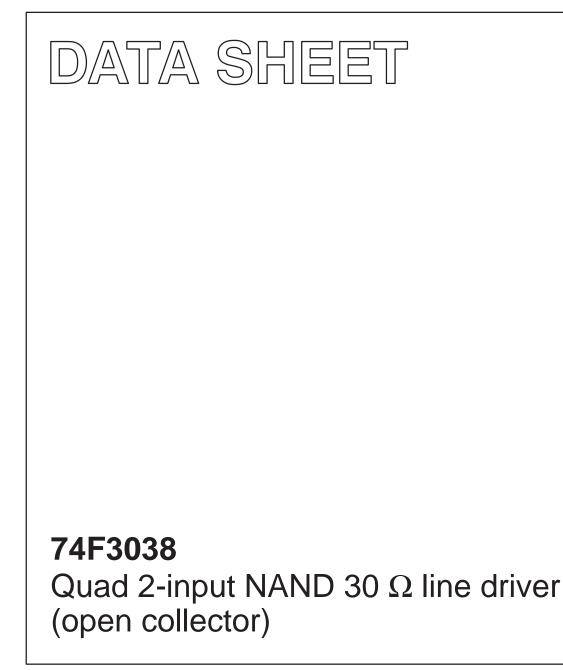
# INTEGRATED CIRCUITS



Product specification Supersedes data of 1990 Jan 29 IC15 Data Handbook

1998 May 21



## 74F3038

#### FEATURES

- 30Ω line driver
- 160mA output drive capability
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V<sub>CC</sub> and GND when both side pins are used

#### DESCRIPTION

The 74F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F3038 can sink 160mA with a  $V_{CC}$  as low as 4.5V. This guarantees incident wave switching with  $V_{OL}$  not more than 0.8V while driving impedances as low as 30 $\Omega$ . This is applicable with any combination of outputs using continuous duty.

The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50pF capacitance, a 500 $\Omega$  pull-up resistor and a 500 $\Omega$  pull-down resistor. (See Test Circuit).

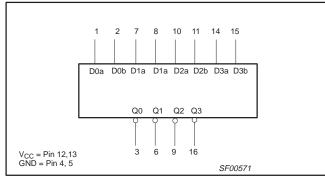
Reducing the load resistors to 100 $\Omega$  will decrease the t<sub>PLH</sub> propagation delay by approximately 50% while increasing t<sub>PHL</sub> only slightly. The graph of typical propagation delay versus load resistor (see AC Characteristics section for Graph) shows a spline fit curve from four measured data points, R<sub>L</sub> = 30 $\Omega$ , R<sub>L</sub> = 100 $\Omega$ , R<sub>L</sub> = 300 $\Omega$ , and R<sub>L</sub> = 500 $\Omega$ .

#### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

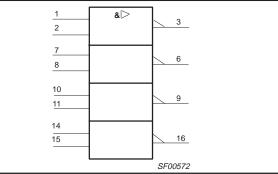
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20µA/0.6mA
Qn	Data outputs	OC/266	OC/160mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state. OC = Open Collector.

#### LOGIC SYMBOL



#### **IEC/IEEE SYMBOL**



PIN CONFIGURATIO	ON	
D0a 1		16 Q3
D0b 2		15 D3b
Q0 3		14 D3a
GND 4		13 V <sub>CC</sub>
GND 5		12 V <sub>CC</sub>
Q1 6		11 D2a
D1a 7		10 D2b
D1b 8		9 Q2
		SF00570

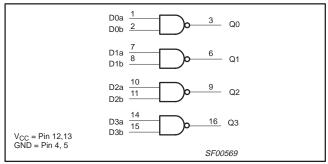
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	6.0ns	17mA

#### **ORDERING INFORMATION**

DESCRIPTION	$\label{eq:scription} \begin{array}{c} \text{COMMERCIAL RANGE} \\ \text{V}_{CC} = 5V \pm 10\%, \\ \text{T}_{amb} = 0^\circ \text{C to } +70^\circ \text{C} \end{array}$			
16-pin Plastic DIP	N74F3038N	SOT38-4		
16-pin Plastic SOL	N74F3038D	SOT162-1		

74F3038

#### LOGIC DIAGRAM



#### **FUNCTION TABLE**

INPU	OUTPUT		
Dna	Dna Dnb		
L	L	Н	
L	Н	Н	
н	L	н	
н	Н	L	

H = High voltage level L = Low voltage level

#### **ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	–0.5 to $V_{CC}$	V
I <sub>OUT</sub>	Current applied to output in Low output state	320	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

#### **RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER		UNIT		
STWBUL	PARAMETER	MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
V <sub>OH</sub>	High-level output voltage			4.5	V
I <sub>OL</sub>	Low-level output current			160	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

74F3038

#### DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

					01		LIMITS		
SYMBOL	PARAMETER	PARAMETER TEST CONDITIONS <sup>1</sup>					TYP <sup>2</sup>	MAX	UNIT
I <sub>OH</sub>	High-level output current		$V_{CC} = MIN, V_{II}$	= MAX, V <sub>IH</sub> = M	IN, V <sub>OH</sub> = MAX			250	μΑ
M	Low-level output current		V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX	I <sub>OL</sub> = 100mA	±10% V <sub>CC</sub>		0.42	0.55	V
V <sub>OL</sub>			$V_{IH} = MIN$	I <sub>OL</sub> = 160mA <sup>3</sup>	$\pm$ 5% V <sub>CC</sub>			0.80	V
V <sub>IK</sub>	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$				-0.73	-1.2	V
I <sub>I</sub>	Input current at maximun voltage	n input	Vc	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA
I <sub>IH</sub>	High-level input current		۷ <sub>C</sub>	$C_C = MAX, V_I = 2.$	7V			20	μΑ
I <sub>IL</sub>	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$					-0.6	mA
1	Supply current (total)	I <sub>CCH</sub>	Vaa	= MAX	$V_{IN} = GND$		3.5	6.0	mA
ICC	Supply current (total)	I <sub>CCL</sub>	VCC =		$V_{IN} = 4.5V$		30	40	mA

#### NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

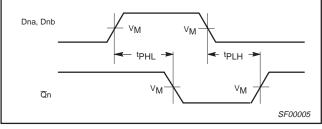
2. All typical values are at  $V_{CC} = 5V$ ,  $T_{amb} = 25^{\circ}C$ . 3.  $I_{OL1}$  is the current necessary to guarantee the High to Low transition in a 30 $\Omega$  transmission line on the incident wave.

#### **AC ELECTRICAL CHARACTERISTICS**

					LIM	ITS		
SYMBOL	PARAMETER	TEST CONDITION	V.	<sub>mb</sub> = +25 <sub>CC</sub> = +5.0 0pF, R <sub>L</sub> =	V	T <sub>amb</sub> = 0°C V <sub>CC</sub> = +5. C <sub>L</sub> = 50pF,	C to +70°C 0V ± 10% R <sub>L</sub> = 500Ω	UNIT
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb to Qn	Waveform 1	6.0 1.0	8.5 2.0	11.5 5.0	6.0 1.0	12.0 5.0	ns

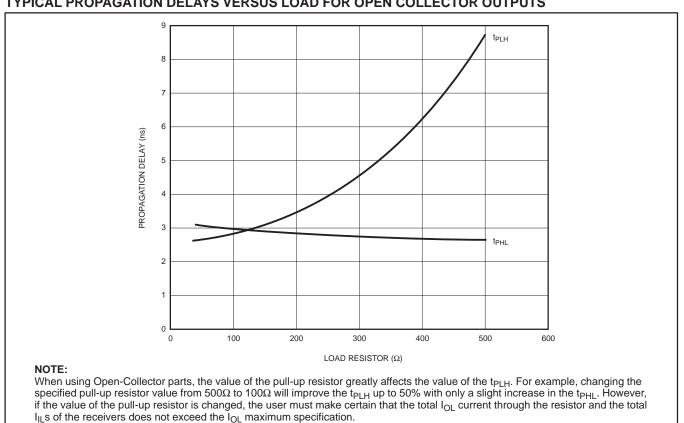
#### **AC WAVEFORMS**

For all waveforms,  $V_M = 1.5V$ .



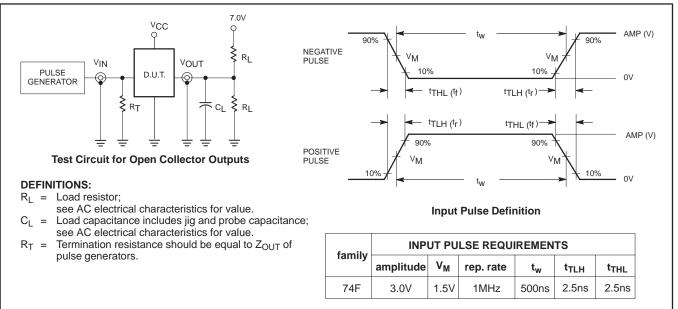
Waveform 1. Propagation Delay for Inputs to Output

### 74F3038



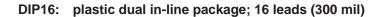
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

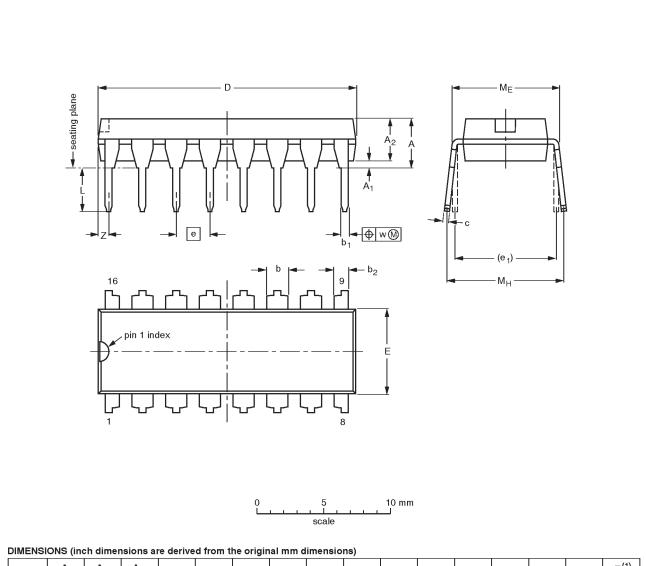
#### **TEST CIRCUIT AND WAVEFORMS**



SF00027

SF01361





UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	с	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

#### Note

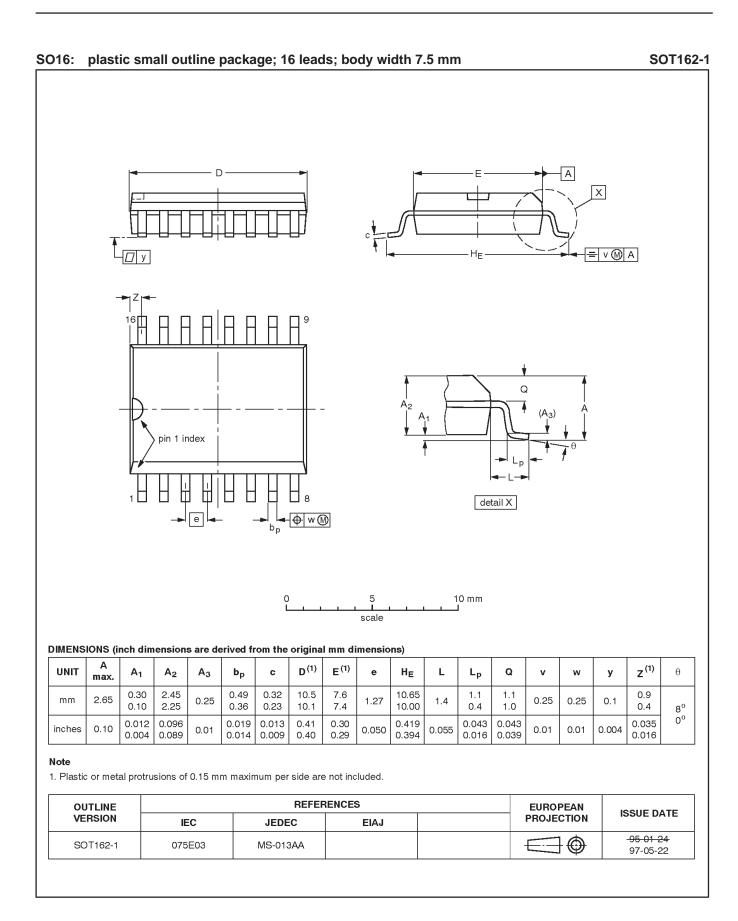
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN ISSUE DATE				
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE			
SOT38-4					<del>-92-11-17</del> 95-01-14			

74F3038

SOT38-4

### 74F3038



#### 1998 May 21

## 74F3038

#### Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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