

74HC393; 74HCT393

Dual 4-bit binary ripple counter

Rev. 4 — 16 May 2013

Product data sheet

1. General description

The 74HC393; 74HCT393 is a dual 4-stage binary ripple counter. Each counter features a clock input (\overline{nCP}), an overriding asynchronous master reset input (nMR) and 4 buffered parallel outputs ($nQ0$ to $nQ3$). The counter advances on the HIGH-to-LOW transition of \overline{nCP} . A HIGH on nMR clears the counter stages and forces the outputs LOW, independent of the state of \overline{nCP} . Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Input levels:
 - ◆ For 74HC393: CMOS level
 - ◆ For 74HCT393: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V.
- Two 4-bit binary counters with individual clocks
- Divide by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually

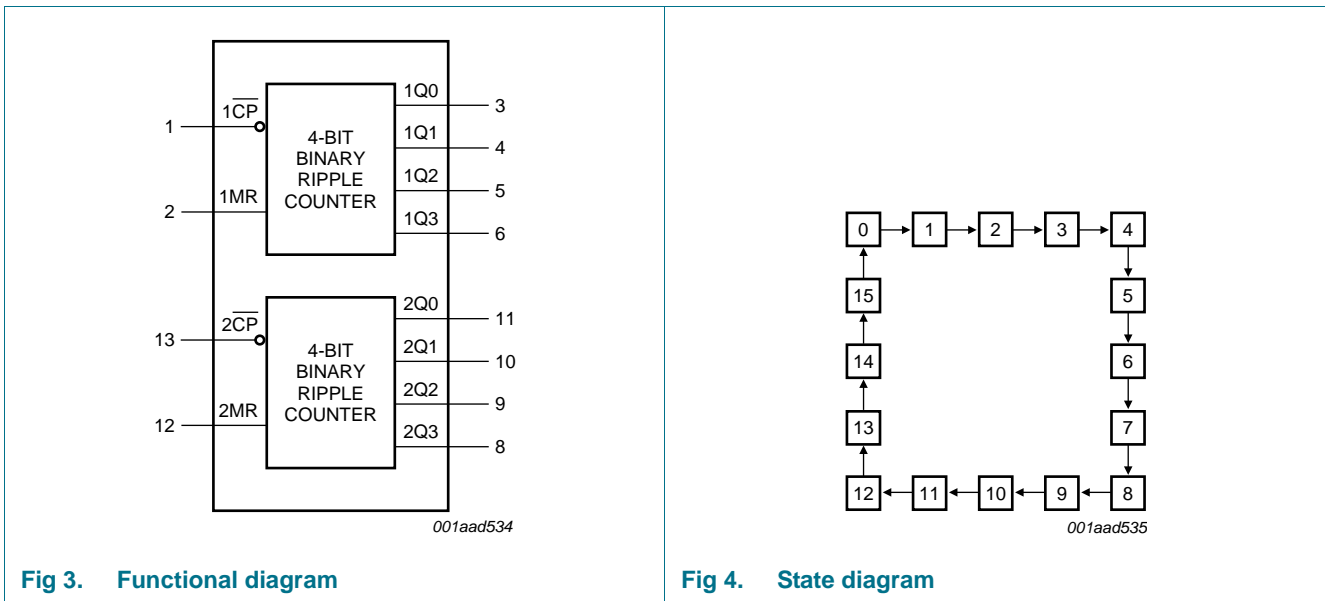
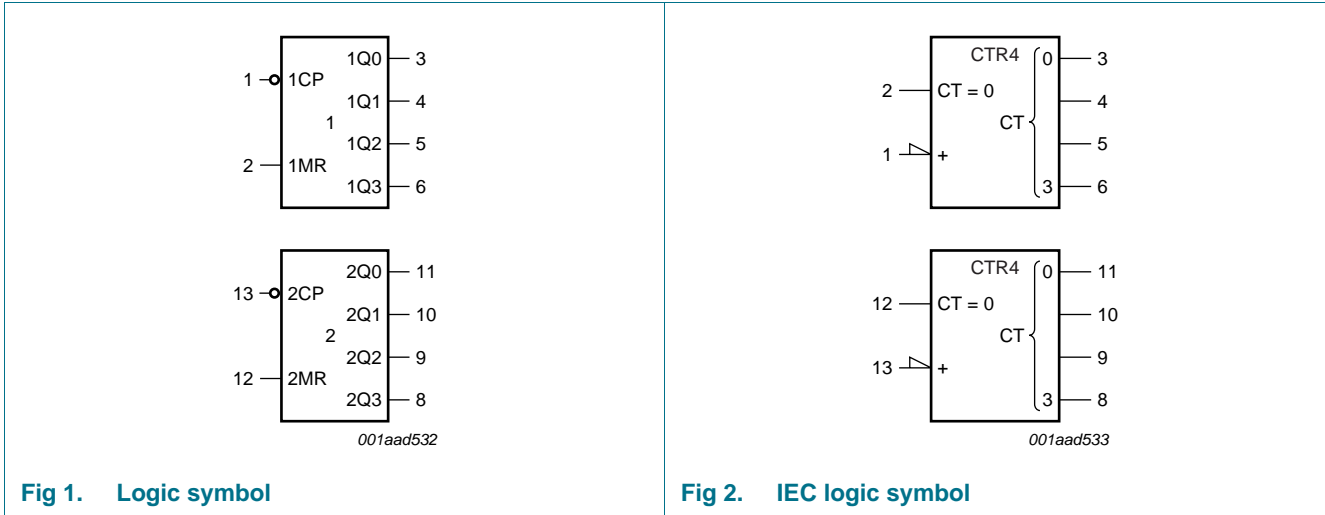
3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC393N 74HCT393N | -40 °C to +125 °C | DIP14 | plastic dual in-line package; 14 leads (300 mil) | SOT27-1 |
| 74HC393D 74HCT393D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HC393DB 74HCT393DB | -40 °C to +125 °C | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74HC393PW 74HCT393PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74HC393BQ 74HCT393BQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |



4. Functional diagram



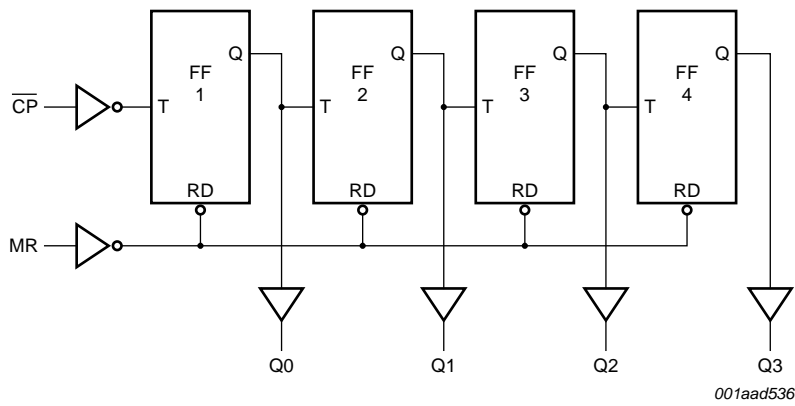


Fig 5. Logic diagram (one counter)

5. Pinning information

5.1 Pinning

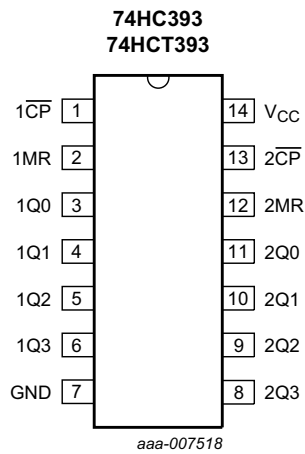
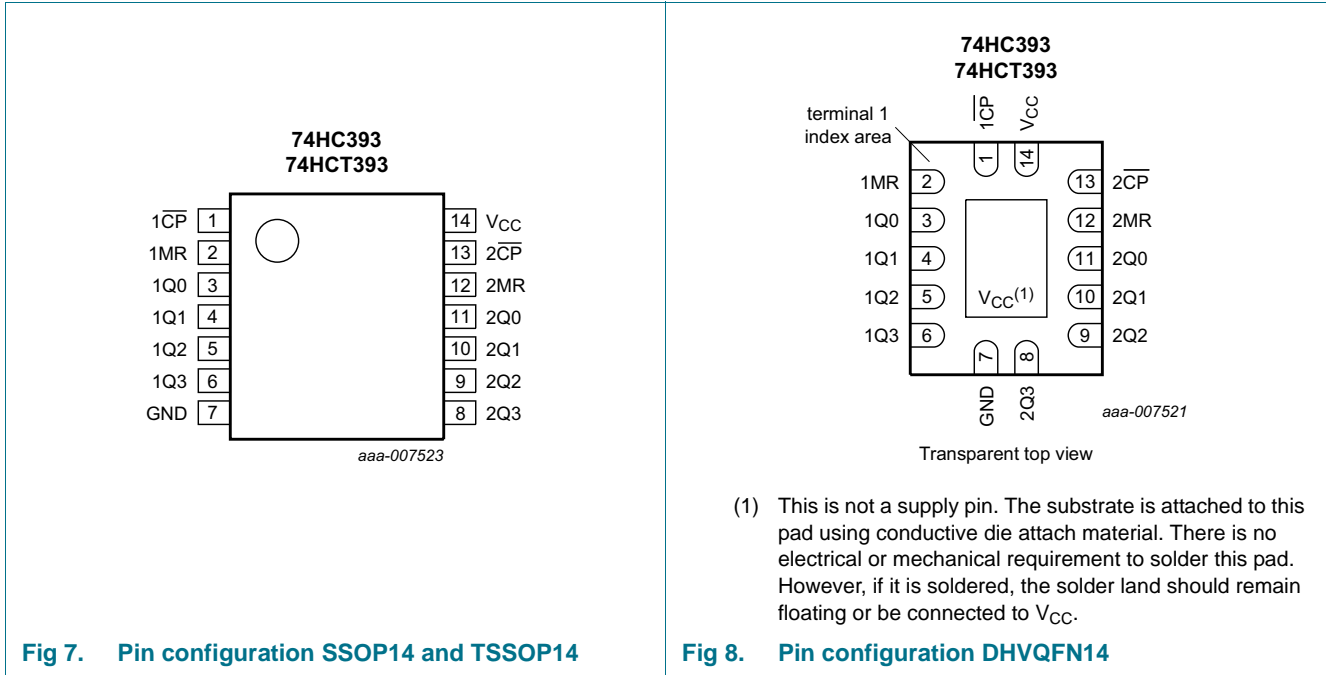


Fig 6. Pin configuration DIP14 and SO14



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------|-----|---|
| $1\overline{CP}$ | 1 | clock input (HIGH-to-LOW, edge-triggered) |
| 1MR | 2 | asynchronous master reset input (active HIGH) |
| 1Q0 | 3 | flip-flop output |
| 1Q1 | 4 | flip-flop output |
| 1Q2 | 5 | flip-flop output |
| 1Q3 | 6 | flip-flop output |
| GND | 7 | ground (0 V) |
| 2Q3 | 8 | flip-flop output |
| 2Q2 | 9 | flip-flop output |
| 2Q1 | 10 | flip-flop output |
| 2Q0 | 11 | flip-flop output |
| 2MR | 12 | asynchronous master reset input (active HIGH) |
| $2\overline{CP}$ | 13 | clock input (HIGH-to-LOW, edge-triggered) |
| V_{CC} | 14 | supply voltage |

6. Functional description

Table 3. Count sequence for one counter [1]

| Count | Output | | | |
|-------|--------|-----|-----|-----|
| | nQ0 | nQ1 | nQ2 | nQ3 |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------|-------------------------|--|------|----------|------|----|
| V_{CC} | supply voltage | | -0.5 | +7 | V | |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA | |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA | |
| I_O | output current | $V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$ | - | ± 25 | mA | |
| I_{CC} | supply current | | - | ± 50 | mA | |
| I_{GND} | ground current | | - | ± 50 | mA | |
| T_{stg} | storage temperature | | -65 | +150 | °C | |
| P_{tot} | total power dissipation | DIP14 package | [1] | - | 750 | mW |
| | | SO14, SSOP14, TSSOP14 and DHVQFN14 package | [2] | - | 500 | mW |

[1] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC393 | | | 74HCT393 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---|---|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC393 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V | |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±0.1 | - | ±0.1 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|---|-------|------|-----------|------------------|-----------|-------------------|-----------|---------------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C_I | input capacitance | | - | 3.5 | - | | | | | pF |
| 74HCT393 | | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | | $I_O = -20 \mu\text{A}$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -6 \text{ mA}$ | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | | $I_O = 20 \mu\text{A}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 6.0 \text{ mA}$ | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I_I | input leakage current | $V_I = V_{CC} \text{ or } \text{GND}; V_{CC} = 5.5 \text{ V}$ | - | - | ± 0.1 | - | ± 1.0 | - | ± 1.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC} \text{ or } \text{GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$ | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI_{CC} | additional supply current | $V_I = V_{CC} - 2.1 \text{ V};$ other inputs at V_{CC} or $\text{GND};$ $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; I_O = 0 \text{ A}$ | | | | | | | | |
| | | per input pin; \overline{nCP} | - | 40 | 144 | - | 180 | - | 196 | μA |
| | | per input pin; nMR | - | 100 | 360 | - | 450 | - | 490 | μA |
| C_I | input capacitance | | - | 3.5 | - | | | | | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 11](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC393 | | | | | | | | | | |
| t_{pd} | propagation delay | \overline{nCP} to $nQ0$; see Figure 9 ^[1] | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | - | 41 | 125 | - | 155 | - | 190 | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 15 | 25 | - | 31 | - | 38 | ns |
| | | $V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 12 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 12 | 21 | - | 26 | - | 32 | ns |
| | | nQx to $nQ(x+1)$; see Figure 9 ^[1] | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | - | 14 | 45 | - | 55 | - | 70 | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 5 | 9 | - | 11 | - | 14 | ns |
| | | $V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 5 | - | - | - | - | ns | |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 4 | 8 | - | 9 | - | 12 | ns |
| t_{PHL} | HIGH to LOW propagation delay | nMR to nQx ; see Figure 10 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | - | 39 | 140 | - | 175 | - | 210 | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 14 | 28 | - | 35 | - | 42 | ns |
| | | $V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 11 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 11 | 24 | - | 30 | - | 36 | ns |
| t_t | transition time | Qn ; see Figure 9 ^[2] | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 6 | 13 | - | 16 | - | 19 | ns |
| t_W | pulse width | \overline{nCP} HIGH or LOW; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | 14 | 5 | - | 17 | - | 20 | - | ns |
| | | nMR HIGH; see Figure 10 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | 80 | 19 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | 16 | 7 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | 14 | 6 | - | 17 | - | 20 | ns | |
| t_{rec} | recovery time | nMR to \overline{nCP} ; see Figure 10 | | | | | | | | |
| | | $V_{CC} = 2.0 \text{ V}$ | 5 | 3 | - | 5 | - | 5 | - | ns |
| | | $V_{CC} = 4.5 \text{ V}$ | 5 | 1 | - | 5 | - | 5 | - | ns |
| | | $V_{CC} = 6.0 \text{ V}$ | 5 | 1 | - | 5 | - | 5 | ns | |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 11](#).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|-----------------------|-------------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $f_{\text{clk(max)}}$ | maximum clock frequency | see Figure 9 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 6 | 30 | - | 5 | - | 4 | - | MHz |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 30 | 90 | - | 24 | - | 20 | - | MHz |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 99 | - | - | - | - | - | MHz |
| | | $V_{\text{CC}} = 6.0 \text{ V}$ | 35 | 107 | - | 28 | - | 24 | - | MHz |
| C_{PD} | power dissipation capacitance | $C_L = 50 \text{ pF}; f = 1 \text{ MHz}; V_I = \text{GND to } V_{\text{CC}}$ | [3] | - | 23 | - | - | - | - | pF |

74HCT393

| | | | | | | | | | | |
|-----------------------|-------------------------------|--|----|----|----|----|----|----|----|-----|
| t_{pd} | propagation delay | $\overline{\text{nCP}}$ to nQ0 ; see Figure 9 [1] | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 15 | 25 | - | 31 | - | 38 | ns |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 20 | - | - | - | - | - | ns |
| | | nQx to nQ(x+1) ; see Figure 9 [1] | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 6 | 10 | - | 13 | - | 15 | ns |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 6 | - | - | - | - | ns | |
| t_{PHL} | HIGH to LOW propagation delay | nMR to nQx ; see Figure 10 | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 18 | 32 | - | 40 | - | 48 | ns |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 15 | - | - | - | - | - | ns |
| t_t | transition time | Qn ; see Figure 9 [2] | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | - | 7 | 15 | - | 19 | - | 22 | ns |
| t_W | pulse width | $\overline{\text{nCP}}$ HIGH or LOW; see Figure 9 | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 19 | 11 | - | 24 | - | 29 | - | ns |
| | | nMR HIGH; see Figure 10 | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 16 | 6 | - | 20 | - | 24 | - | ns |
| t_{rec} | recovery time | nMR to $\overline{\text{nCP}}$; see Figure 10 | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 5 | 0 | - | 5 | - | 5 | - | ns |
| $f_{\text{clk(max)}}$ | maximum clock frequency | see Figure 9 | | | | | | | | |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 27 | 48 | - | 22 | - | 18 | - | MHz |
| | | $V_{\text{CC}} = 5 \text{ V}; C_L = 15 \text{ pF}$ | - | 53 | - | - | - | - | - | MHz |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 11](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------|-------------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C_{PD} | power dissipation capacitance | $C_L = 50 \text{ pF}$; $f = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$ | - | 25 | - | - | - | - | - | pF |

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1 Waveforms

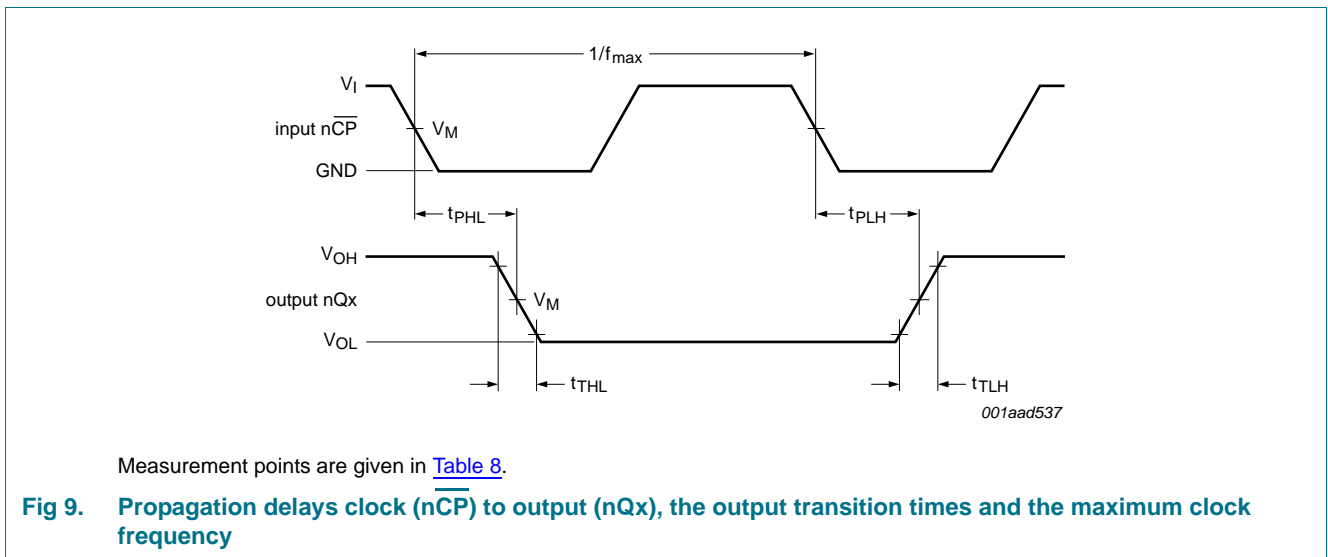
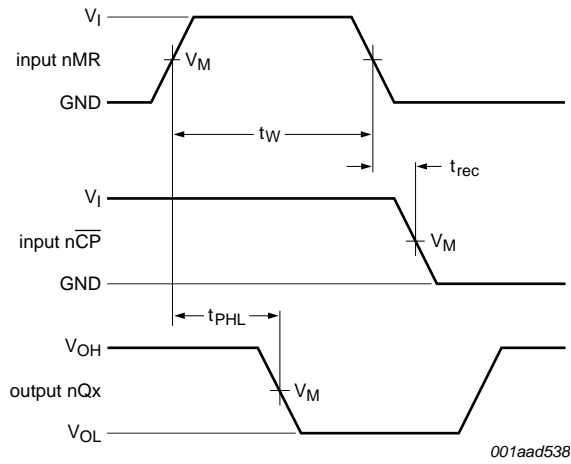


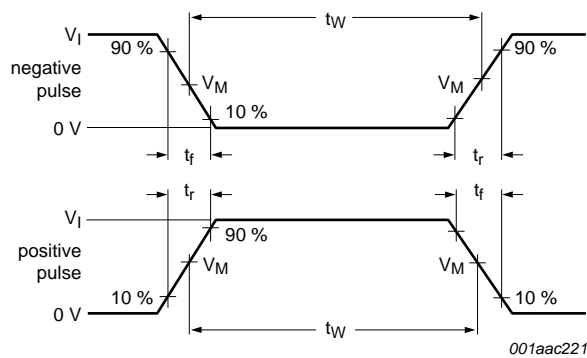
Table 8. Measurement points

| Type | Input | Output |
|----------|-------------|-------------|
| | V_M | V_M |
| 74HC393 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT393 | 1.3 V | 1.3 V |



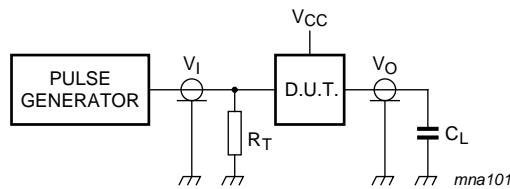
Measurement points are given in [Table 8](#).

Fig 10. Propagation delays clock (nCP) to output (nQx), pulse width master reset (nMR), and recovery time master reset (nMR) to clock (nCP)



Measurement points are given in [Table 8](#).

a. Input pulse definition



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

b. Test circuit

Fig 11. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load |
|----------|----------|------------|--------------|
| | V_I | t_r, t_f | C_L |
| 74HC393 | V_{CC} | 6 ns | 15 pF, 50 pF |
| 74HCT393 | 3 V | 6 ns | 15 pF, 50 pF |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

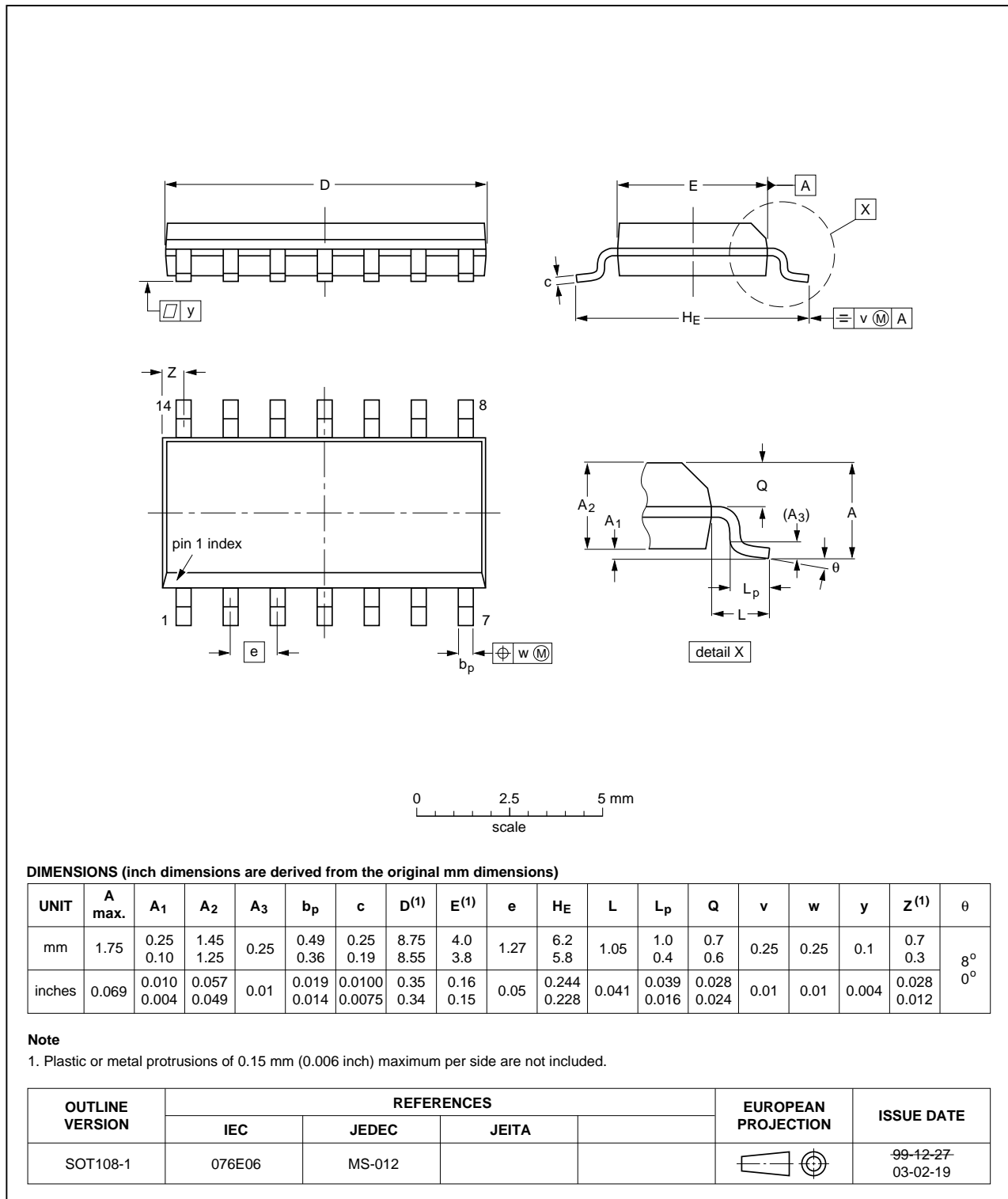


Fig 12. Package outline SOT108-1 (SO14)

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

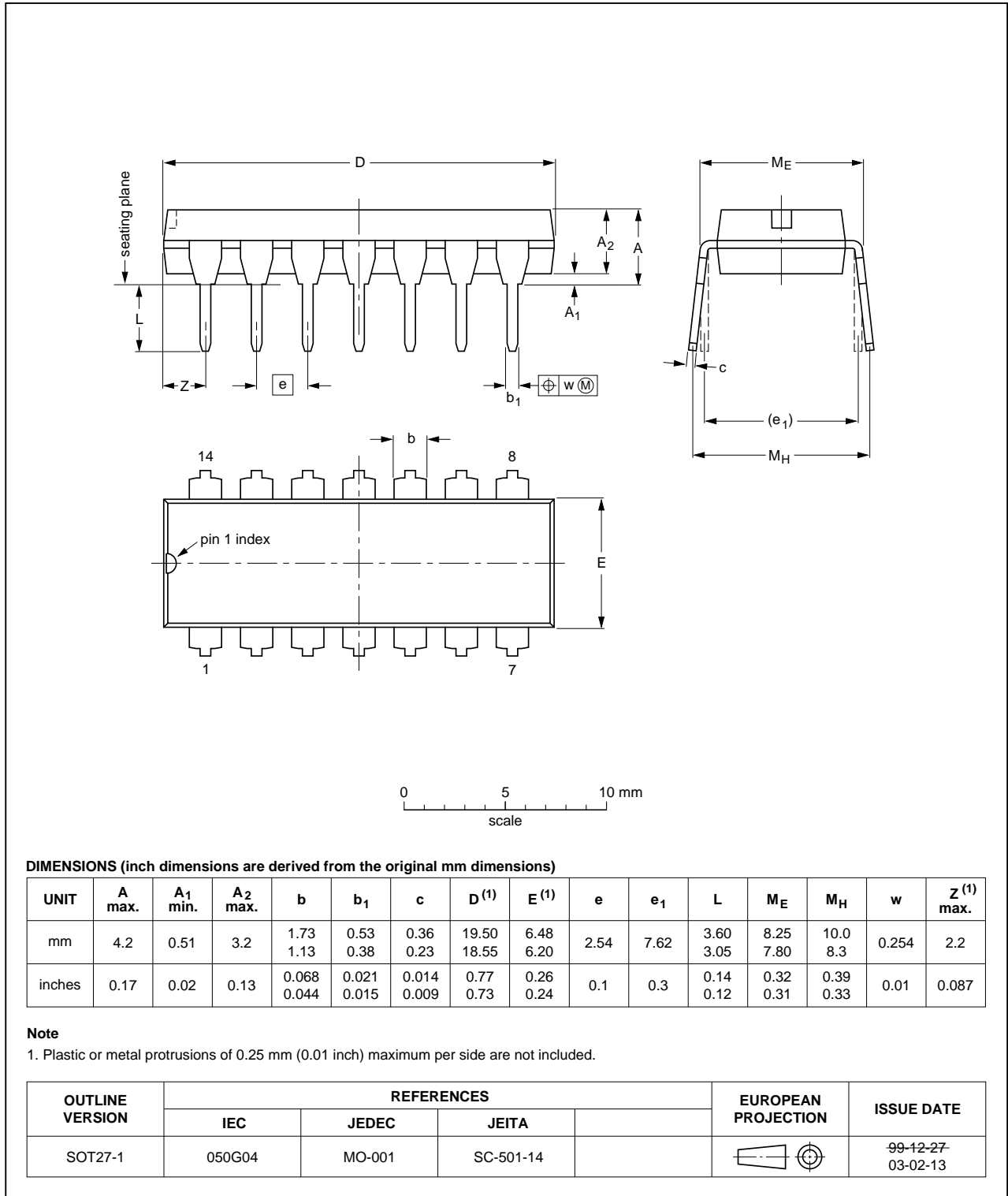


Fig 13. Package outline SOT27-1 (DIP14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

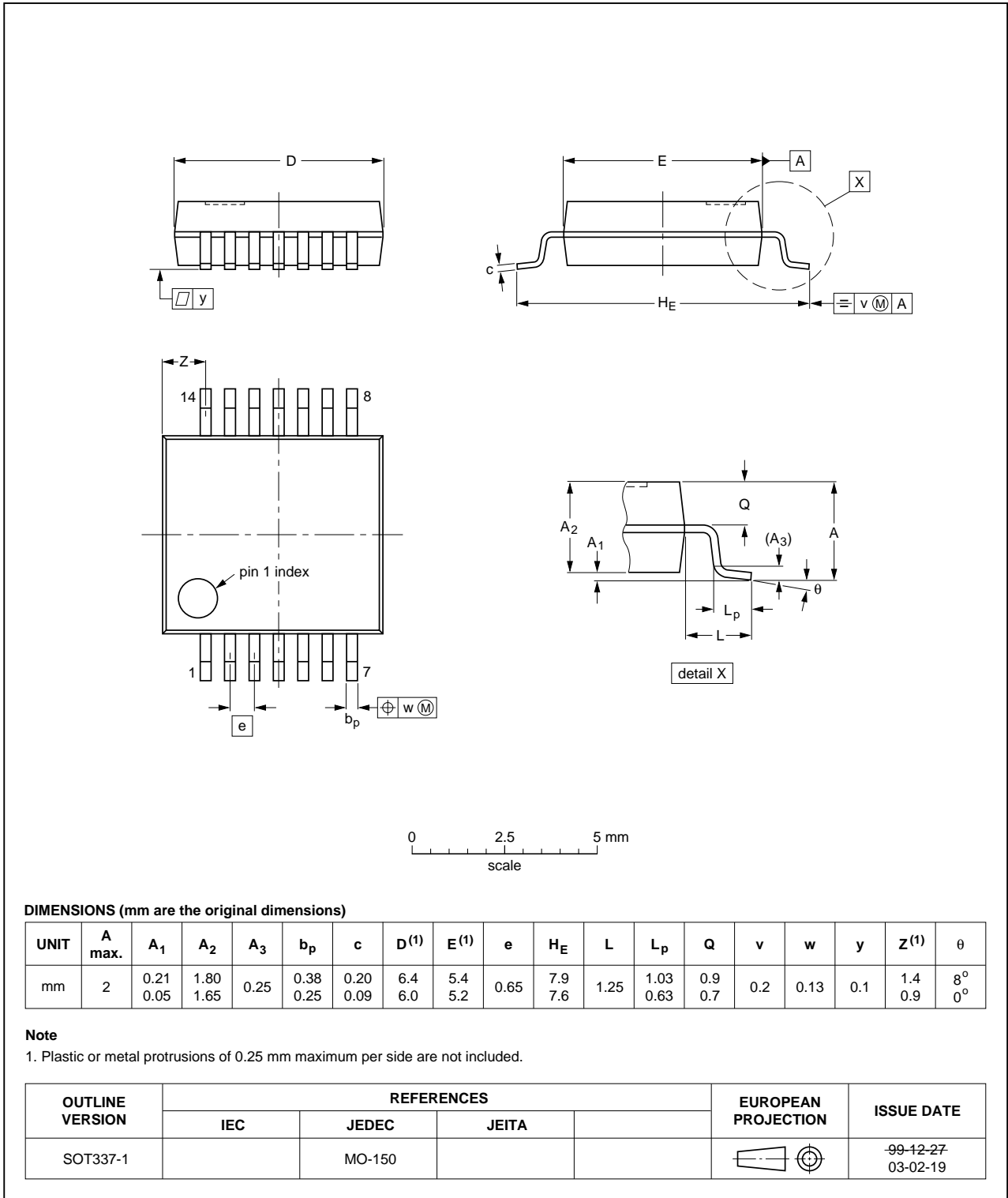


Fig 14. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

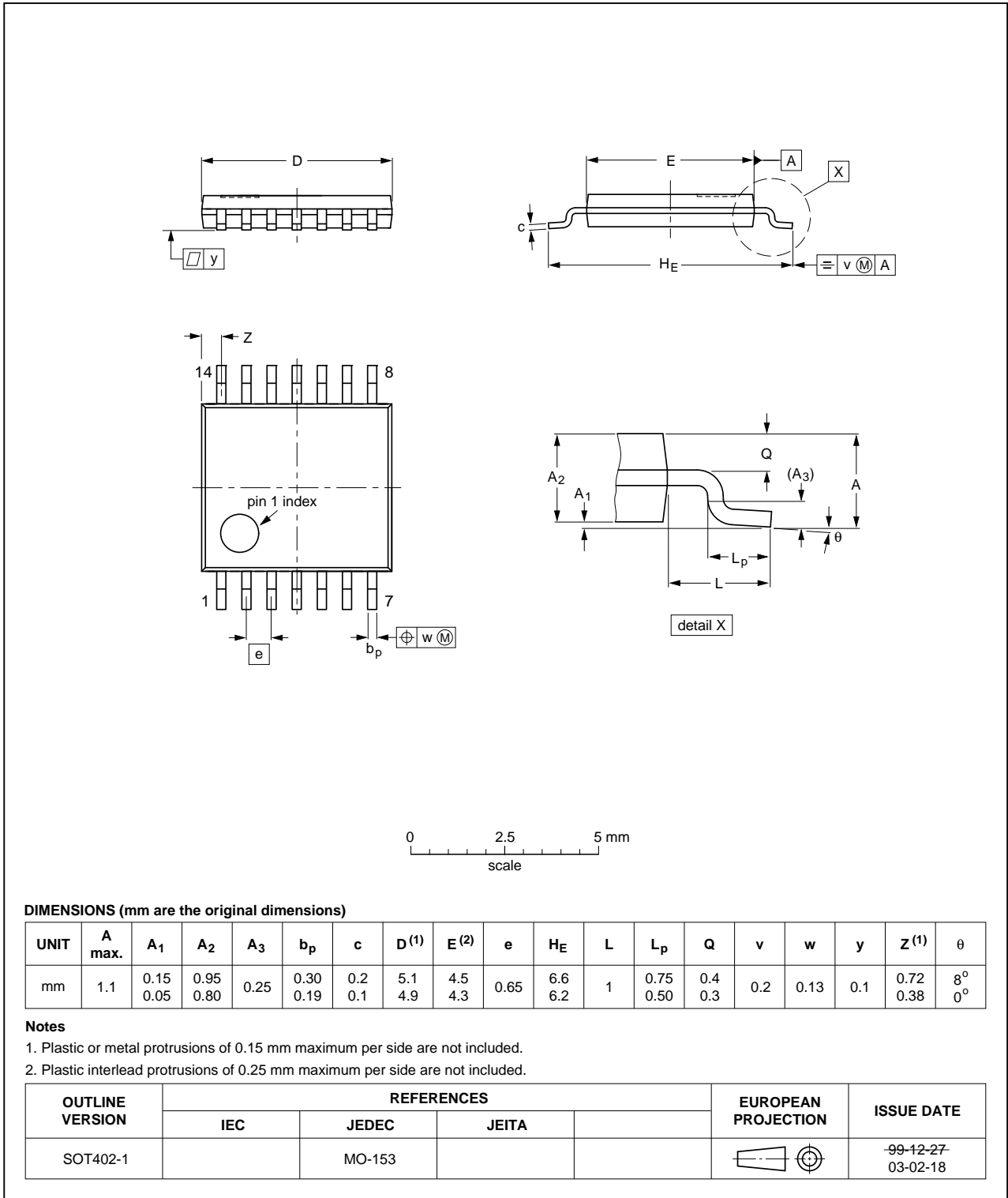


Fig 15. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

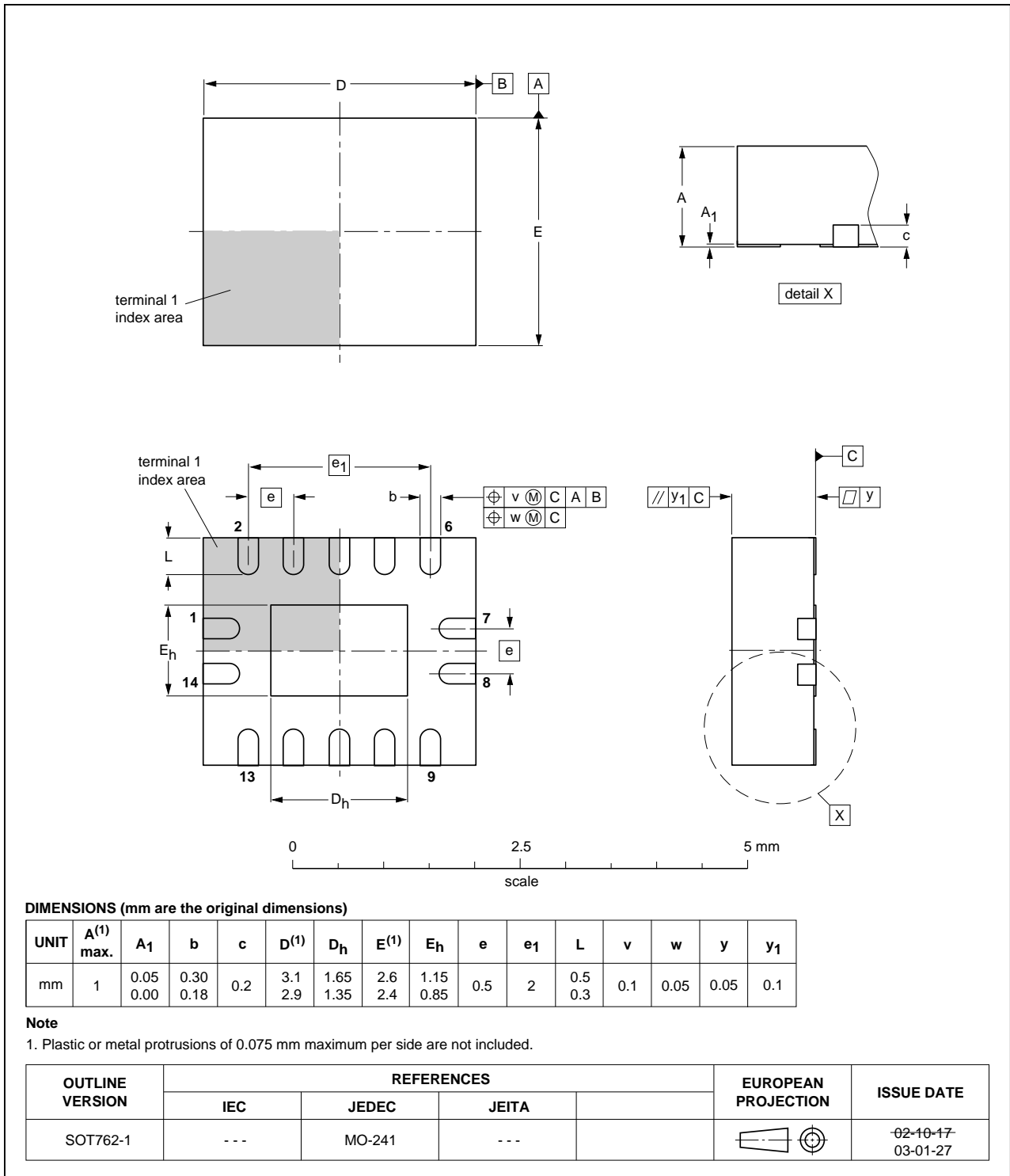


Fig 16. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations table

| Acronym | Description |
|---------|--|
| CMOS | Complementary Metal Oxide Semiconductor |
| TTL | Transistor-Transistor Logic |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| DUT | Device Under Test |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--------------|-----------------------|---------------|--|
| 74HC_HCT393 v.4 | 20130516 | Product data sheet | - | 74HC_HCT393 v.3 |
| Modifications: | | | | |
| | | | | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate. |
| 74HC_HCT393 v.3 | 20050906 | Product data sheet | - | 74HC_HCT393_CNV v.2 |
| 74HC_HCT393_CNV v.2 | 19901201 | Product specification | - | - |

14. Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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16. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Ordering information | 1 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 3 |
| 5.1 | Pinning | 3 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 5 |
| 7 | Limiting values | 5 |
| 8 | Recommended operating conditions | 6 |
| 9 | Static characteristics | 6 |
| 10 | Dynamic characteristics | 8 |
| 10.1 | Waveforms | 10 |
| 11 | Package outline | 13 |
| 12 | Abbreviations | 18 |
| 13 | Revision history | 18 |
| 14 | Legal information | 19 |
| 14.1 | Data sheet status | 19 |
| 14.2 | Definitions | 19 |
| 14.3 | Disclaimers | 19 |
| 14.4 | Trademarks | 20 |
| 15 | Contact information | 20 |
| 16 | Contents | 21 |

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Date of release: 16 May 2013

Document identifier: 74HC_HCT393