74LVC1G175

Single D-type flip-flop with reset; positive-edge trigger

Rev. 5 — 6 December 2011 **Product data sheet**

1. General description

The 74LVC1G175 is a low-power, low-voltage single positive edge triggered D-type flip-flop with individual data (D) input, clock (CP) input, master reset ($\overline{MR}$) input, and Q output.

The master reset ($\overline{MR}$) is an asynchronous active LOW input and operates independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V.
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G175GW	–40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVC1G175GV	–40 °C to +125 °C	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457
74LVC1G175GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G175GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
74LVC1G175GN	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G175GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

4. Marking

Table 2. Marking

Type number	Marking code[1]
74LVC1G175GW	YT
74LVC1G175GV	V75
74LVC1G175GM	YT
74LVC1G175GF	YT
74LVC1G175GN	YT
74LVC1G175GS	YT

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

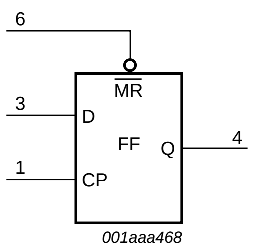


Fig 1. Logic symbol.

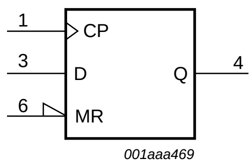


Fig 2. IEC logic symbol.

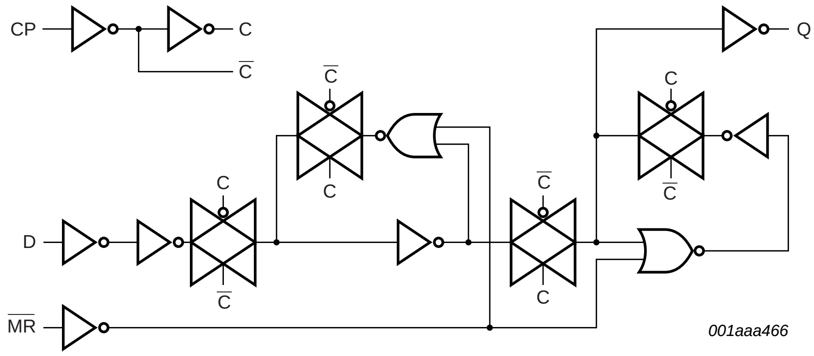


Fig 3. Logic diagram.

6. Pinning information

6.1 Pinning

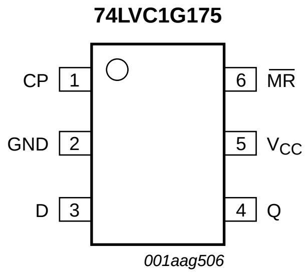


Fig 4. Pin configuration SOT363 and SOT457

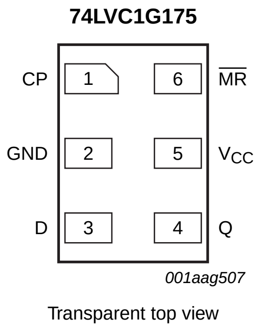


Fig 5. Pin configuration SOT886

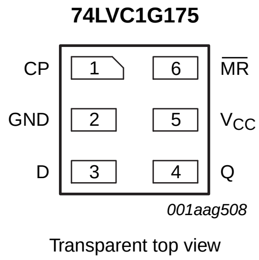


Fig 6. Pin configuration SOT891, SOT1115 and SOT1202

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
GND	2	ground (0 V)
D	3	data input
Q	4	output Q
V_{CC}	5	supply voltage
$\overline{MR}$	6	master reset input (active LOW)

7. Functional description

Table 4. Function table[1]

Operating mode	Input			Output
	$\overline{MR}$	CP	D	Q
Reset (clear)	L	X	X	L
Load ‘1’	H	↑	h	H
Load ‘0’	H	↑	l	L

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH CP transition;
X = don’t care.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	–50	-	mA
V_I	input voltage	[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	Active mode [1][2]	–0.5	V_{CC} + 0.5	V
		Power-down mode [1][2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		–100	-	mA
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C [3]	-	250	mW
T_{stg}	storage temperature		–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For SC-88 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	1.54	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.9	2.15	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	2.50	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.3	2.62	-	V
		I_O = –32 mA; V_{CC} = 4.5 V	3.8	4.11	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	0.07	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	0.12	0.30	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.17	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.33	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	0.39	0.55	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND [2]	-	±0.1	±5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±10	µA

Table 7. Static characteristics *…continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{CC}	supply current	V_{CC} = 1.65 V to 5.5 V; I_O = 0 A; V_I = 5.5 V or GND		-	0.1	10	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} − 0.6 V; I_O = 0 A	[2]	-	5	500	μA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}		-	2.5	-	pF
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V		0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V		-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V		-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA; V_{CC} = 1.65 V to 5.5 V		V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V		0.95	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V		1.7	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V		1.9	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V		2.0	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V		3.4	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V		-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V		-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V		-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V		-	-	0.80	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND		-	-	±20	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V		-	-	±20	μA
I_{CC}	supply current	V_{CC} = 1.65 V to 5.5 V; I_O = 0 A; V_I = 5.5 V or GND		-	-	40	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} − 0.6 V; I_O = 0 A		-	-	5000	μA

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Q; see Figure 7 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.5	4.9	13.4	1.5	17	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.1	7.1	1.0	9.0	ns
		V_{CC} = 2.7 V	1.0	3.2	7.1	1.0	9.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.1	5.7	0.5	7.5	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.2	4.0	0.5	5.5	ns
		$\overline{MR}$ to Q; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	1.5	4.3	12.9	1.5	17	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.8	7.0	1.0	9.0	ns
		V_{CC} = 2.7 V	1.0	3.0	7.0	1.0	9.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	5.8	0.5	7.5	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.0	4.1	0.5	5.5	ns
t_W	pulse width	CP HIGH or LOW; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	6.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	1.3	-	2.7	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	ns
		$\overline{MR}$ LOW; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	6.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	1.6	-	2.7	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	ns
t_{rec}	recovery time	$\overline{MR}$; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	1.9	-	-	1.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	ns
		V_{CC} = 2.7 V	1.3	-	-	1.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	0.4	-	1.2	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
t_{su}	set-up time	D to CP; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	2.9	-	-	2.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	ns
		V_{CC} = 2.7 V	1.7	-	-	1.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	0.5	-	1.3	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.1	-	-	1.1	-	ns

Table 8. Dynamic characteristics *...continued*
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_h	hold time	D to CP; see Figure 7							
		V_{CC} = 1.65 V to 1.95 V		0.0	-	-	0.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		0.3	-	-	0.3	-	ns
		V_{CC} = 2.7 V		0.5	-	-	0.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.2	0.2	-	1.2	-	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	-	-	0.5	-	ns
f_{max}	maximum frequency	CP; see Figure 7							
		V_{CC} = 1.65 V to 1.95 V		80	125	-	80	-	MHz
		V_{CC} = 2.3 V to 2.7 V		175	-	-	175	-	MHz
		V_{CC} = 2.7 V		175	-	-	175	-	MHz
		V_{CC} = 3.0 V to 3.6 V		175	300	-	175	-	MHz
		V_{CC} = 4.5 V to 5.5 V		200	-	-	200	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V	[3]	-	14	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

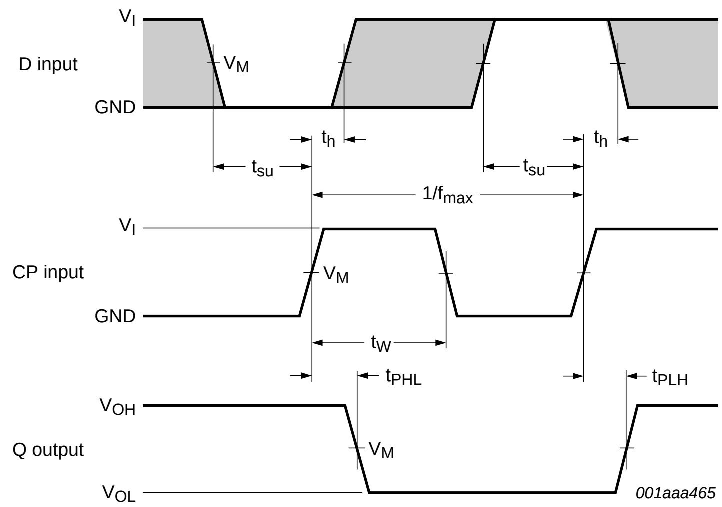
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms

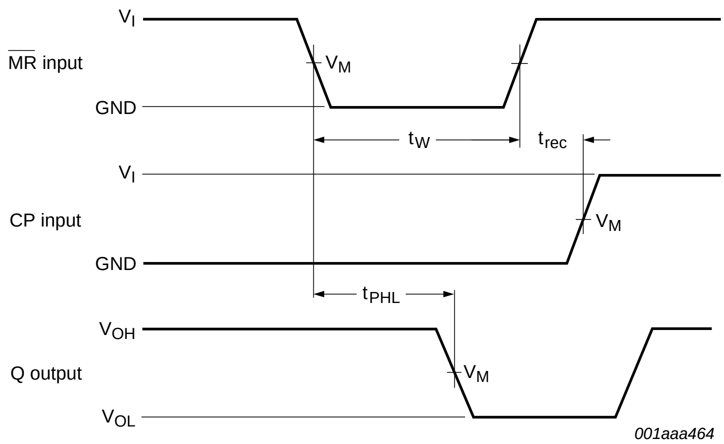


Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 7. The clock input (CP) to output (Q) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times, and the maximum clock pulse frequency



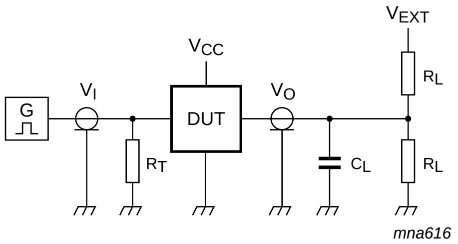
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 8. The master reset ($\overline{MR}$) input to output (Q) propagation delays, the master reset pulse width, and the $\overline{MR}$ to CP recovery time

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

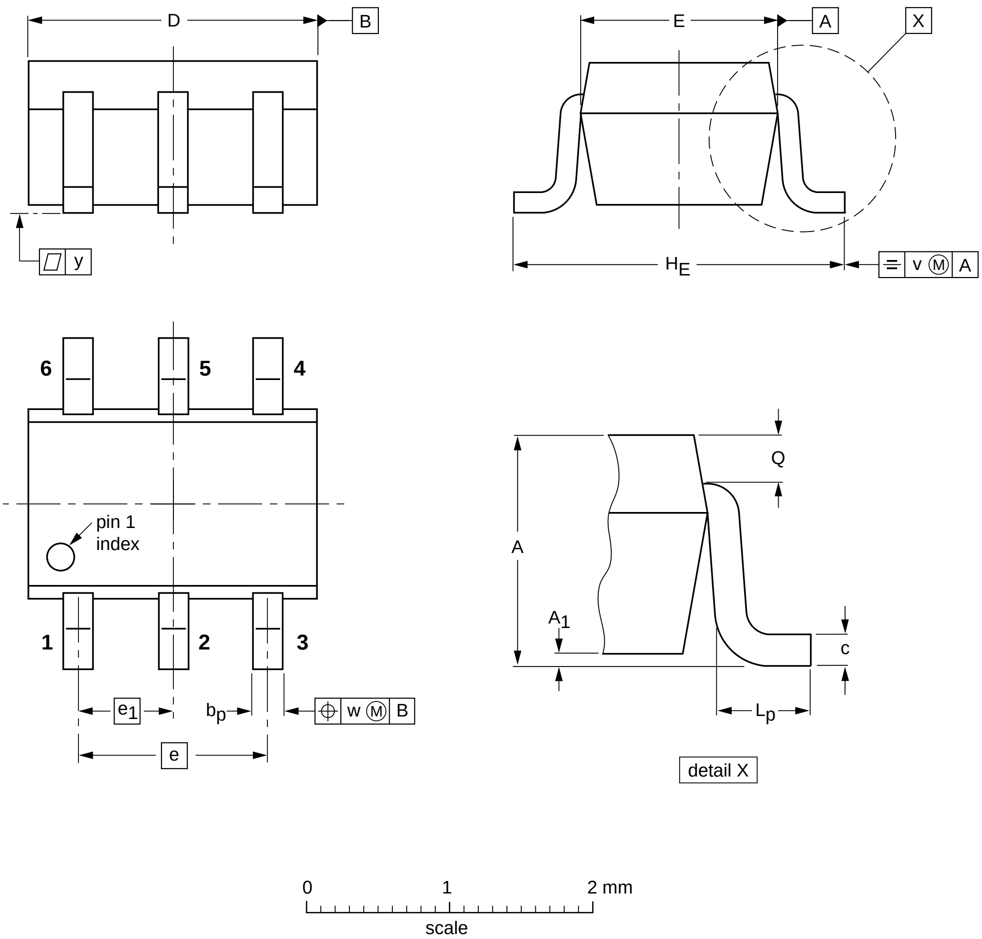
Fig 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Package outline

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

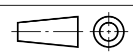
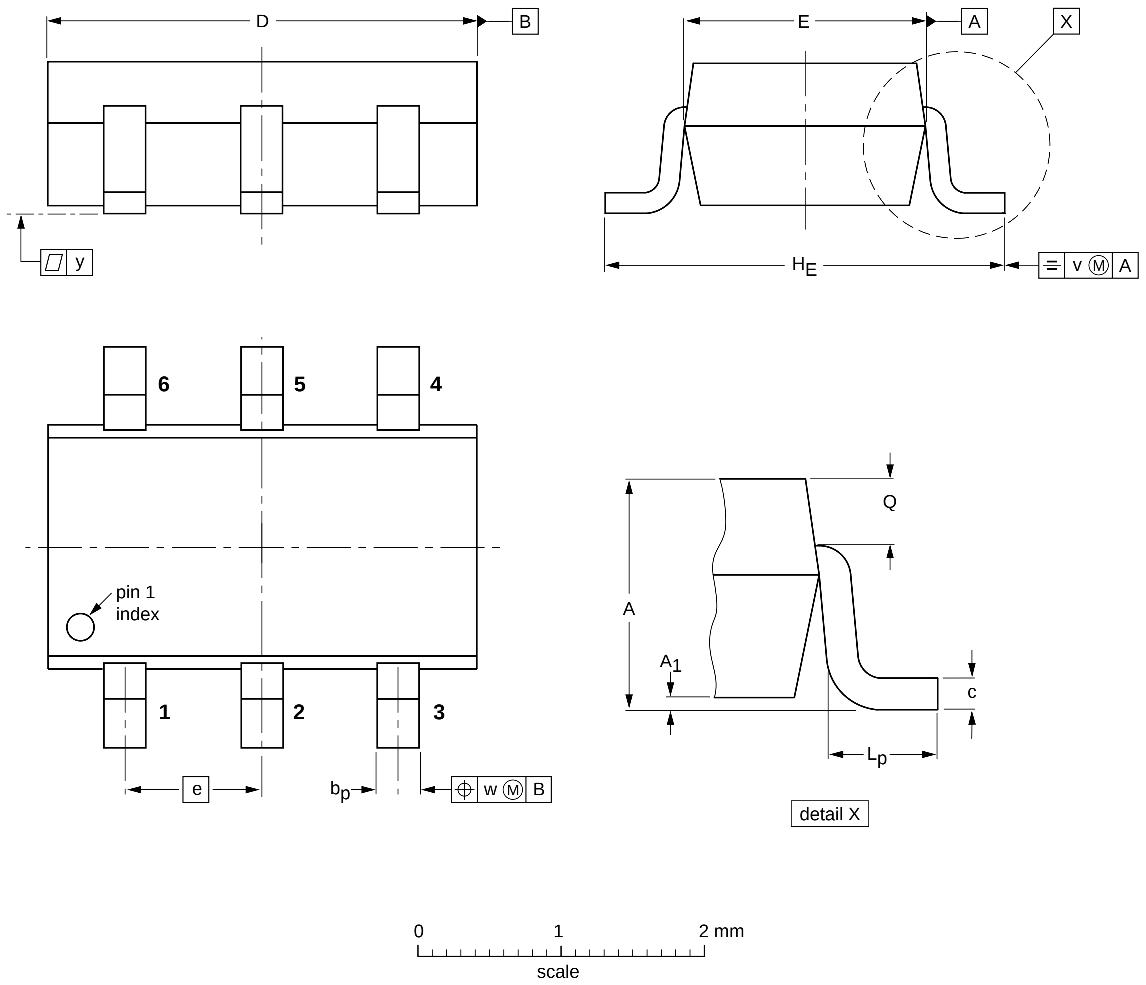
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Fig 10. Package outline SOT363 (SC-88)

Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



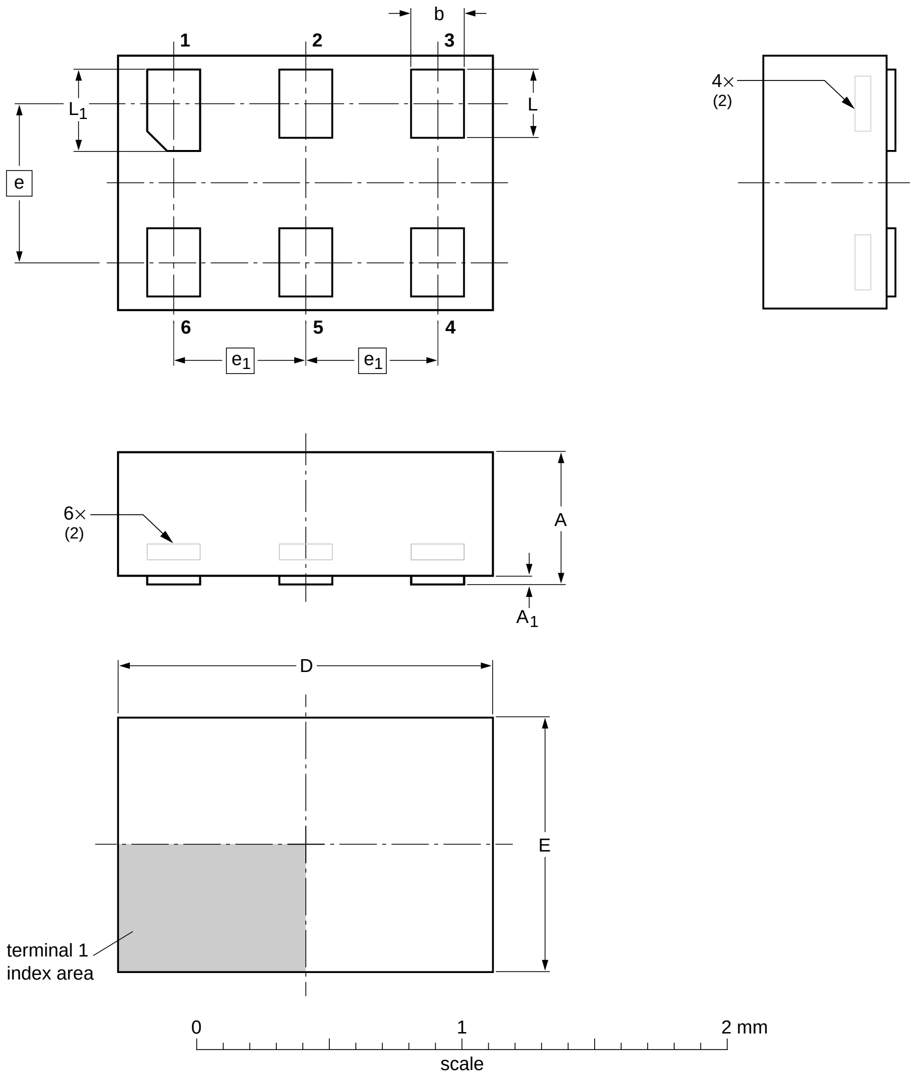
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Fig 11. Package outline SOT457 (SC-74)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A (1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

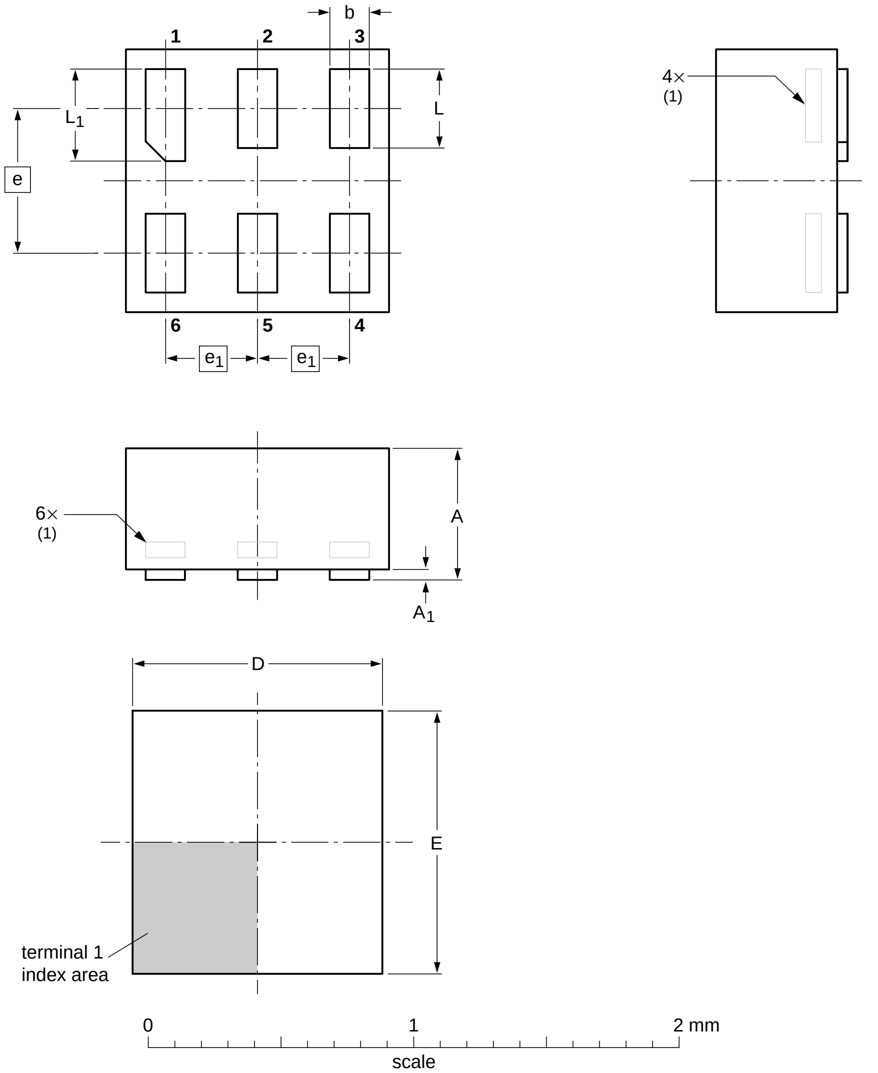
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

Fig 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm **SOT891**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

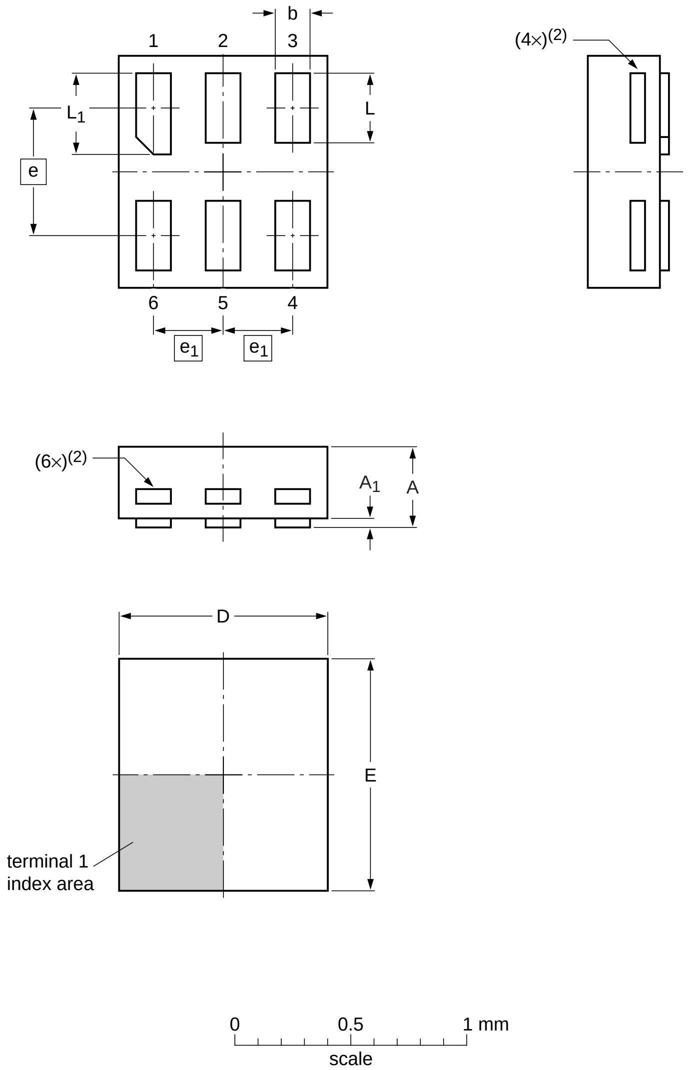
Note

1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						~~05-04-06~~ 07-05-15

Fig 13. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
mm	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

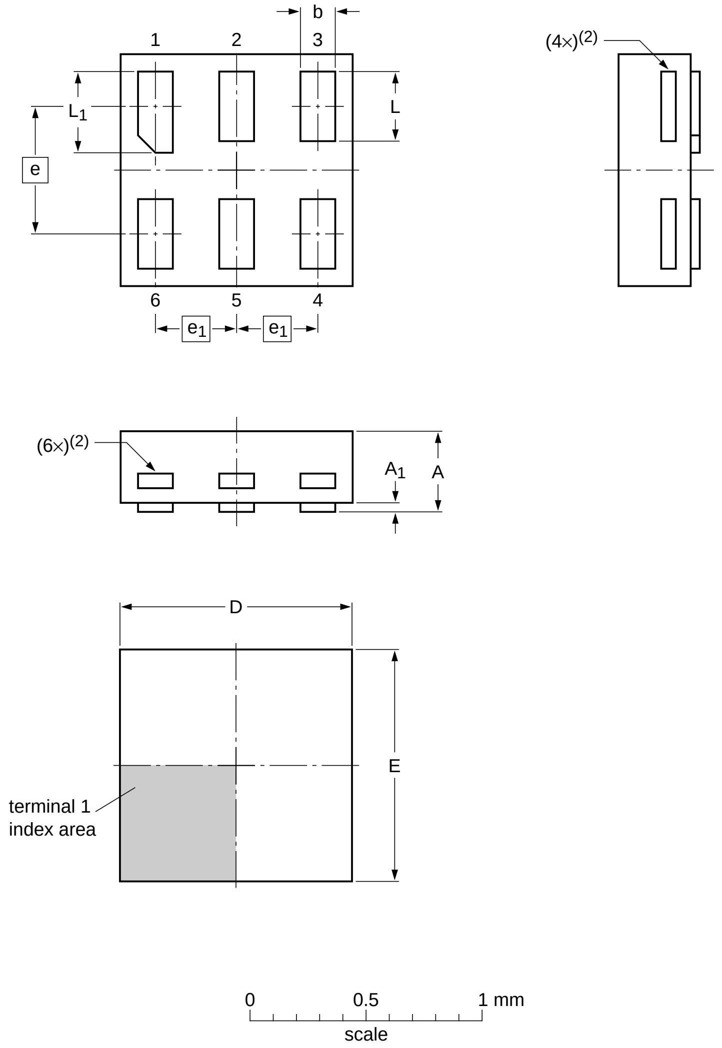
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References IEC	JEDEC	JEITA		European projection	Issue date
SOT1115						~~10-04-02~~ 10-04-07

Fig 14. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		A[1]	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
mm	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig 15. Package outline SOT1202 (XSON6)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G175 v.5	20111206	Product data sheet	-	74LVC1G175 v.4
Modifications:	• Legal pages updated.			
74LVC1G175 v.4	20101004	Product data sheet	-	74LVC1G175 v.3
74LVC1G175 v.3	20070521	Product data sheet	-	74LVC1G175 v.2
74LVC1G175 v.2	20041018	Product specification	-	74LVC1G175 v.1
74LVC1G175 v.1	20040318	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 6 December 2011

Document identifier: 74LVC1G175