

74LVC32245A

32-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Rev. 3 — 16 December 2011

Product data sheet

1. General description

The 74LVC32245A is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features four output enable ($\overline{\text{nOE}}$) inputs for easy cascading and four send/receive (nDIR) inputs for direction control. Pin $\overline{\text{nOE}}$ controls the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

To ensure the high-impedance state during power-up or power-down, pin $\overline{\text{nOE}}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 2.3 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when $V_{CC} = 0$ V
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C
- Packaged in plastic fine-pitch ball grid array package



3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|---------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LVC32245AEC | −40 °C to +125 °C | LFBGA96 | plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm | SOT536-1 |

4. Functional diagram

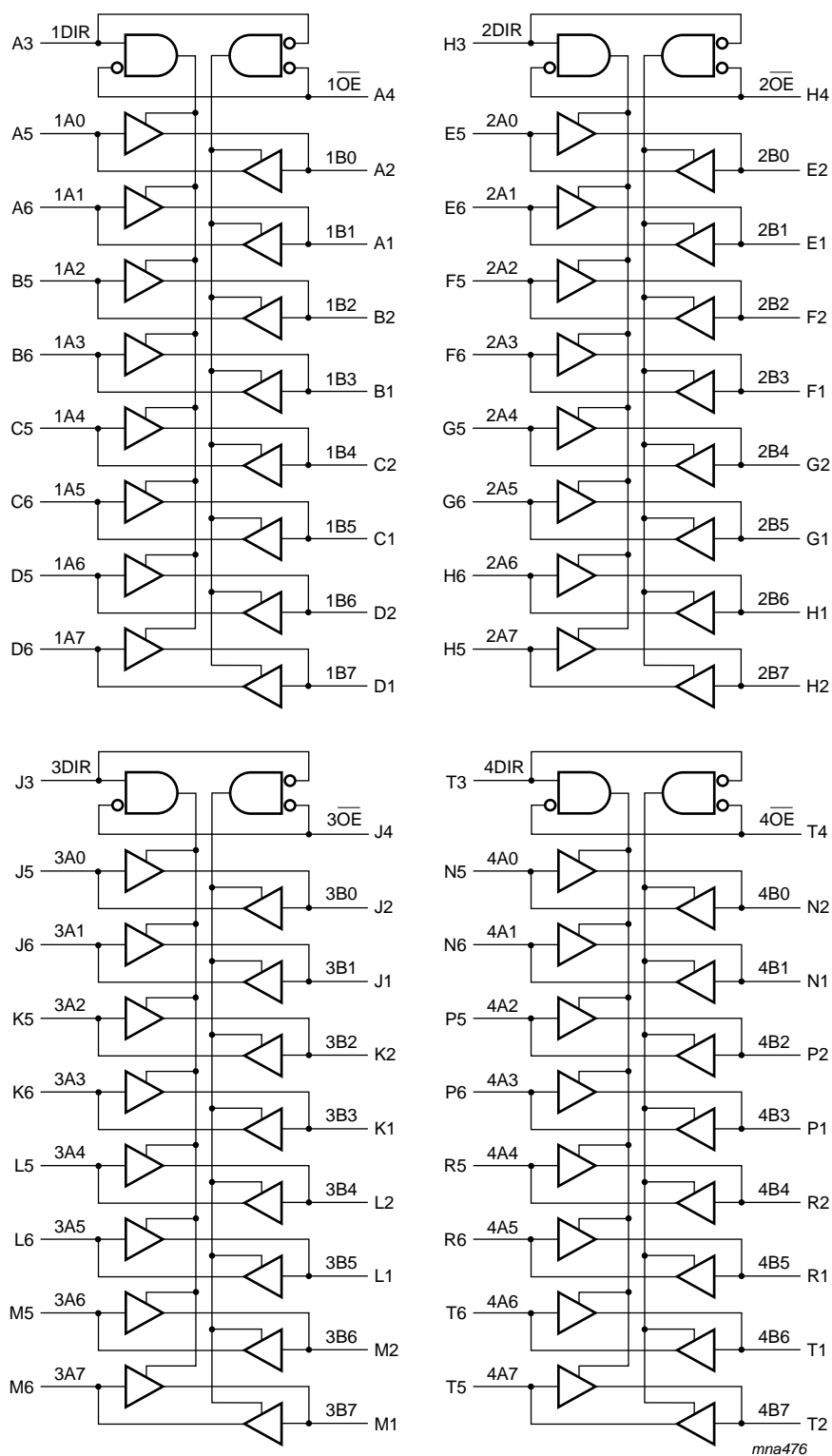


Fig 1. Logic symbol

5. Pinning information

5.1 Pinning

mna475

| | | | | | | | | | | | | | | | | |
|---|--------------------------|-----|-----------------|-----|-----|-----------------|-----|--------------------------|--------------------------|-----|-----------------|-----|-----|-----------------|-----|--------------------------|
| 6 | 1A1 | 1A3 | 1A5 | 1A7 | 2A1 | 2A3 | 2A5 | 2A6 | 3A1 | 3A3 | 3A5 | 3A7 | 4A1 | 4A3 | 4A5 | 4A6 |
| 5 | 1A0 | 1A2 | 1A4 | 1A6 | 2A0 | 2A2 | 2A4 | 2A7 | 3A0 | 3A2 | 3A4 | 3A6 | 4A0 | 4A2 | 4A4 | 4A7 |
| 4 | 1 $\overline{\text{OE}}$ | GND | V _{CC} | GND | GND | V _{CC} | GND | 2 $\overline{\text{OE}}$ | 3 $\overline{\text{OE}}$ | GND | V _{CC} | GND | GND | V _{CC} | GND | 4 $\overline{\text{OE}}$ |
| 3 | 1DIR | GND | V _{CC} | GND | GND | V _{CC} | GND | 2DIR | 3DIR | GND | V _{CC} | GND | GND | V _{CC} | GND | 4DIR |
| 2 | 1B0 | 1B2 | 1B4 | 1B6 | 2B0 | 2B2 | 2B4 | 2B7 | 3B0 | 3B2 | 3B4 | 3B6 | 4B0 | 4B2 | 4B4 | 4B7 |
| 1 | 1B1 | 1B3 | 1B5 | 1B7 | 2B1 | 2B3 | 2B5 | 2B6 | 3B1 | 3B3 | 3B5 | 3B7 | 4B1 | 4B3 | 4B5 | 4B6 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |

Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

| Symbol | Ball | Description |
|---------------------------------------|--|----------------------------------|
| nDIR (n = 1 to 4) | A3, H3, J3, T3 | direction control |
| n $\overline{\text{OE}}$ (n = 1 to 4) | A4, H4, J4, T4 | output enable input (active LOW) |
| 1A[0:7] | A5, A6, B5, B6, C5, C6, D5, D6 | input or output |
| 1B[0:7] | A2, A1, B2, B1, C2, C1, D2, D1 | input or output |
| 2A[0:7] | E5, E6, F5, F6, G5, G6, H6, H5 | input or output |
| 2B[0:7] | E2, E1, F2, F1, G2, G1, H1, H2 | input or output |
| 3A[0:7] | J5, J6, K5, K6, L5, L6, M5, M6 | input or output |
| 3B[0:7] | J2, J1, K2, K1, L2, L1, M2, M1 | input or output |
| 4A[0:7] | N5, N6, P5, P6, R5, R6, T6, T5 | input or output |
| 4B[0:7] | N2, N1, P2, P1, R2, R1, T1, T2 | input or output |
| GND | B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4 | ground (0 V) |
| V _{CC} | C3, C4, F3, F4, L3, L4, P3, P4 | supply voltage |

6. Functional description

Table 3. Function selection^[1]

| Input | | Output | |
|--------------------------|------|-----------|-----------|
| n $\overline{\text{OE}}$ | nDIR | nAn | nBn |
| L | L | nAn = nBn | inputs |
| L | H | inputs | nBn = nAn |
| H | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-------------------------------|----------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ± 50 | mA |
| V_O | output voltage | output HIGH or LOW state | [2] -0.5 | $V_{CC} + 0.5$ | V |
| | | output 3-state | [2] -0.5 | +6.5 | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ± 50 | mA |
| I_{CC} | supply current | | [3] - | 200 | mA |
| I_{GND} | ground current | | [3] -200 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [4] - | 1000 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] All supply and ground pins connected externally to one voltage source.

[4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---------------------------|------|-----|----------|------|
| V_{CC} | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | - | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | output HIGH or LOW state | 0 | - | V_{CC} | V |
| | | output 3-state | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.3$ V to 2.7 V | - | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 3.6 V | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|------------------------|--------------------|------------------------|------------------------|------------------------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | 0.65 × V _{CC} | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = –100 µA; V _{CC} = 1.65 V to 3.6 V | V _{CC} – 0.2 | - | - | V _{CC} – 0.3 | - | V |
| | | I _O = –4 mA; V _{CC} = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | I _O = –8 mA; V _{CC} = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | I _O = –12 mA; V _{CC} = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | I _O = –18 mA; V _{CC} = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| | | I _O = –24 mA; V _{CC} = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| I _I | input leakage current | V _{CC} = 3.6 V; V _I = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | µA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND; ^[2] | - | 0.1 | ±5 | - | ±20 | µA |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 5.5 V | - | 0.1 | ±10 | - | ±20 | µA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A | - | 0.1 | 40 | - | 160 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} – 0.6 V; I _O = 0 A | - | 5 | 500 | - | 5000 | µA |
| C _I | input capacitance | V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC} | - | 5.0 | - | - | - | pF |

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] For I/O ports the parameter I_{OZ} includes the input leakage current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 5](#).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|--------------------|-------------------------------|---|-------------------------------------|--------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{pd} | propagation delay | nAn to nBn; nBn to nAn; see Figure 3 ^[2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 13.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 4.8 | 10.4 | 1.5 | 12.0 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.6 | 5.4 | 1.0 | 6.1 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 2.6 | 4.7 | 1.0 | 6.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.2 | 4.5 | 1.0 | 6.0 | ns |
| t _{en} | enable time | nOE to nAn, nBn; see Figure 4 ^[2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 15.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 5.8 | 12.5 | 1.5 | 14.4 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.3 | 6.9 | 1.0 | 8.0 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 3.4 | 6.7 | 1.5 | 8.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.7 | 5.5 | 1.0 | 7.0 | ns |
| t _{dis} | disable time | nOE to nAn, nBn; see Figure 4 ^[2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 11.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 4.4 | 9.7 | 1.0 | 11.2 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 2.5 | 5.5 | 0.5 | 6.5 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 2.5 | 6.6 | 1.5 | 8.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.1 | 5.6 | 1.5 | 7.0 | ns |
| t _{sk(o)} | output skew time | V _{CC} = 3.0 V to 3.6 V ^[3] | - | - | 1.0 | - | 1.5 | ns |
| C _{PD} | power dissipation capacitance | per buffer; V _I = GND to V _{CC} ^[4] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | - | 11.5 | - | - | - | pF |
| | | V _{CC} = 2.3 V to 2.7 V | - | 15.2 | - | - | - | pF |
| | | V _{CC} = 3.0 V to 3.6 V | - | 18.5 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

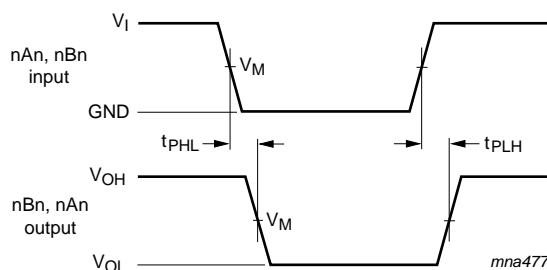
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

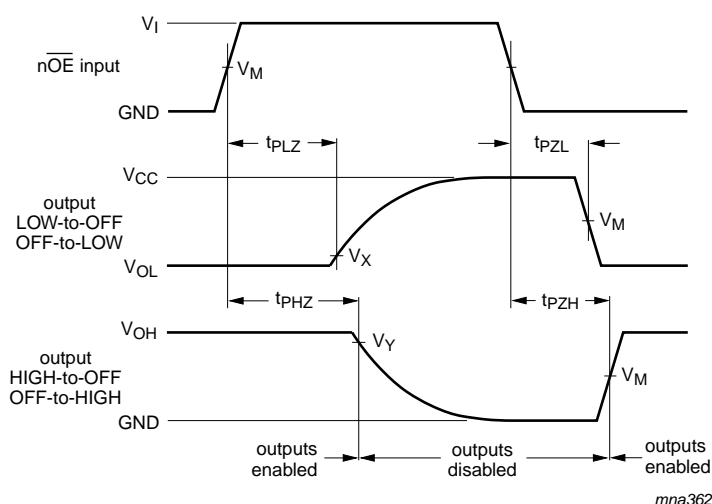
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms


$$V_M = 1.5 \text{ V at } V_{CC} \geq 2.7 \text{ V.}$$
$$V_M = 0.5 \times V_{CC} \text{ at } V_{CC} < 2.7 \text{ V.}$$

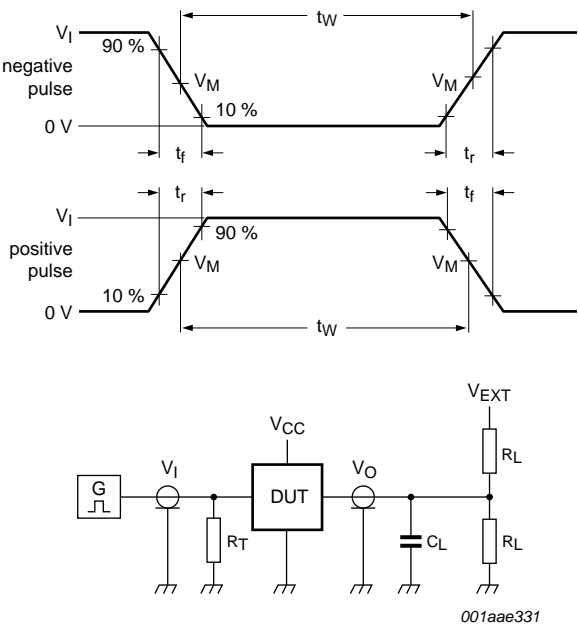
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 3. The input (nAn, nBn) to output (nBn, nAn) propagation delays

 $V_M = 1.5 \text{ V at } V_{CC} \geq 2.7 \text{ V.}$
$$V_M = 0.5 \times V_{CC} \text{ at } V_{CC} < 2.7 \text{ V.}$$
$$V_X = V_{OL} + 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V;}$$
$$V_X = V_{OL} + 0.15 \text{ V at } V_{CC} < 2.7 \text{ V.}$$
$$V_Y = V_{OH} - 0.3 \text{ V at } V_{CC} \geq 2.7 \text{ V;}$$
$$V_Y = V_{OH} - 0.15 \text{ V at } V_{CC} < 2.7 \text{ V.}$$

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. 3-state enable and disable times.



Test data is given in [Table 8](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 5. Load circuitry for switching times

Table 8. Test data

| Supply voltage | Input | | Load | | V _{EXT} | | |
|------------------|-----------------|---------------------------------|----------------|----------------|-------------------------------------|-------------------------------------|-------------------------------------|
| | V _I | t _r , t _f | C _L | R _L | t _{PLH} , t _{PHL} | t _{PLZ} , t _{PZL} | t _{PHZ} , t _{PZH} |
| 1.2 V | V _{CC} | ≤ 2 ns | 30 pF | 1 kΩ | open | 2 × V _{CC} | GND |
| 1.65 V to 1.95 V | V _{CC} | ≤ 2 ns | 30 pF | 1 kΩ | open | 2 × V _{CC} | GND |
| 2.3 V to 2.7 V | V _{CC} | ≤ 2 ns | 30 pF | 500 Ω | open | 2 × V _{CC} | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 2 × V _{CC} | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 2 × V _{CC} | GND |

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

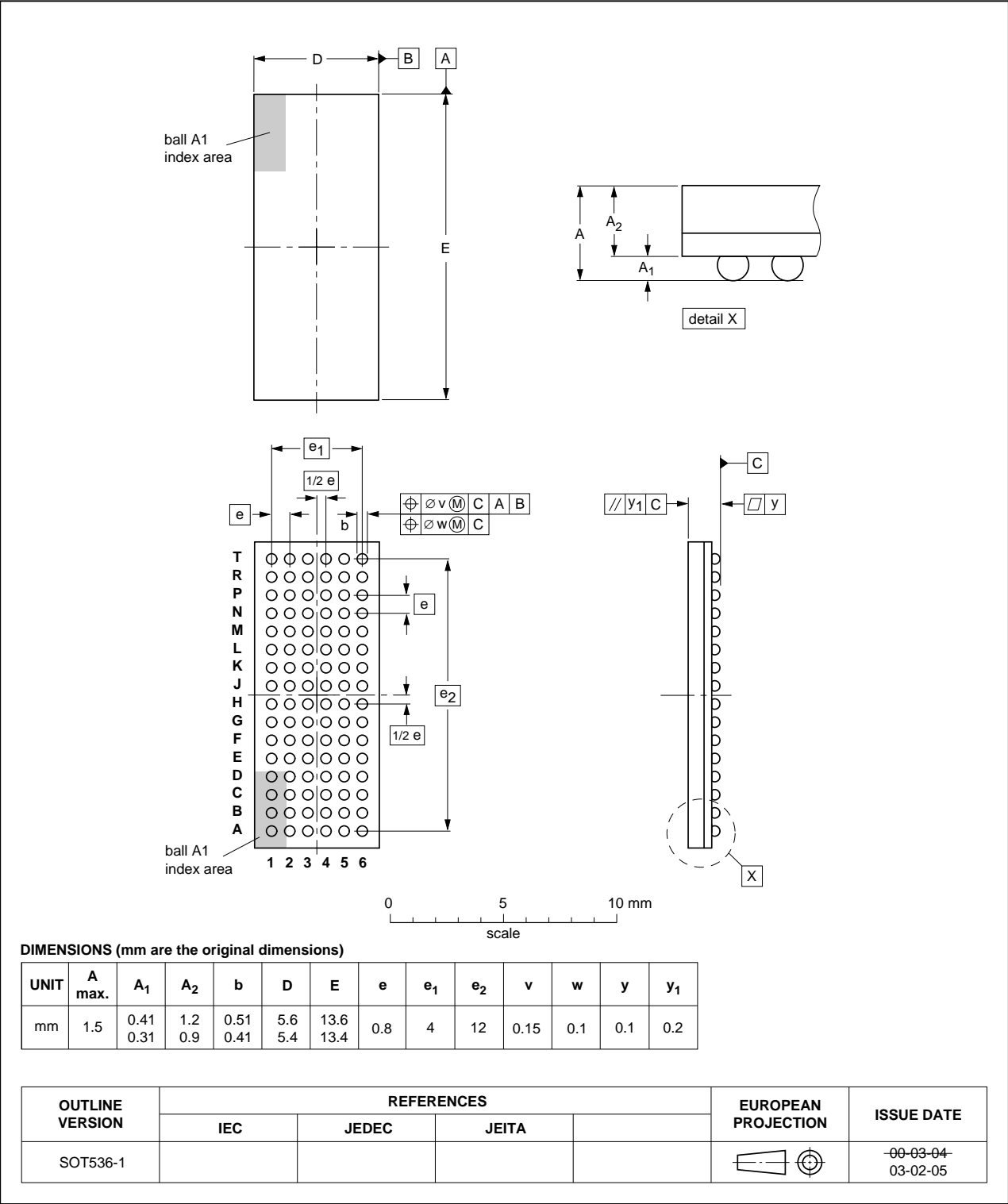


Fig 6. Package outline SOT536-1 (LFBGA96)

13. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|-----------------------------|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|---|-----------------------|---------------|-----------------|
| 74LVC32245A v.3 | 20111216 | Product data sheet | - | 74LVC32245A v.2 |
| Modifications: | <ul style="list-style-type: none">Maximum propagation delay value for $V_{CC} = 1.65\text{ V}$ to 1.95 V at $+125\text{ }^{\circ}\text{C}$ changed from 11.7 ns to 12.0 nsMaximum enable time value for $V_{CC} = 1.65\text{ V}$ to 1.95 V at $+125\text{ }^{\circ}\text{C}$ changed from 14.3 ns to 14.4 ns | | | |
| 74LVC32245A v.2 | 20111108 | Product data sheet | - | 74LVC32245A v.1 |
| Modifications: | <ul style="list-style-type: none">The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate.Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. | | | |
| 74LVC32245A v.1 | 19990901 | Product Specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Ordering information | 2 |
| 4 | Functional diagram | 3 |
| 5 | Pinning information | 4 |
| 5.1 | Pinning | 4 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 4 |
| 7 | Limiting values | 5 |
| 8 | Recommended operating conditions | 5 |
| 9 | Static characteristics | 6 |
| 10 | Dynamic characteristics | 7 |
| 11 | Waveforms | 8 |
| 12 | Package outline | 10 |
| 13 | Abbreviations | 11 |
| 14 | Revision history | 11 |
| 15 | Legal information | 12 |
| 15.1 | Data sheet status | 12 |
| 15.2 | Definitions | 12 |
| 15.3 | Disclaimers | 12 |
| 15.4 | Trademarks | 13 |
| 16 | Contact information | 13 |
| 17 | Contents | 14 |

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