

LMV932 DUAL, LMV934 QUAD LMV931 SINGLE

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1.8-V OPERATIONAL AMPLIFIERS WITH RAIL-TO-RAIL INPUT AND OUTPUT

Check for Samples: LMV932 DUAL, LMV934 QUAD, LMV931 SINGLE

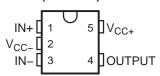
FEATURES

- 1.8-V, 2.7-V, and 5-V Specifications
- Rail-to-Rail Output Swing
 - 600- Ω Load . . . 80 mV From Rail
 - 2-kΩ Load . . . 30 mV From Rail
- V_{ICR} . . . 200 mV Beyond Rails
- Gain Bandwidth . . . 1.4 MHz
- Supply Current . . . 100 μA/Amplifier
- Max V_{IO} . . . 4 mV
- Space-Saving Packages
 - LMV931: SOT-23 and SC-70
 - LMV932: MSOP and SOIC
 - LMV934: SOIC and TSSOP

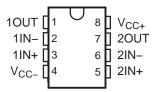
APPLICATIONS

- Industrial (Utility/Energy Metering)
- Automotive
- Communications (Optical Telecom, Data/Voice Cable Modems)
- Consumer Electronics (PDAs, PCs, CDR/W, Portable Audio)
- Supply-Current Monitoring
- Battery Monitoring

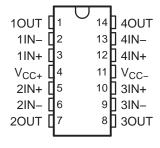
LMV931...DBV (SOT-23-5) OR DCK (SC-70) PACKAGE (TOP VIEW)



LMV932...D (SOIC) OR DGK (VSSOP/MSOP) PACKAGE (TOP VIEW)



LMV934...D (SOIC) OR PW (TSSOP) PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

INSTRUMENTS

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ORDERING INFORMATION

T _A		PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING (2)
		SOT-23 – DBV	Reel of 3000	LMV931IDBVR	RBB_
	Cinala	301-23 – DBV	Reel of 250	LMV931IDBVT	PREVIEW
	Single	Single Reel of 3000 LMV	LMV931IDCKR	RB_	
		30-70 - DCK	Reel of 250	LMV931IDCKT	PREVIEW
	Duol	MSOP/VSSOP – DGK	Reel of 2500	LMV932IDGKR	RD_
–40°C to 125°C		W30P/V330P - DGK	Reel of 250	LMV932IDGKT	PREVIEW
-40°C to 125°C	Dual	SOIC – D	Tube of 75	LMV932ID	MV932I
		201C - D	Reel of 2500	LMV932IDR	WIV932I
		SOIC – D	Tube of 50	LMV934ID	LMV934I
	Quad	301C - D	Reel of 2500	LMV934IDR	LIVI V 9341
	Quad	TSSOP – PW	Tube of 90	LMV934IPW	MV934I
		1330P – PW	Reel of 2000	LMV934IPWR	WV934I

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The LMV93x devices are low-voltage low-power operational amplifiers that are well suited for today's low-voltage and/or portable applications. Specified for operation of 1.8 V to 5 V, they can be used in portable applications that are powered from a single-cell Li-ion or two-cell batteries. They have rail-to-rail input and output capability for maximum signal swings in low-voltage applications. The LMV93x input common-mode voltage extends 200 mV beyond the rails for increased flexibility. The output can swing rail-to-rail unloaded and typically can reach 80 mV from the rails, while driving a $600-\Omega$ load (at 1.8-V operation).

During 1.8-V operation, the devices typically consume a quiescent current of 103 µA per channel, and yet they are able to achieve excellent electrical specifications, such as 101-dB open-loop DC gain and 1.4-MHz gain bandwidth. Furthermore, the amplifiers offer good output drive characteristics, with the ability to drive a 600-Ω load and 1000-pF capacitance with minimal ringing.

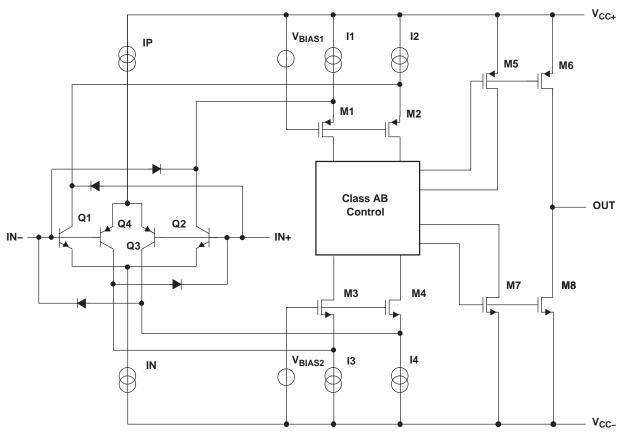
The LMV93x devices are offered in the latest packaging technology to meet the most demanding spaceconstraint applications. The LMV931 is offered in standard SOT-23 and SC-70 packages. The LMV932 is available in the traditional MSOP and SOIC packages. The LMV934 is available in the traditional SOIC and TSSOP packages.

The LMV93x devices are characterized for operation from -40°C to 125°C, making the part universally suited for commercial, industrial, and automotive applications.

DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.



Figure 1. SIMPLIFIED SCHEMATIC



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Absolute Maximum Ratings(1)

over free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC+} - V _{CC-}	Supply voltage ⁽²⁾			5.5	V
V_{ID}	Differential input voltage (3)		Supply vo	ltage	
VI	Input voltage range, either input		V _{CC} 0.2	V _{CC+} + 0.2	V
	Duration of output short circuit (one ampl	lifier) to V _{CC±} (4) (5)	Unlimit	ed	
		D package (8 pin)		97	
		D package (14 pin)		86	
0	Deckage thermal impedance (5) (6)	DBV package		206	°C/W
OJA	Package thermal impedance (5) (6)	DCK package		5.5 bltage V _{CC+} + 0.2 ted 97	· C/vv
		DGK package		172	
		PW package		113	
TJ	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.
- (5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage (V _{CC+} – V _{CC})	1.8	5	V
T _A	Operating free-air temperature	-40	125	°C

ESD Protection

	TYP	UNIT
Human-Body Model	2000	V
Machine Model	200	V

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Electrical Characteristics

 $V_{CC+} = 1.8 \text{ V}, \ V_{CC-} = 0 \ \underline{\text{V}}, \ V_{IC} = V_{CC+}/2, \ V_O = V_{CC+}/2, \ \text{and} \ R_L > 1 \ \text{M}\Omega \ \text{(unless otherwise noted)}$

	PARAMETE	R	TEST COND	ITIONS	T _A	MIN	TYP	MAX	UNIT
			LMV931 (single)		25°C		1	4	
,	Input offset v	oltogo	Liviv931 (Sirigle)		Full range			6	mV
/ _{IO}	iliput oliset v	ollage	LMV932 (dual), LMV93	R4 (guad)	25°C		1	5.5	IIIV
			LIVIV932 (dual), LIVIV93	54 (quau)	Full range			7.5	
$\alpha_{V_{IO}}$	Average temposers coefficient of offset voltage	input			25°C		5.5		μV/°C
			$V_{IC} = V_{CC+} - 0.8 \text{ V}$		25°C		15	35	
IB	Input bias cu	rrent			25°C			65	nA
					Full range			75	
	Input offset c	urrent			25°C		13	25	nA
Ю	input onset c	unem			Full range			40	ПА
	Supply curre				25°C		103	185	μA
СС	(per channel))			Full range			205	μΑ
					25°C	60	78		-
CMRR	Common-mo	de	$0 \le V_{IC} \le 0.6 \text{ V}, 1.4 \text{ V}$	5 V, 1.4 V ≤ V _{IC} ≤ 1.8 V		55			٩D
JIVIKK	rejection ratio		0.2 ≤ V _{IC} ≤ 0.6 V, 1.4 V	/ ≤ V _{IC} ≤ 1.6 V	-40°C to 125°C	55			dB
			$-0.2 \le V_{IC} \le 0 \text{ V}, 1.8 \text{ V}$	′ ≤ V _{IC} ≤ 2 V	25°C	50	72		
	Supply-voltage	ge	101/21/25/11/	0.5.1/	25°C	75	100		40
SVR	rejection ratio	Ó	$1.8 \text{ V} \le \text{V}_{\text{CC+}} \le 5 \text{ V}, \text{ V}_{\text{IC}}$	_C = 0.5 V	Full range	70			dB
					25°C	V _{CC} 0.2	-0.2 to 2.1	V _{CC+} + 0.2	
Common-mode input voltage ran		CMRR ≥ 50 dB		-40°C to 85°C	V _{CC} -		V _{CC+}	٧	
	input voltage	range			-40°C to 125°C	V _{CC} -+ 0.2		V _{CC+} - 0.2	
				$R_L = 600 \Omega$	25°C	77	101		
		1.843/004		$to^{L}0.9 \text{ V}$ $R_{L} = 2 \text{ k}\Omega$	Full range	73			
		LMV931			25°C	80	105		
	Large-signal		$V_O = 0.2 \text{ V to } 1.6 \text{ V},$	to 0.9 V	Full range	75			-ID
A_{\bigvee}	voltage gain		V _{IC} = 0.5 V	$R_L = 600 \Omega$	25°C	75	90		dB
		LMV932,		to 0.9 V	Full range	72			
		LMV934		$R_L = 2 k\Omega$	25°C	78	100		
				to 0.9 V	Full range	75			
				Lligh lovel	25°C	1.65	1.72		
			$R_1 = 600 \Omega \text{ to } 0.9 \text{ V},$	High level	Full range	1.63			
			$V_{ID}^{L} = \pm 100 \text{ mV}$	Low level	25°C		0.077	0.105	
,	Ott			Low level	Full range			0.120	1/
/ ₀	Output swing			Liber level	25°C	1.75	1.77		V
			$R_L = 2 k\Omega$ to 0.9 V,	High level	Full range	1.74			
			$V_{ID} = \pm 100 \text{ mV}$	Lauriana.	25°C		0.024	0.035	
				Low level	Full range			0.040	
			$V_O = 0 V$,	Course	25°C	4	8		
	Output short-	circuit	$V_{ID} = 100 \text{ mV}$	Sourcing	Full range	3.3			mA
os	current		V _O = 1.8 V,	Sinking	25°C	7	9		
			$V_{O} = 1.8 \text{ V},$ $V_{ID} = -100 \text{ mV}$ Sir		Full range	5			
GBW	Gain bandwidth				25°C		1.4		MHz

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Electrical Characteristics (continued)

 $\underline{V_{CC+}} = 1.8 \text{ V}, \ V_{CC-} = 0 \text{ V}, \ V_{IC} = V_{CC+}/2, \ V_O = V_{CC+}/2, \ \text{and} \ R_L > 1 \ \text{M}\Omega \ \text{(unless otherwise noted)}$

	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
SR	Slew rate ⁽¹⁾		25°C		0.35		V/µS
Φ_{m}	Phase margin		25°C		67		0
	Gain margin		25°C		7		dB
V_n	Equivalent input noise voltage	f = 1 kHz, V _{IC} = 0.5 V	25°C		60		nV/√ Hz
I _n	Equivalent input noise current	f = 1 kHz	25°C		0.06		pA/√ Hz
THD	Total harmonic distortion	$f = 1 \text{ kHz}, A_V = 1, R_L = 600 \Omega, \ V_{ID} = 1 V_{p-p}$	25°C		0.023		%
	Amplifier-to-amplifier isolation (2)		25°C		123		dB

⁽¹⁾ Number specified is the slower of the positive and negative slew rates.

 ⁽²⁾ Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

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Electrical Characteristics

 V_{CC+} = 2.7 V, V_{CC-} = 0 V, V_{IC} = $V_{CC+}/2$, V_O = $V_{CC+}/2$, and R_L > 1 M Ω (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T _A	MIN	TYP	MAX	UNIT
			LMV931 (single)		25°C		1	4	
V	Input offset vo	ltage	LIVIV 301 (SILIGIE)		Full range			6	mV
V _{IO}	iiiput oliset VO	lage	LMV932 (dual), LMV93	34 (auad)	25°C		1	5.5	1117
			LIVIV932 (dual), LIVIV93	34 (quau)	Full range			7.5	
$\alpha_{V_{10}}$	Average tempo coefficient of in offset voltage				25°C		5.5		μV/°C
			$V_{IC} = V_{CC+} - 0.8 \text{ V}$	25°C		15	35		
I_{IB}	Input bias curr	ent			25°C			65	nA
					Full range			75	
I _{IO}	Input offset cu	rrent			25°C		8	25	nA
'IO	input onset ou	TICHE			Full range			40	ш
	Supply current				25°C		105	190	μΑ
I _{CC}	(per channel)				Full range			210	μΛ
					25°C	60	81		
CMRR	Common-mod	е	$0 \le V_{IC} \le 1.5 \text{ V}, 2.3 \text{ V}$	≤ V _{IC} ≤ 2.7 V	–40°C to 85°C	55			dB
CIVIKK	ejection ratio		0.2 ≤ V _{IC} ≤ 1.5 V, 2.3 V	–40°C to 125°C	55			uБ	
			$-0.2 \le V_{IC} \le 0 \text{ V}, 2.7 \text{ V}$	$V \le V_{IC} \le 2.9 \text{ V}$	25°C	50	74		
اما	Supply-voltage)	1.8 V ≤ V _{CC+} ≤ 5 V, V _I	- 0 5 V	25°C	75	100		dB
k _{SVR}	rejection ratio		1.0 V = V _{CC+} = 5 V, V _{[0}	C = 0.3 V	Full range	70			uБ
					25°C	V _{CC} 0.2	-0.2 to 3	$V_{CC+} + 0.2$	
	Common-mode input voltage range		CMRR ≥ 50 dB		-40°C to 85°C	V _{CC} -		V _{CC+}	٧
				-40°C to 125°C	V _{CC} - + 0.2		V _{CC+} – 0.2		
		LMV931		$R_L = 600 \Omega$	25°C	87	104		
				to 1.35 V $R_L = 2 k\Omega$ to 1.35 V	Full range	86			
					25°C	92	110		
۸	Large-signal		V _O = 0.2 V to 2.5 V		Full range	91			dB
A_{V}	voltage gain		V ₀ = 0.2 V to 2.3 V	$R_L = 600 \Omega$	25°C	78	90		uБ
		LMV932,		to 1.35 V	Full range	75			
		LMV934		$R_L = 2 k\Omega$	25°C	81	100		
				to 1.35 V	Full range	78			
				High level	25°C	2.55	2.62		
			$R_L = 600 \Omega \text{ to } 1.35 \text{ V},$	i ligit level	Full range	2.53			
			$V_{ID} = \pm 100 \text{ mV}$	Low level	25°C		0.083	0.11	
\/_	Output swing			LOW IEVEI	Full range			0.13	V
Vo	Output Swilig			High level	25°C	2.65	2.675		V
			$R_L = 2 k\Omega \text{ to } 1.35 \text{ V},$	i ligit level	Full range	2.64			
			$V_{ID} = \pm 100 \text{ mV}$	Low level	25°C		0.025	0.04	İ
				LOW IEVEI	Full range			0.045	
			V _O = 0 V,	Sourcina	25°C	20	30		
laa	Output short-c	ircuit	V _{ID} = 100 mV	Sourcing	Full range	15			
100	current		$V_O = 2.7 \text{ V},$ Sinking		25°C	18	25		mA -
					Full range	12			
GBW	Gain bandwidt	ndwidth product		25°C		1.4		MHz	

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Electrical Characteristics (continued)

 $V_{CC+} = 2.7 \text{ V}, \ V_{CC-} = 0 \text{ V}, \ V_{IC} = V_{CC+}/2, \ V_O = V_{CC+}/2, \ \text{and} \ R_L > 1 \ \text{M}\Omega \ \text{(unless otherwise noted)}$

	PARAMETER	TEST CONDITIONS	T _A	MIN TYP	MAX	UNIT
SR	Slew rate ⁽¹⁾		25°C	0.4		V/µS
Φ_{m}	Phase margin		25°C	70		0
	Gain margin		25°C	7.5		dB
V _n	Equivalent input noise voltage	f = 1 kHz, V _{IC} = 0.5 V	25°C	57		nV/√ Hz
In	Equivalent input noise current	f = 1 kHz	25°C	0.082		pA/√ Hz
THD	Total harmonic distortion	$ f = 1 \text{ kHz}, \ A_V = 1, \ R_L = 600 \ \Omega, $ $V_{ID} = 1 \ V_{p\text{-}p} $	25°C	0.022		%
	Amplifier-to-amplifier isolation (2)		25°C	123		dB

⁽¹⁾ Number specified is the slower of the positive and negative slew rates.

⁽²⁾ Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce V_O = 3 V_{p-p}.

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Electrical Characteristics

 $V_{CC+} = 5 \text{ V}, \ V_{CC-} = 0 \text{ V}, \ V_{IC} = V_{CC+}/2, \ V_O = V_{CC+}/2, \ \text{and} \ R_L > 1 \ \text{M}\Omega \ \text{(unless otherwise noted)}$

	PARAMETER	₹	TEST CONDI	TIONS	T _A	MIN	TYP	MAX	UNIT
			LM\(024 (single)		25°C		1	4	
\ /	lament affact	-14	LMV931 (single)		Full range			6	\/
V_{IO}	Input offset v	oitage	LM\(000 (dd\) LM\(00	24 (25°C		1	5.5	mV
			LMV932 (dual), LMV93	34 (quad)	Full range			7.5	
$\alpha_{V_{\text{IO}}}$	Average temposers coefficient of offset voltage	input			25°C		5.5		μV/°C
			$V_{IC} = V_{CC+} - 0.8 \text{ V}$		25°C		15	35	
I_{IB}	Input bias cu	rrent			25°C			65	nA
					Full range			75	
l.a	Input offset c	urrent			25°C		9	25	nA
I _{IO}	input onset c	ullelit			Full range			40	ПА
laa	Supply currer				25°C		116	210	μΑ
I _{CC}	(per channel)				Full range			230	μΛ
					25°C	60	86		
	Common-mo	مام	$0 \le V_{IC} \le 3.8 \text{ V}, 4.6 \text{ V}$	≤ V _{IC} ≤ 5 V	-40°C to 85°C	55			
CMRR	mrrejection ratio		0.3 ≤ V _{IC} ≤ 3.8 V, 4.6 V	/ ≤ V _{IC} ≤ 4.7 V	-40°C to	55			dB
			-0.2 ≤ V _{IC} ≤ 0 V, 5 V ≤		25°C	50	78		
	Supply-voltag	ie	$1.8 \text{ V} \le \text{V}_{\text{CC+}} \le 5 \text{ V}, \text{V}_{\text{IC}} = 0.5 \text{ V}$		25°C	75	100		i.
k _{SVR}	rejection ratio		$1.8 \text{ V} \le \text{V}_{CC+} \le 5 \text{ V}, \text{ V}_{IC}$	$_{\rm C} = 0.5 \text{ V}$	Full range	70			dB
					25°C	V _{CC} 0.2	-0.2 to 5.3	V _{CC+} + 0.2	
V	Common-mo	de input	CMRR ≥ 50 dB		-40°C to 85°C	V _{CC} -		V _{CC+}	V
VICR	ICR voltage range)	CIVILITY 2 30 UB	-40°C to	V _{CC} - + 0.3		V _{CC+} - 0.3	V	
		LMV931		R _L = 600 Ω	25°C	88	102		
				$R_L = 000 \Omega$ to 2.5 V $R_L = 2 k\Omega$	Full range	87			
					25°C	94	113		
	Large-signal			to 2.5 V	Full range	93			
A_V	voltage gain		$V_0 = 0.2 \text{ V to } 4.8 \text{ V}$	R _L = 600 Ω	25°C	81	90		dB
		LMV932,		$R_L = 600 \Omega$ to 2.5 V	Full range	78			
		LMV934		$R_L = 2 k\Omega$	25°C	85	100		
				to 2.5 V	Full range	82			
					25°C	4.855	4.89		
			$R_L = 600 \Omega \text{ to } 2.5 \text{ V},$	High level	Full range	4.835			
			$V_{ID} = \pm 100 \text{ mV}$		25°C		0.12	0.16	
				Low level	Full range			0.18	
Vo	Output swing				25°C	4.945	4.967		V
			$R_L = 2 k\Omega$ to 2.5 V,	High level	Full range	4.935			
			$V_{ID} = \pm 100 \text{ mV}$		25°C		0.037	0.065	
				Low level	Full range			0.075	
			V _O = 0 V,		25°C	80	100		
	Output short-	circuit	$V_{ID} = 100 \text{ mV}$	Sourcing	Full range	68			mA
os	current	J. J Guil	$V_0 = 5 \text{ V}$, Sinking		25°C	58	65		
				Full range	45				
GBW	Gain bandwid	dth			25°C		1.5		MHz

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Electrical Characteristics (continued)

 $V_{CC+} = 5~V,~V_{CC-} = 0~V,~V_{IC} = V_{CC+}/2,~V_O = V_{CC+}/2,~\text{and}~R_L > 1~M\Omega~\text{(unless otherwise noted)}$

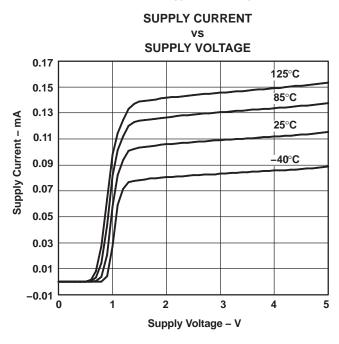
	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
SR	Slew rate ⁽¹⁾		25°C		0.42		V/µS
Фт	Phase margin		25°C		71		0
	Gain margin		25°C		8		dB
V _n	Equivalent input noise voltage	f = 1 kHz, V _{IC} = 0.5 V	25°C		50		nV/√ Hz
In	Equivalent input noise current	f = 1 kHz	25°C		0.07		pA/√ Hz
THD	Total harmonic distortion	$f = 1 \text{ kHz}, A_V = 1, R_L = 600 \Omega,$ $V_{ID} = 1 V_{p-p}$	25°C		0.022		%
	Amplifier-to-amplifier isolation (2)		25°C		123		dB

 ⁽¹⁾ Number specified is the slower of the positive and negative slew rates.
 (2) Input referred, V_{CC+} = 5 V and R_L = 100 kΩ connected to 2.5 V. Each amplifier is excited, in turn, with a 1-kHz signal to produce $V_{O} = 3 V_{p-p}$.



TYPICAL CHARACTERISTICS

 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)



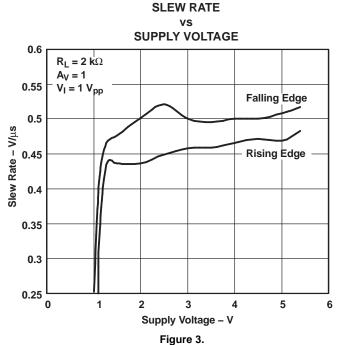
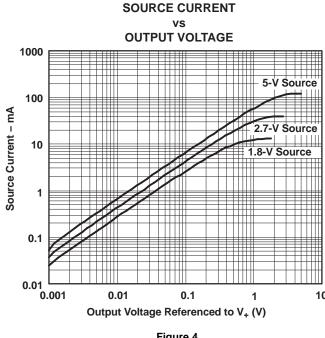


Figure 2.



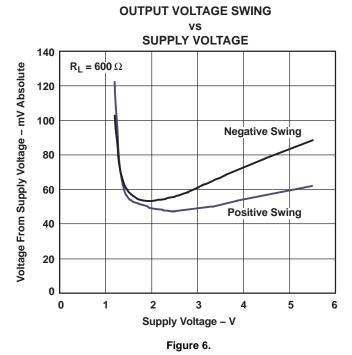
SINK CURRENT OUTPUT VOLTAGE 1000 5-V Sink 100 Sink Current - mA 10 1 0.1 0.01 0.001 0.01 0.1 10 Output Voltage Referenced to V- (V)

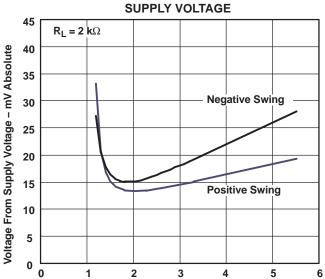
Figure 5.

Figure 4.



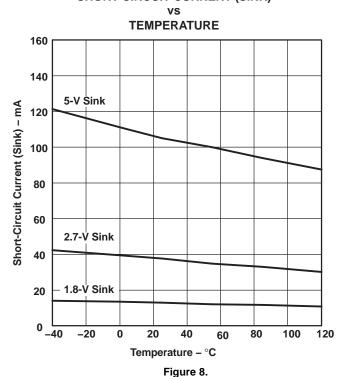
 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)





OUTPUT VOLTAGE SWING

SHORT-CIRCUIT CURRENT (SINK)



SHORT-CIRCUIT CURRENT (SOURCE)

Supply Voltage – V Figure 7.

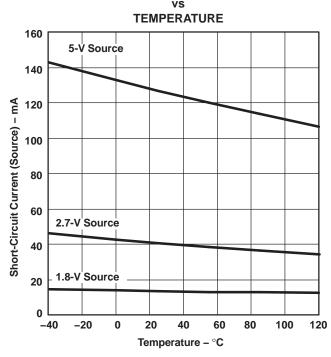


Figure 9.



 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)

1.8-V FREQUENCY RESPONSE

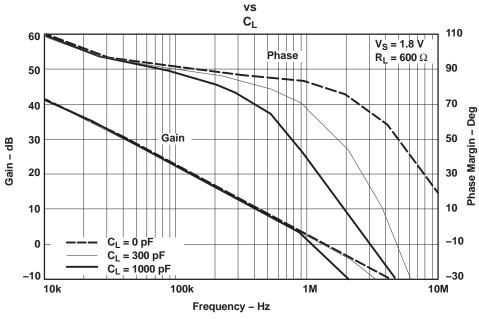


Figure 10.

5-V FREQUENCY RESPONSE

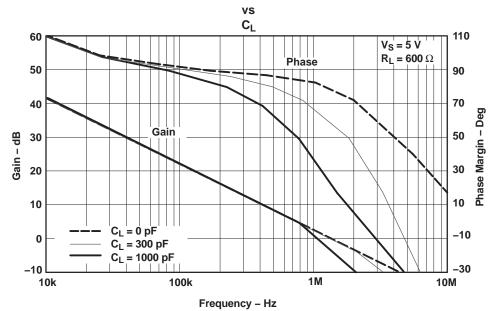
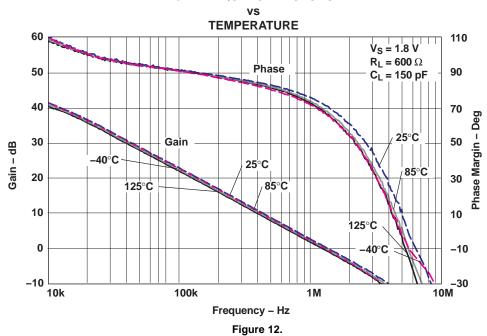


Figure 11.



 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)

1.8-V FREQUENCY RESPONSE



5-V FREQUENCY RESPONSE

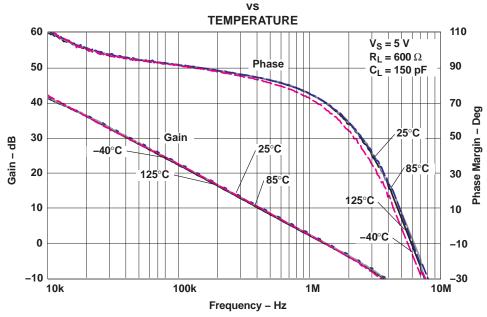


Figure 13.

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TYPICAL CHARACTERISTICS (continued)

 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)

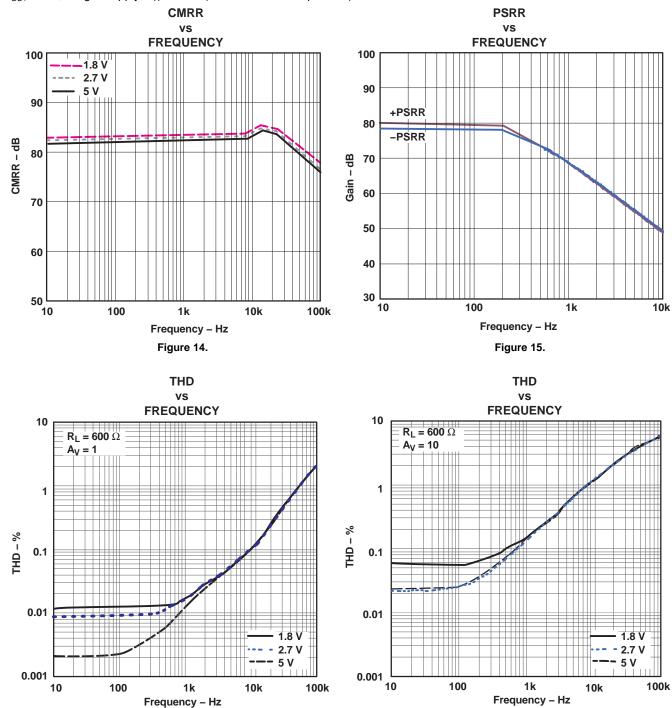
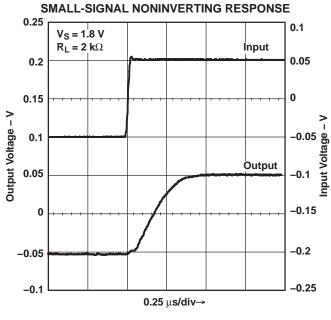


Figure 16.

Figure 17.



 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)





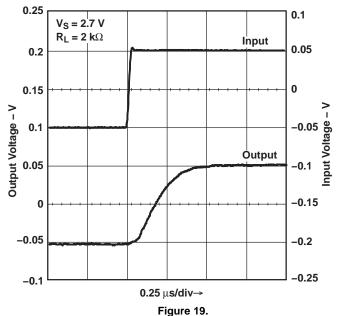


Figure 18.



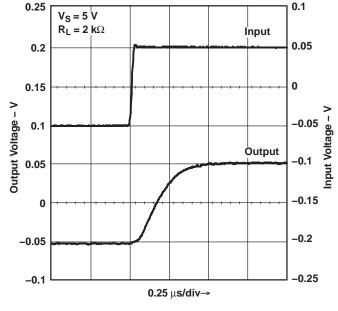


Figure 20.

LARGE-SIGNAL NONINVERTING RESPONSE

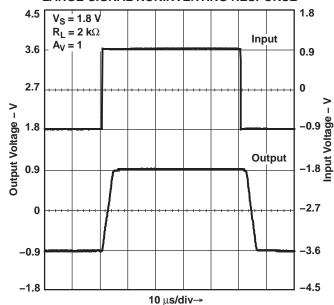


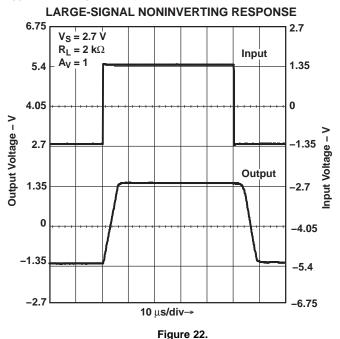
Figure 21.

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TYPICAL CHARACTERISTICS (continued)

 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)



LARGE-SIGNAL NONINVERTING RESPONSE

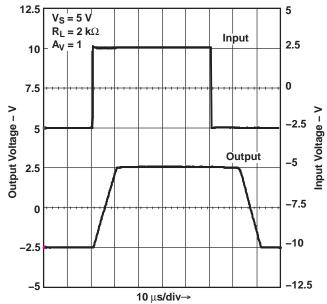
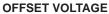
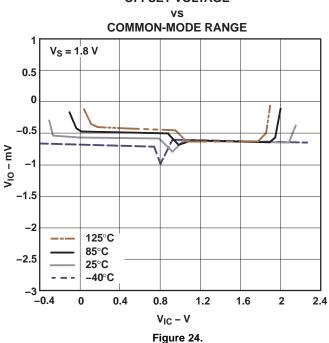


Figure 23.





OFFSET VOLTAGE

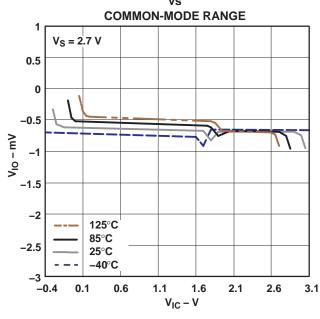
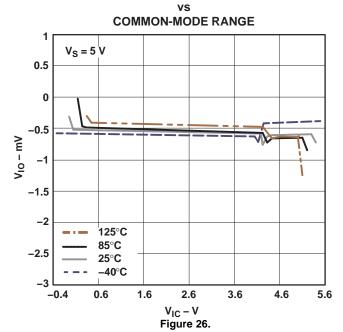


Figure 25.



 $V_{CC+} = 5 \text{ V}$, Single Supply, $T_A = 25^{\circ}\text{C}$ (unless otherwise specified)

OFFSET VOLTAGE







27-Jul-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type		Pins I		Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
LMV931IDBVR	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	(RBBB ~ RBBC ~ RBBI)	
LMV931IDBVRE4	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
LMV931IDBVRG4	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125		
LMV931IDCKR	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125	(RBB ~ RBC ~ RBI)	
LMV931IDCKRE4	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125		
LMV931IDCKRG4	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125		
LMV932ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	MV932I	
LMV932IDE4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDGKR	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125	(RD6 ~ RDB)	
LMV932IDGKRG4	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	MV932I	
LMV932IDRE4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV932IDRG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LMV934ID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LMV934I	
LMV934IDE4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IDG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LMV934I	
LMV934IDRE4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IDRG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	MV934I	
LMV934IPWE4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPWG4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPWR	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	MV934I	
LMV934IPWRE4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
LMV934IPWRG4	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



PACKAGE OPTION ADDENDUM

27-Jul-2013

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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