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Product Brief

TC358766 Display Bridge for DisplayPort™ Connectivity

Highlights

- Display bridge for connectivity of DisplayPort™ panels to the Application Processors with a Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) or Display Pixel Interface (DPI).
- Solutions based on the latest versions of the industry standard MIPI DSI 1.01 to ensure high speed data rates of up to 1 Gbps per lane and MIPI DPI 2.0 to ensure speed of 154 MHz.
- Display port transmitter features VESA DisplayPort 1.1a standard that supports 1.62 or 2.7 Gbps per lane; and configurable to single or dual lane per Main Link.
- Supports high-resolution DisplayPort panels up to WUXGA 1920 x 1200 at refresh rates of 60 fps.
- Applicable to products such as tablets, eBooks, netbooks and laptops.

Description

The Toshiba TC358766 display bridge is optimized for handheld devices using a Host Processor with Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) or Display Pixel Interface (DPI) connectivity. The TC358766 functions as a protocol bridge enabling the video stream from the Host Processor DSI link or DPI link to drive a single or two independent DisplayPort panel(s). The TC358766 has a DSI receiver that can be configured to support up to four DSI lanes with data rates up to 1 Gbps per lane, for maximum total bandwidth of 4 Gbps. It also has a DPI receiver that can be configured to support 16, 18 or 24 bits parallel interfaces and can be operated up to 154 MHz parallel clock. The DisplayPort transmitter can be configured to support a single Main Link with one or 2 lanes or dual Main Links with single lane per link. The data throughput is 1.62 Gbps or 2.7 Gbps per lane of the DisplayPort Main Link.

As the DisplayPort interface uses fewer lines and power consumption is more efficient, availability and usage of high-resolution DisplayPort panels is becoming a feature in handheld applications such as tablets and netbooks. The Toshiba TC358766 display bridge can support displays with resolution up to 1920 x 1200 (WUXGA) at 24 bits per pixel, at refresh rate of 60 frames per second. The TC358766 can support both an embedded DisplayPort panel (eDP) or an external DP panel at one time or simultaneously. The TC358766 bridge supports audio streaming from the Application Processor through the I²S interface. The audio is transmitted through the DisplayPort link if the application requires, i.e. connecting to an external panel.

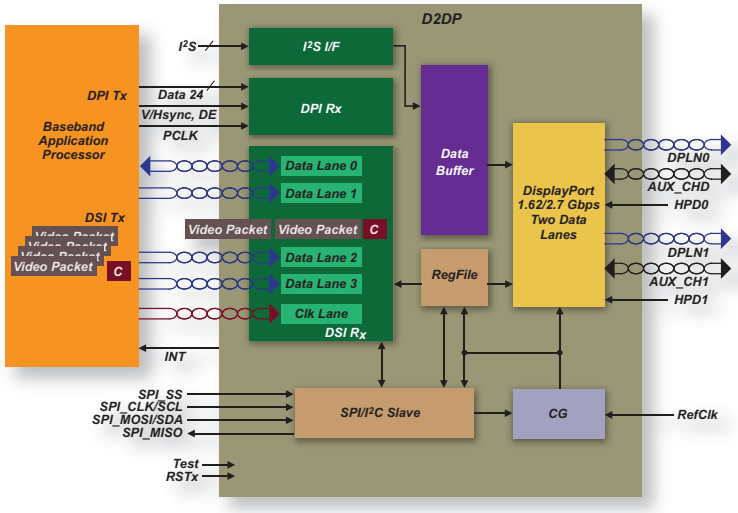
The TC358766 is a 120-pin device, in a small package size of 6 mm x 6 mm, 0.50 mm ball pitch designed for portable products.

Features

DSI Receiver

- MIPI DSI: v1.01 / MIPI D-PHY: v1.0 compliant.
- Up to four (4) data lanes with bi-directional support on Data Lane 0.
- Maximum speed at 1 Gbps/lane.
- Video input data formats:
  - RGB-565, RGB-666 and RGB-888.
  - New DSI V1.02 data type support: 16-bit YCbCr 422
- Interlaced video mode is not supported.

TC358766XBG System Block Diagram



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DPI Receiver

- Maximum speed at 154 MHz.
- Video input data formats: RGB-565, RGB-666 and RGB-888.

I²S Audio Interface

- Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 KHz.
- Supports up to 2 audio channels.
- Optionally inserts IEC60958 status bits and preamble bits per channel.

DisplayPort Interface

- High-speed serial bridge chip using VESA DisplayPort 1.1a standard.
- Supports one dual-lane port for high bandwidth application or two single-lane ports for connection to two DisplayPort panels.
- Supports 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2V
- Support of pre-emphasis levels of 0, 3.5 dB and 6 dB.
- AUX channel supported at 1 Mbps.
- Supports HDCP encryption Version 1.3 Amendment for DisplayPort Revision 1.1.
- SSCG with ~30 KHz modulation to reduce EMI.

I²C Interface

- I²C slave interface for debugging and/or chip register set access.

SPI Interface

- SPI slave interface for chip register set access.
- SPI interface support for up to 30 MHz operation.

Clock Source

- DisplayPort clock source can be derived from an external clock input or from the DSI clock. Acceptable clock values from external source or DSI clock derivatives are 13, 26, 19.2 or 38.4 MHz.

Power Supply Inputs

- Core and MIPI D-PHY: 1.2V
- Digital I/O: 1.8V
- DisplayPort PHY and PLL: 1.8V and 1.2V

Package

- TC358766XBG: 120-pin, 6.0 x 6.0 mm², 0.5 mm ball pitch, 1.0 mm height

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