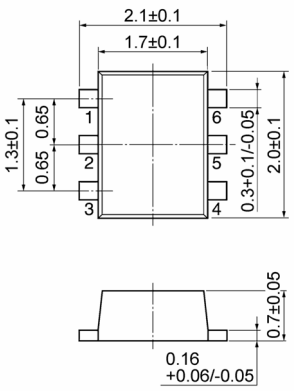
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6K32TU

○ Relay drive, DC-DC converter application

Unit: mm

- 4-V drive
- Low ON-resistance: $R_{DS(ON)}$ = 440mΩ (max) (@V_{GS} = 4 V)
  $R_{DS(ON)}$ = 300mΩ (max) (@V_{GS} = 10 V)



1,2,5,6 : Drain
3 : Gate
4 : Source

UF6	
JEDEC	―
JEITA	―
TOSHIBA	2-2T1D

Weight: 7.0 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	2	A
	Pulse	I_{DP}	6	
Power dissipation		P_D (Note 1)	500	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

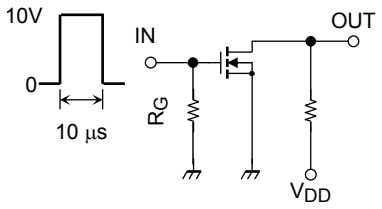
Note 1: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16V, V_{DS} = 0V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10mA, V_{GS} = 0V	60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10V, I_D = 1mA	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4V, I_D = 1A	—	0.33	0.44	Ω
			V_{GS} = 10V, I_D = 1A	—	0.23	0.30	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10V, I_D = 1A	1.0	2.0	—	S
Input capacitance		C_{iss}	V_{DS} = 10V, V_{GS} = 0V f = 1MHz	—	140	—	pF
Reverse transfer capacitance		C_{rss}		—	20	—	
Output capacitance		C_{oss}		—	65	—	
Switching time	Rise time	t_r	V_{DD} ≈ 30 V, I_D = 1 A V_{GS} = 0 to 10 V, R_G = 50 Ω	—	140	—	ns
	Turn-on time	t_{on}		—	210	—	
	Fall time	t_f		—	470	—	
	Turn-off time	t_{off}		—	1600	—	
Total gate charge		Q_g	V_{DD} ≈ 48V, V_{GS} = 10V I_D = 2A	—	5.0	—	nC
Gate−source charge		Q_{gs}		—	3.6	—	
Gate−drain charge		Q_{gd}		—	1.4	—	
Drain-source forward voltage		V_{DSF}	I_D = -2A, V_{GS} = 0V	—	—	−1.5	V

Switching Time Test Circuit

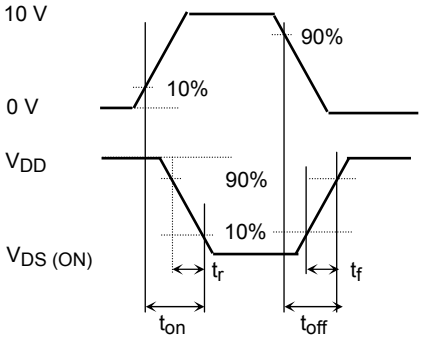
(a) Test Circuit



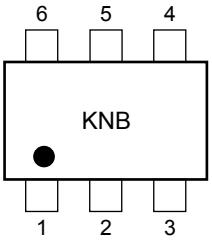
V_{DD} ≈ 30 V
R_G = 50 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b)) V_{IN}

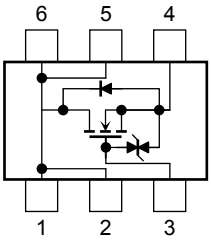
(c) V_{OUT}



Marking



Equivalent Circuit (Top View)



Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = 1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.

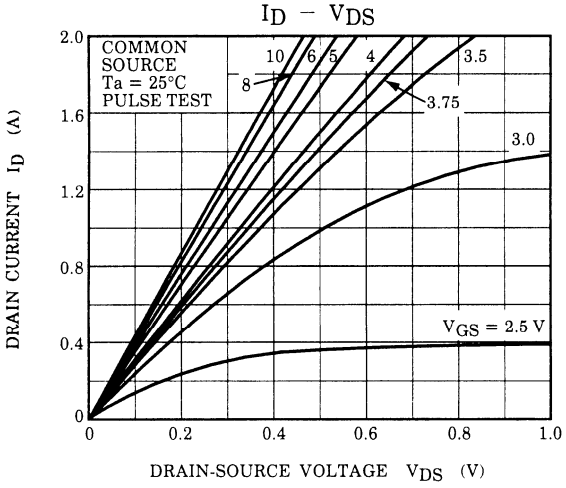
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)
Take this into consideration when using the device.

Handling Precaution

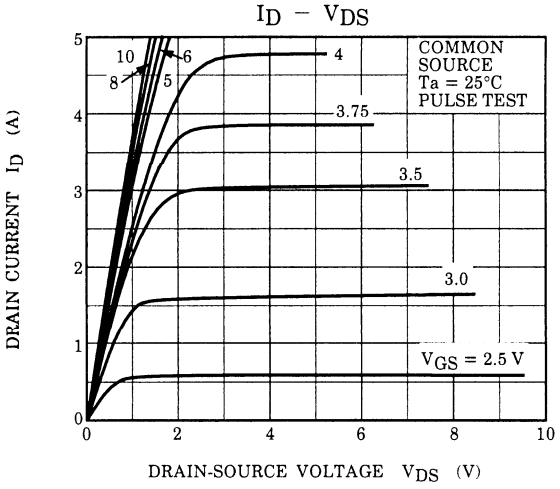
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th\ (ch\text{-}a)}$ and Power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

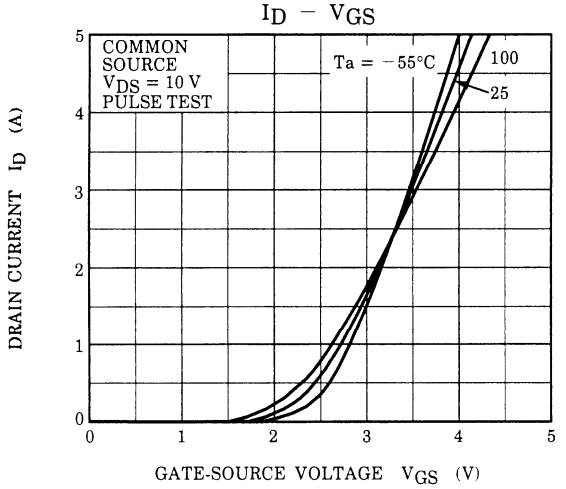
$I_D - V_{DS}$



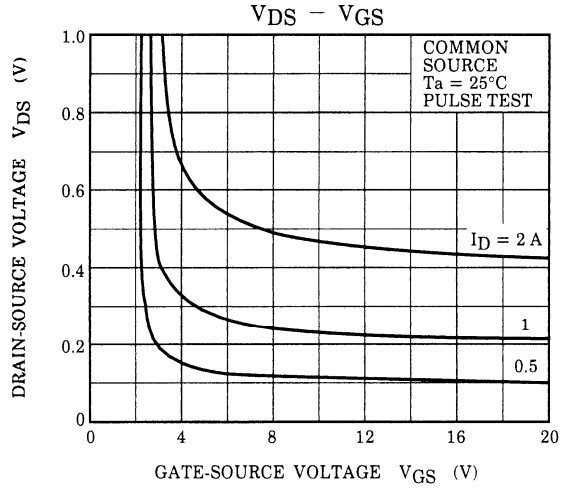
$I_D - V_{DS}$



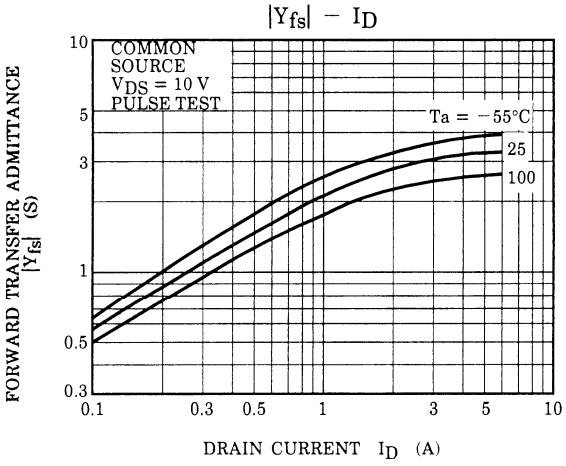
$I_D - V_{GS}$



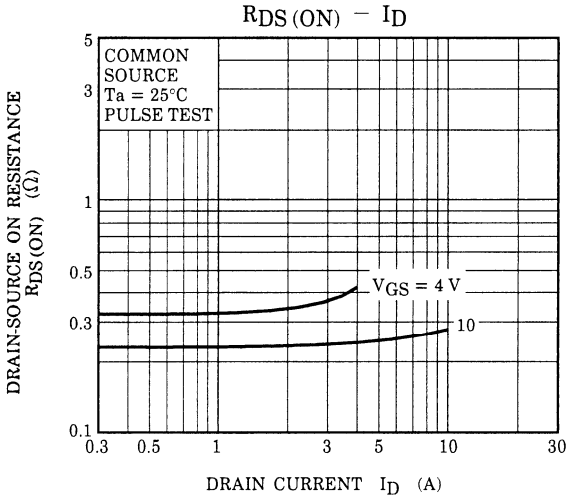
$V_{DS} - V_{GS}$



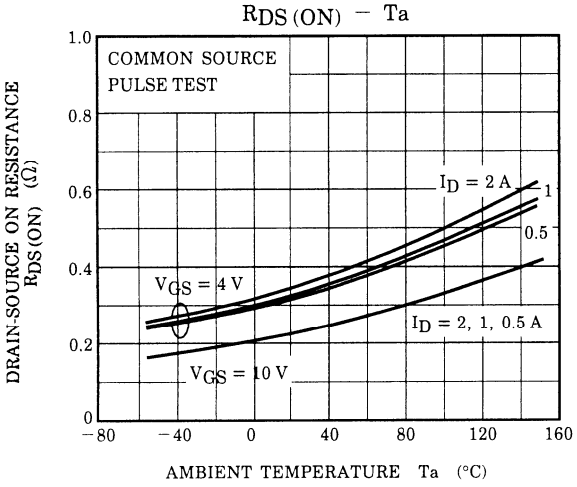
$|Y_{fs}| - I_D$



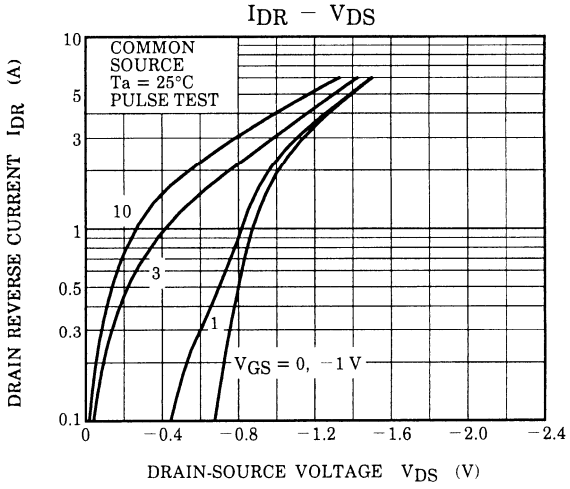
$R_{DS\,(ON)} - I_D$



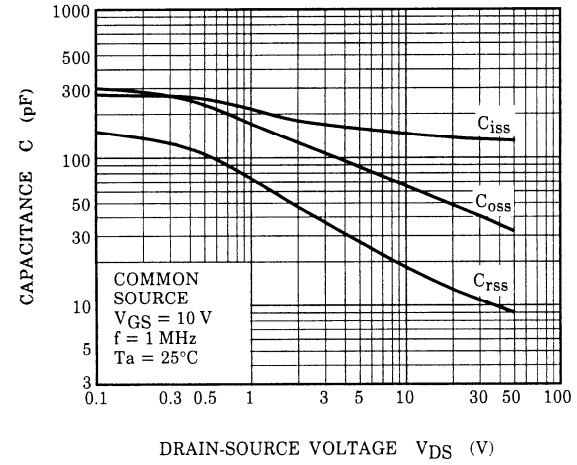
$R_{DS\,(ON)}$ – Ta



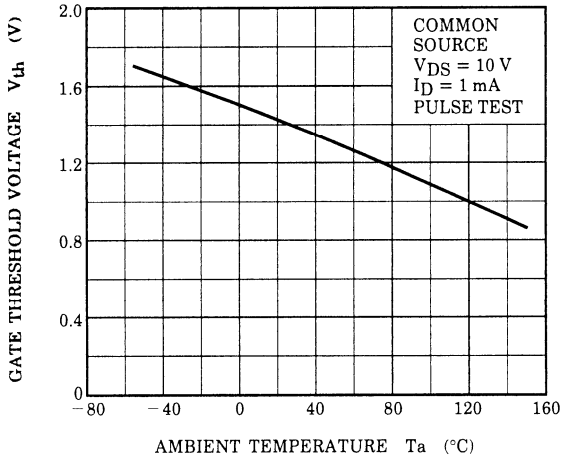
I_{DR} – V_{DS}



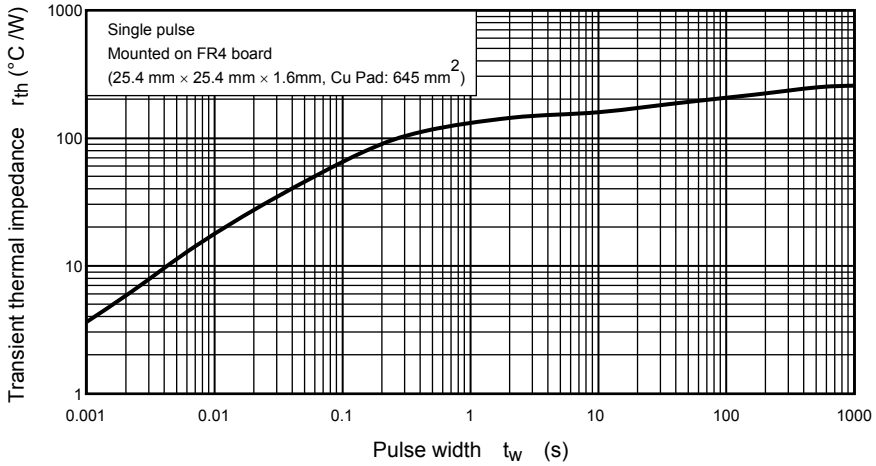
CAPACITANCE – V_{DS}



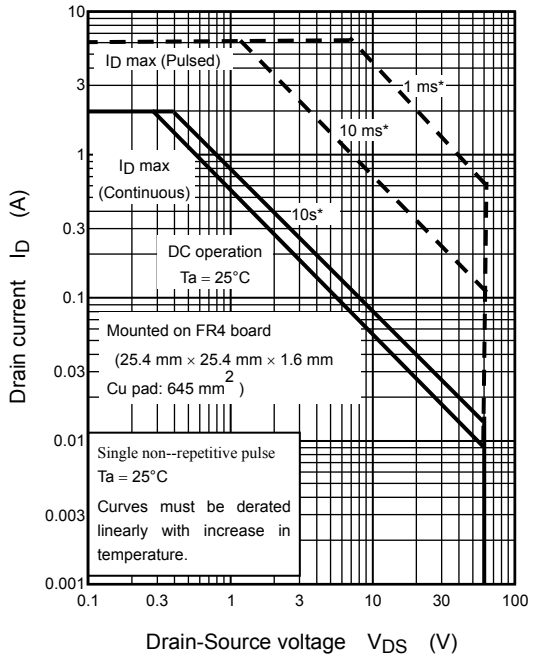
V_{th} – Ta



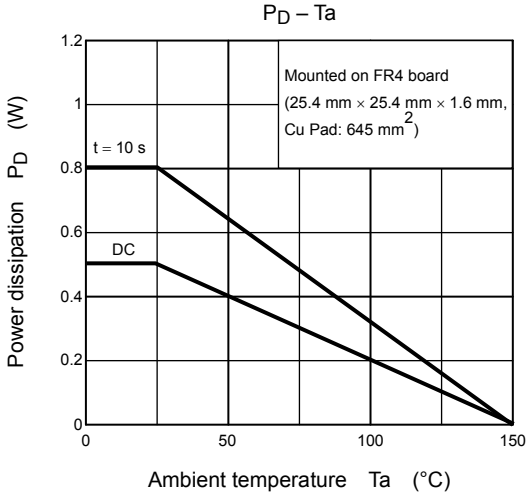
$r_{th} - t_w$



Safe operating area



P_D – Ta



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