

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7WB66CFK, TC7WB67CFK

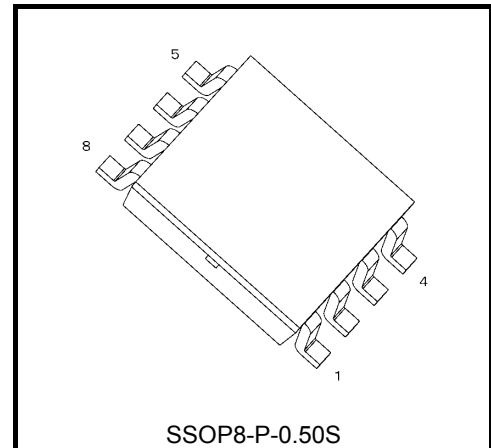
## Low Capacitance Dual Bus Switch (analog)

The TC7WB66C and TC7WB67C are low ON-resistance / low Capacitance high-speed CMOS 2-bit bus switches. These bus switches allow connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

The TC7WB66C requires the output enable (OE) input to be set low to place the output into the high impedance state, whereas the TC7WB67C requires the output enable ( $\overline{\text{OE}}$ ) input to be set high to place the output into the high impedance.

These Bus switches consist of P-MOS and N-MOS structure, meaning these devices are suitable for analog signal transmission.

All inputs are equipped with protector circuits to protect the device from static discharge.

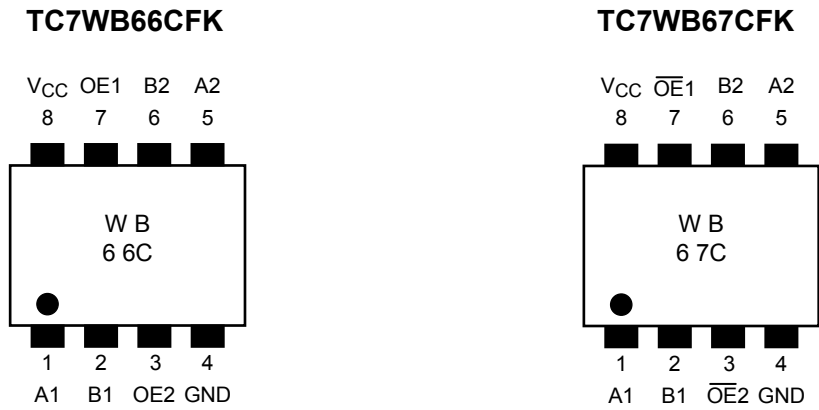


Weight : 0.01 g (typ.)

## Features

- Operating voltage :  $V_{CC} = 1.65$  to  $5.5$  V
- On capacitance :  $C_{I/O} = 10$  pF Switch On (typ.) @  $V_{CC} = 5.0$  V
- On resistance :  $R_{ON} = 4$   $\Omega$  (typ.) @  $V_{CC} = 4.5$  V,  $V_{IS} = 0$  V
- ESD performance : Machine model  $\geq \pm 200$  V  
Human body model  $\geq \pm 2000$  V
- Package: US8

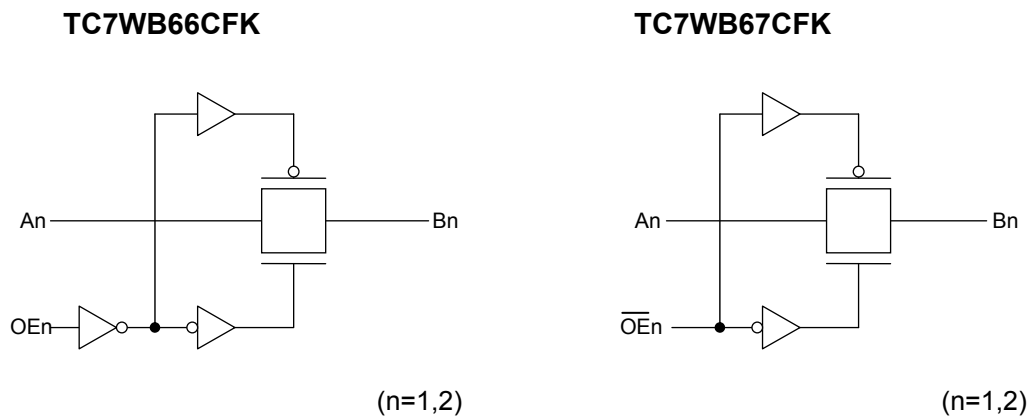
## Pin Assignment (top view)



## Truth Table

Inputs (66C)	Inputs (67C)	Function
OE	$\overline{OE}$	
H	L	A port = B port
L	H	Disconnect

## System Diagram



## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	-0.5 to 7.0	V
Control pin input voltage	$V_{IN}$	-0.5 to 7.0	V
Switch terminal I/O voltage	$V_S$	-0.5 to $V_{CC}+0.5$	V
Clump diode current	$I_{IK}$	-50	mA
Switch I/O current	$I_S$	50	mA
Power dissipation	$P_D$	200	mW
DC $V_{CC}/GND$ current	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	1.65 to 5.5	V
Control pin input voltage	$V_{IN}$	0 to 5.5	V
Switch I/O voltage	$V_S$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Control pin input rise/fall time	dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Typ.	Max	Unit
High-level input Voltage (OE, $\overline{\text{OE}}$ )	V <sub>IH</sub>	—	1.65~1.95	0.8 × V <sub>CC</sub>	—	—	V
			2.3~5.5	0.7 × V <sub>CC</sub>	—	—	
Low-level input Voltage (OE, $\overline{\text{OE}}$ )	V <sub>IL</sub>	—	1.65~1.95	—	—	0.2 × V <sub>CC</sub>	V
			2.3~5.5	—	—	0.3 × V <sub>CC</sub>	
Input leakage current (OE, $\overline{\text{OE}}$ )	I <sub>IN</sub>	V <sub>IN</sub> = 0~5.5V	1.65~5.5	—	—	±1.0	μA
Switch terminal Off-state leakage current	I <sub>SZ</sub>	A, B = 0 to V <sub>CC</sub> , OE = GND (66C), $\overline{\text{OE}}$ = V <sub>CC</sub> (67C)	1.65~5.5	—	—	±10	μA
ON resistance (Note 2)	R <sub>ON</sub>	V <sub>IS</sub> = 0 V, I <sub>IS</sub> = 30 mA (Note 1)	4.5	—	4	7	Ω
		V <sub>IS</sub> = 2.4 V, I <sub>IS</sub> = 30 mA (Note 1)	4.5	—	5	12	
		V <sub>IS</sub> = 4.5 V, I <sub>IS</sub> = 15 mA (Note 1)	4.5	—	6	10	
		V <sub>IS</sub> = 0 V, I <sub>IS</sub> = 24 mA (Note 1)	3.0	—	5	9	
		V <sub>IS</sub> = 3.0 V, I <sub>IS</sub> = 24 mA (Note 1)	3.0	—	7	14	
		V <sub>IS</sub> = 0 V, I <sub>IS</sub> = 8 mA (Note 1)	2.3	—	6	12	
		V <sub>IS</sub> = 2.3 V, I <sub>IS</sub> = 8 mA (Note 1)	2.3	—	9	18	
		V <sub>IS</sub> = 0 V, I <sub>IS</sub> = 4 mA (Note 1)	1.65	—	8	20	
		V <sub>IS</sub> = 1.65 V, I <sub>IS</sub> = 4 mA (Note 1)	1.65	—	15	30	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0A	5.5	—	—	10	μA
	ΔI <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> -0.6 V	5.5	—	—	50	μA

Note 1: All typical values are at Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch.  
ON resistance is determined by the lower of the voltages on the two (A or B) pins.

**AC Characteristics (Ta = -40 to 85°C)**

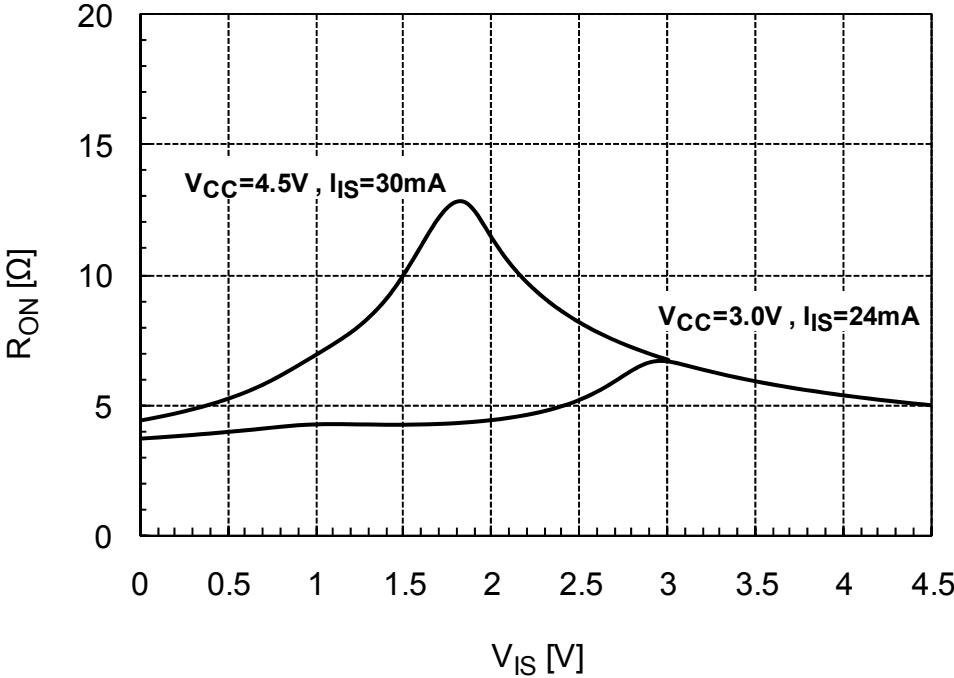
Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Output enable time	t <sub>pZL</sub> t <sub>pZH</sub>	Figure 1, Figure 2	5.0 ± 0.5	—	4	ns
			3.3 ± 0.3	—	6	
			2.5 ± 0.2	—	9	
			1.8 ± 0.15	—	18	
Output disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	Figure 1, Figure 2	5.0 ± 0.5	—	4.5	ns
			3.3 ± 0.3	—	7	
			2.5 ± 0.2	—	9	
			1.8 ± 0.15	—	18	

**Capacitive Characteristics (Ta = 25°C)**

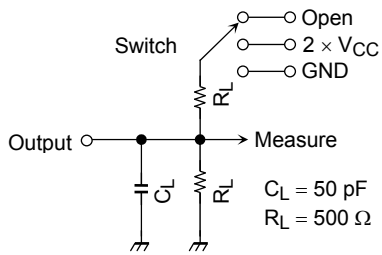
Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Control pin input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V (Note)	5.0	4	pF
Switch terminal OFF capacitance	C <sub>I/O</sub>	OE = GND (66C), $\overline{OE}$ = V <sub>CC</sub> (67C), V <sub>IS</sub> = 0 V (Note)	5.0	5	pF
Switch terminal ON capacitance	C <sub>I/O</sub>	OE = V <sub>CC</sub> (66C), $\overline{OE}$ = GND (67C), V <sub>IS</sub> = 0 V (Note)	5.0	10	pF

Note: Parameter guaranteed by design.

**R<sub>ON</sub> - V<sub>IS</sub> Characteristic (Typ.) Ta = 25°C**



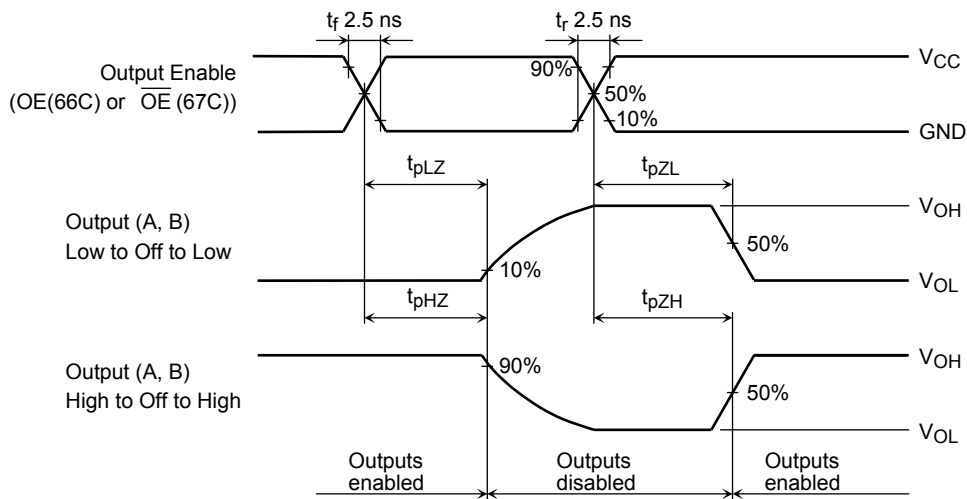
**AC Test Circuit**



Parameter	Switch
$t_{pLZ}, t_{pZL}$	$2 \times V_{CC}$
$t_{pHZ}, t_{pZH}$	GND

**Figure 1**

**AC Waveform**



**Figure 2  $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$**

**Rise and Fall Time (tr / tf) of the TC7WB66C, 67C I/O Signals**

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance (C<sub>I/O</sub>) and the on-resistance (R<sub>ON</sub>) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7WB66C, 67C.

The tr / tf(out) values can be approximated as follows. (Figure 3 shows the test circuit.)

$$tr / tf(out) \text{ (approx)} = -(C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln \left( \frac{(V_{OH} - V_{OL}) - V_M}{(V_{OH} - V_{OL})} \right)$$

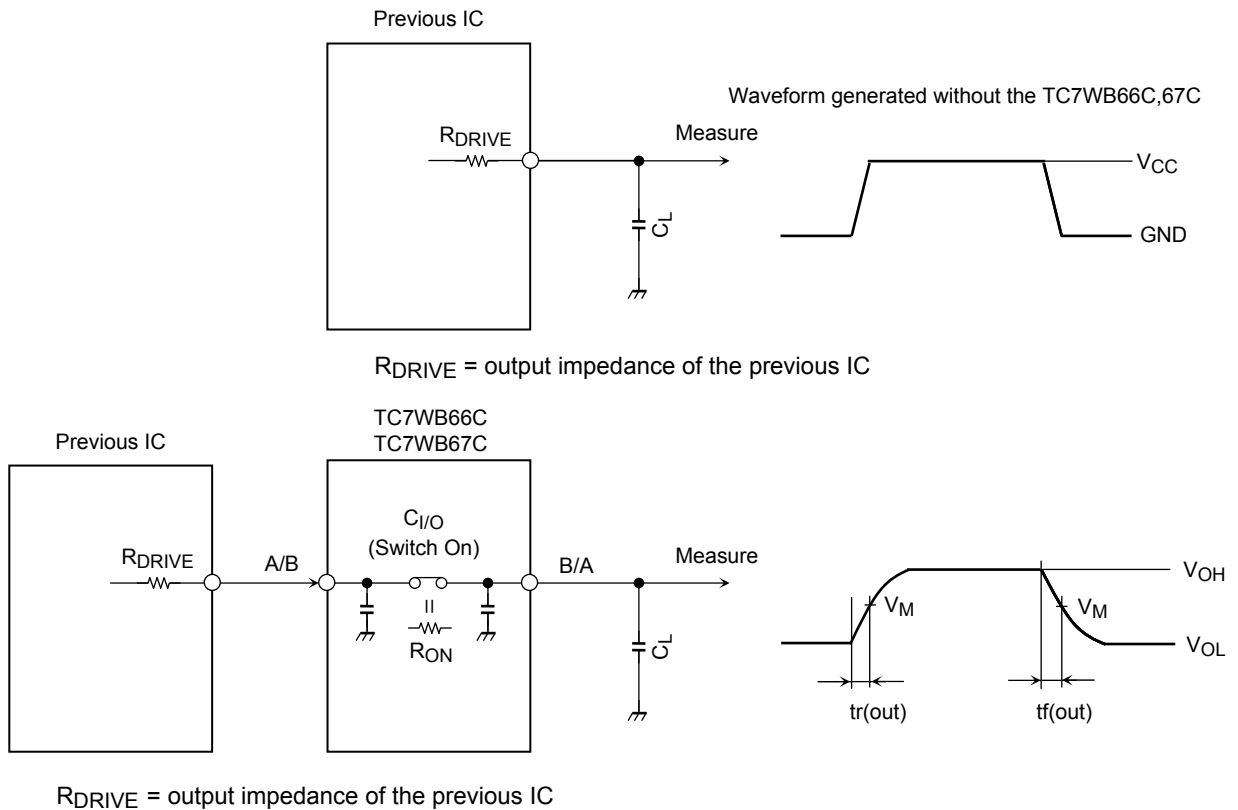
where, R<sub>DRIVE</sub> is the output impedance of the previous-stage circuit.

Calculation example:

$$tr / tf(out) \text{ (approx)} = -(10 + 15) \times 10^{-12} \cdot (120 + 4) \cdot \ln \left( \frac{(4.5 - 0) - 2.25}{(4.5 - 0)} \right) \approx 2.1 \text{ ns}$$

Calculation conditions:

V<sub>CC</sub> = 4.5 V, C<sub>L</sub> = 15 pF, R<sub>DRIVE</sub> = 120 Ω (output impedance of the previous IC), V<sub>M</sub> = 2.25 V (V<sub>CC</sub> / 2)  
 Output voltage of the previous IC = digital (i.e., high-level voltage = V<sub>CC</sub>; low-level voltage = GND)



Parameter	V <sub>CC</sub>			
	5.0 ± 0.5 V	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 ± 0.15 V
V <sub>M</sub>	V <sub>CC</sub> / 2	V <sub>CC</sub> / 2	V <sub>CC</sub> / 2	V <sub>CC</sub> / 2

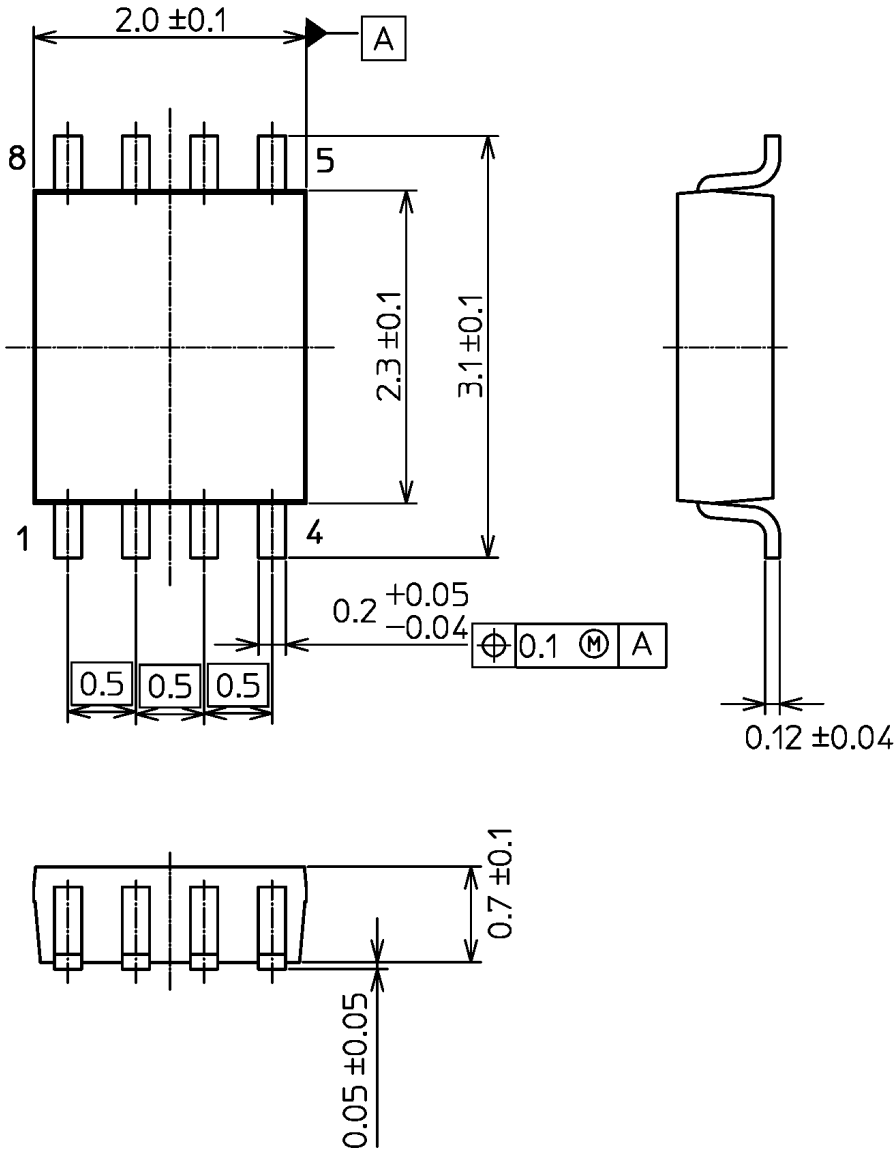
**Figure 3 Test Circuit**



Package Dimensions

SSOP8-P-0.50S

Unit: mm



Weight: 0.01 g (typ.)

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