

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74HC221AP, TC74HC221AF

### Dual Monostable Multivibrator

The TC74HC221A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs,  $\overline{A}$  input (negative edge), and B input (positive edge). These inputs are valid for a slow rise/fall time signal ( $t_r = t_f = 1$  s) as they are schmitt trigger inputs. This device may also be triggered by using  $\overline{CLR}$  input (positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor ( $R_x, C_x$ ). A low level at the  $\overline{CLR}$  input breaks this state.

Limits for  $C_x$  and  $R_x$  are:

External capacitor,  $C_x$ : No limit

External resistor,  $R_x$ :  $V_{CC} = 2.0$  V more than 5 k $\Omega$

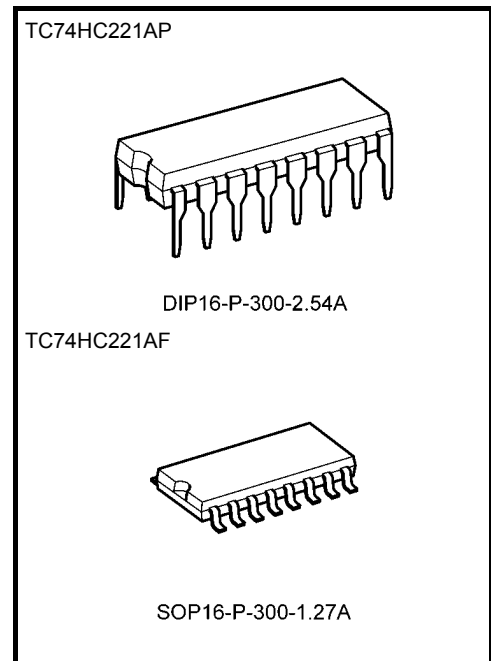
$V_{CC} \geq 3.0$  V more than 1 k $\Omega$

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features (Note)

- High speed:  $t_{pd} = 25$  ns (typ.) at  $V_{CC} = 5$  V
- Low power dissipation
  - Standby by State:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ$ C
  - Active State:  $I_{CC} = 700$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4$  mA (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} (opr) = 2$  to 6 V
- Pin and function compatible with 74LS221

Note: In the case of using only one circuit,  $\overline{CLR}$  should be tied to GND,  $R_x/C_x \cdot C_x \cdot Q \cdot \overline{Q}$  should be tied to OPEN, the other inputs should be tied to  $V_{CC}$  or GND.

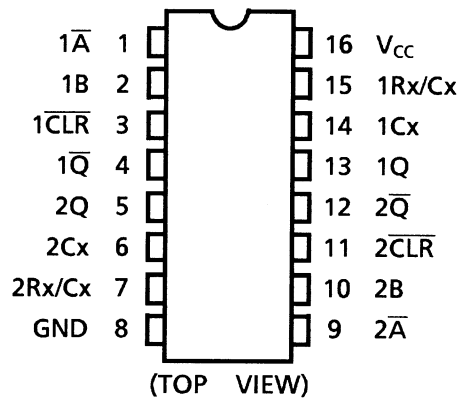


Weight

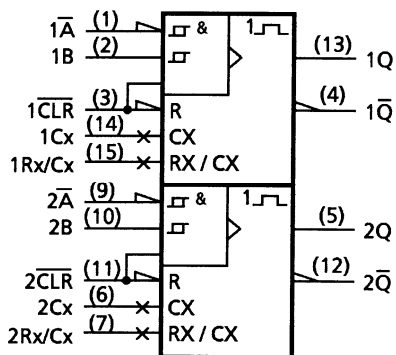
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

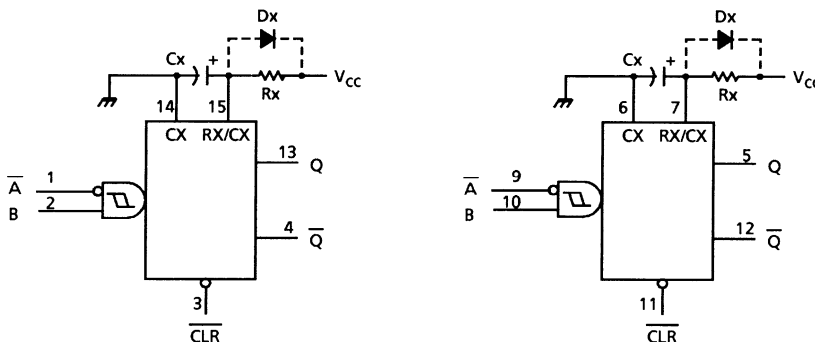
## Pin Assignment



## IEC Logic Symbol



## Block Diagram (Note 1)(Note 2)



Note 1: Cx, Rx, Dx are external capacitor, resistor, and diode, respectively.

Note 2: External clamping diode, Dx;

The external capacitor is charged to  $V_{CC}$  level in the wait state, i.e. when no trigger is applied.

If the supply voltage is turned off, Cx is discharged mainly through the internal (parasitic) diode. If Cx is sufficiently large and  $V_{CC}$  drops rapidly, there will be some possibility of damaging the IC through inrush current or latch-up. If the capacitance of the supply voltage filter is large enough and  $V_{CC}$  drops slowly, the inrush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is  $\pm 20$  mA.

In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (V_{CC} - 0.7) Cx / 20 \text{ mA}$$

( $t_f$  is the time between the supply voltage turn off and the supply voltage reaching  $0.4 V_{CC}$ .)

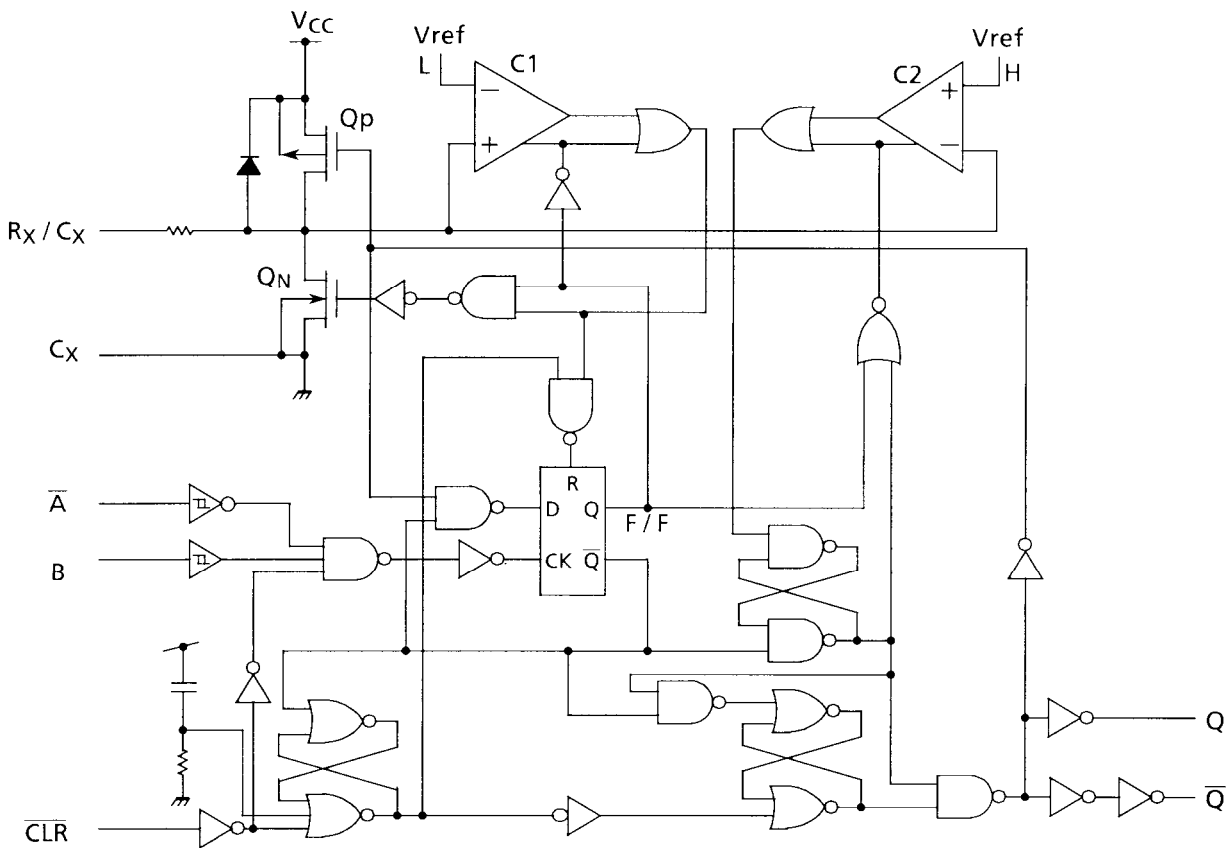
In the even a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from inrush current.

**Truth Table**

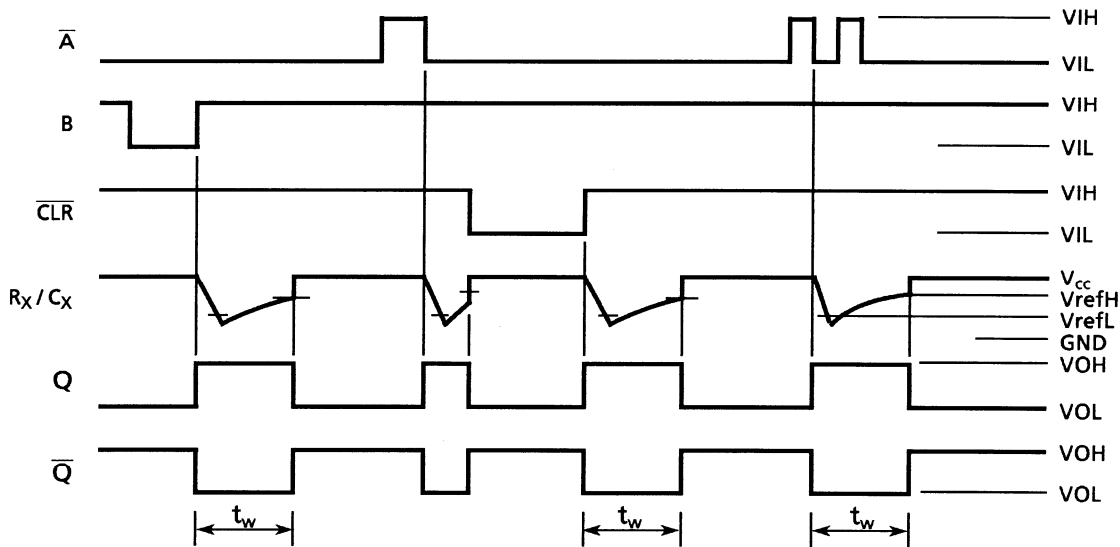
Inputs			Outputs		Function
$\bar{A}$	B	$\bar{CLR}$	Q	$\bar{Q}$	
	H	H			Output Enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L		H			Output Enable
L	H				Output Enable
X	X	L	L	H	Inhibit

X: Don't care

**System Diagram**



**Timing Chart**



**Functional Description**

(1) Stand-by state

The external capacitor ( $C_x$ ) is fully charged to  $V_{CC}$  in the stand-by state. That means, before triggering, the  $Q_P$  and  $Q_N$  transistors which are connected to the  $R_x/C_x$  node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First the condition where the  $\overline{A}$  input is low, and the B input has a rising signal; second, where the B input is high, and the  $\overline{A}$  input has a falling signal; and third, where the  $\overline{A}$  input is low and the B input is high, and the  $\overline{CLR}$  input has a rising signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and  $Q_N$  is turned on. The external capacitor discharges through  $Q_N$ . The voltage level at the  $R_x/C_x$  node drops. If the  $R_x/C_x$  voltage level falls to the internal reference voltage  $V_{refL}$ , the output of C1 becomes low. The flip-flop is then reset and  $Q_N$  turns off. At that moment C1 stops but C2 continues operating.

After  $Q_N$  turns off, the voltage at the  $R_x/C_x$  node starts rising at a rate determined by the time constant of external capacitor  $C_x$  and resistor  $R_x$ .

Upon the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of  $R_x/C_x$  changes from falling to rising. When  $R_x/C_x$  reaches the internal reference voltage  $V_{refH}$ , the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the  $R_x/C_x$  node reaches  $V_{refH}$ , the IC returns to its MONOSTABLE state.

With large values of  $C_x$  and  $R_x$ , and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse,  $t_w$  (OUT), is as follows:

$$t_w \text{ (OUT)} = 1.0 C_x R_x$$

(3) Reset operation

In normal operation,  $\overline{CLR}$  input is held high. If  $\overline{CLR}$  is low, a trigger has no effect because the Q output is held low and trigger control F/F is reset. Also,  $Q_P$  turns on and  $C_x$  is charge rapidly to  $V_{CC}$ .

This means if  $\overline{CLR}$  input is set low, the IC goes into a wait state.

## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}\text{C}$ . From  $T_a = 65$  to  $85^{\circ}\text{C}$  a derating factor of  $-10$  mW/ $^{\circ}\text{C}$  shall be applied until 300 mW.

## Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time ( $\overline{\text{CLR}}$ only)	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns
External capacitor	$C_x$	No limitation (Note 2)	F
External resistor	$R_x$	$\geq 5$ k (Note 5) ( $V_{CC} = 2.0$ V) $\geq 1$ k (Note 5) ( $V_{CC} \geq 3.0$ V)	$\Omega$

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Note 2 The maximum allowable values of  $C_x$  and  $R_x$  are a function of leakage of capacitor  $C_x$ , the leakage of TC74HC221A, and leakage due to board layout and surface resistance.

Susceptibility to externally induced noise signals may occur for  $R_x > 1$  M $\Omega$ .

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage (Q, $\bar{Q}$ )	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 $\mu$ A	2.0	1.9	2.0	—	1.9	—	V
			I <sub>OH</sub> = -4 mA	4.5	4.4	4.5	—	4.4	—	
			I <sub>OH</sub> = -5.2 mA	6.0	5.9	6.0	—	5.9	—	
Low-level output voltage (Q, $\bar{Q}$ )	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 $\mu$ A	2.0	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 4 mA	4.5	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 5.2 mA	6.0	—	0.0	0.1	—	0.1	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	$\pm$ 0.1	—	$\pm$ 1.0	$\mu$ A
Rx/Cx terminal off-state current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	$\pm$ 0.1	—	$\pm$ 1.0	$\mu$ A
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	4.0	—	40.0	$\mu$ A
Active-state supply current (Note)	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND Rx/Cx = 0.5 V <sub>CC</sub>		2.0	—	45	200	—	260	$\mu$ A
				4.5	—	400	500	—	650	$\mu$ A
				6.0	—	0.7	1.0	—	1.3	mA

Note: Per circuit

### Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C	Unit
				V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width	t <sub>W</sub> (L) t <sub>W</sub> (H)	—		2.0	—	75	95	ns
				4.5	—	15	19	
				6.0	—	13	16	
Minimum clear width	t <sub>W</sub> (L)	—		2.0	—	75	95	ns
				4.5	—	15	19	
				6.0	—	13	16	

### AC Characteristics ( $C_L = 15 \text{ pF}$ , $V_{CC} = 5 \text{ V}$ , $T_a = 25^\circ\text{C}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$ $t_{THL}$	—	—	4	8	ns
Propagation delay time ( $\bar{A}$ , B-Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	—	25	36	ns
Propagation delay time ( $\overline{\text{CLR}}$ TRIGGER-Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	—	25	41	ns
Propagation delay time ( $\overline{\text{CLR}}$ -Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	—	16	27	ns

## AC Characteristics ( $C_L = 50 \text{ pF}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	$t_{TLH}$ $t_{THL}$	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time ( $\overline{A}$ , B-Q, $\overline{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	2.0	—	102	210	—	265	ns
			4.5	—	30	42	—	53	
			6.0	—	24	36	—	45	
Propagation delay time ( $\overline{CLR}$ TRIGGER-Q, Q)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	102	235	—	295	ns
			4.5	—	30	47	—	59	
			6.0	—	24	40	—	50	
Propagation delay time ( $\overline{CLR}$ -Q, $\overline{Q}$ )	$t_{pLH}$ $t_{pHL}$	—	2.0	—	67	160	—	200	ns
			4.5	—	20	32	—	40	
			6.0	—	16	27	—	34	
Output pulse width	$t_{wOUT}$	$C_x = 28 \text{ pF}$ $R_x = 6 \text{ k}\Omega$ ( $V_{CC} = 2 \text{ V}$ ) $R_x = 2 \text{ k}\Omega$ ( $V_{CC} = 4.5 \text{ V}, 6 \text{ V}$ )	2.0	—	700	2000	—	2500	ns
			4.5	—	250	400	—	500	
			6.0	—	210	340	—	425	
		$C_x = 0.01 \text{ }\mu\text{F}$ $R_x = 10 \text{ k}\Omega$	2.0	90	110	130	90	130	$\mu\text{s}$
			4.5	95	105	115	95	115	
			6.0	95	105	115	95	115	
		$C_x = 0.1 \text{ }\mu\text{F}$ $R_x = 10 \text{ k}\Omega$	2.0	0.9	1.0	1.2	0.9	1.2	ms
			4.5	0.9	1.0	1.1	0.9	1.1	
			6.0	0.9	1.0	1.1	0.9	1.1	
Output pulse width error between circuits (in same package)	$\Delta t_{wOUT}$	—	—	—	$\pm 1$	—	—	—	%
Input capacitance	$C_{IN}$	—	—	—	5	10	—	10	pF
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	—	174	—	—	—	pF

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot \text{duty}/100 + I_{CC}/2 \text{ (per circuit)}$$

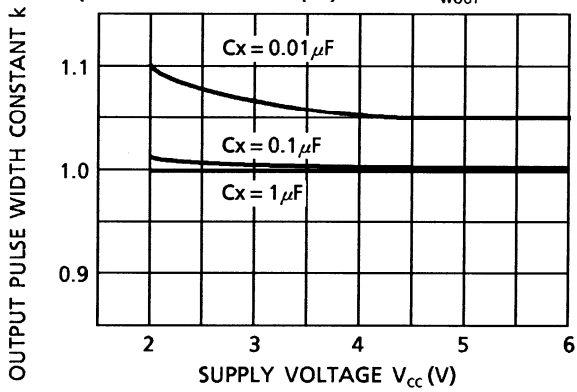
( $I_{CC}'$ : active supply current)

(duty: %)

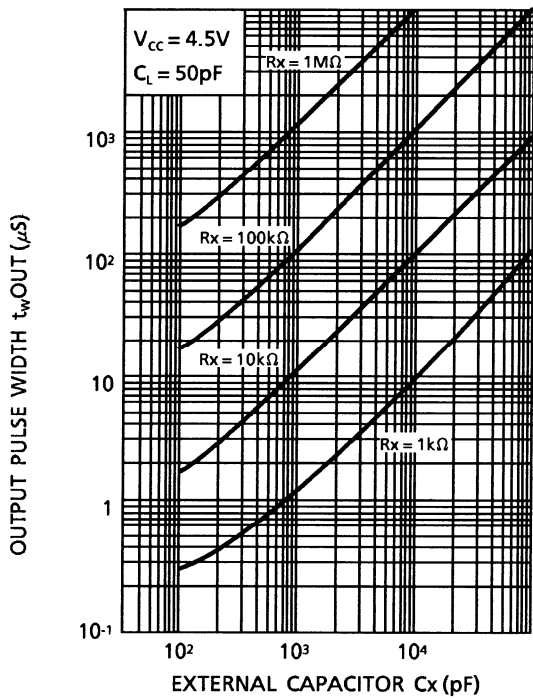


Output Pulse Width Constant K – Supply Voltage (typical)

(EXTERNAL RESISTOR (Rx) = 10kΩ : t<sub>WOUT</sub> = K · Cx · Rx)



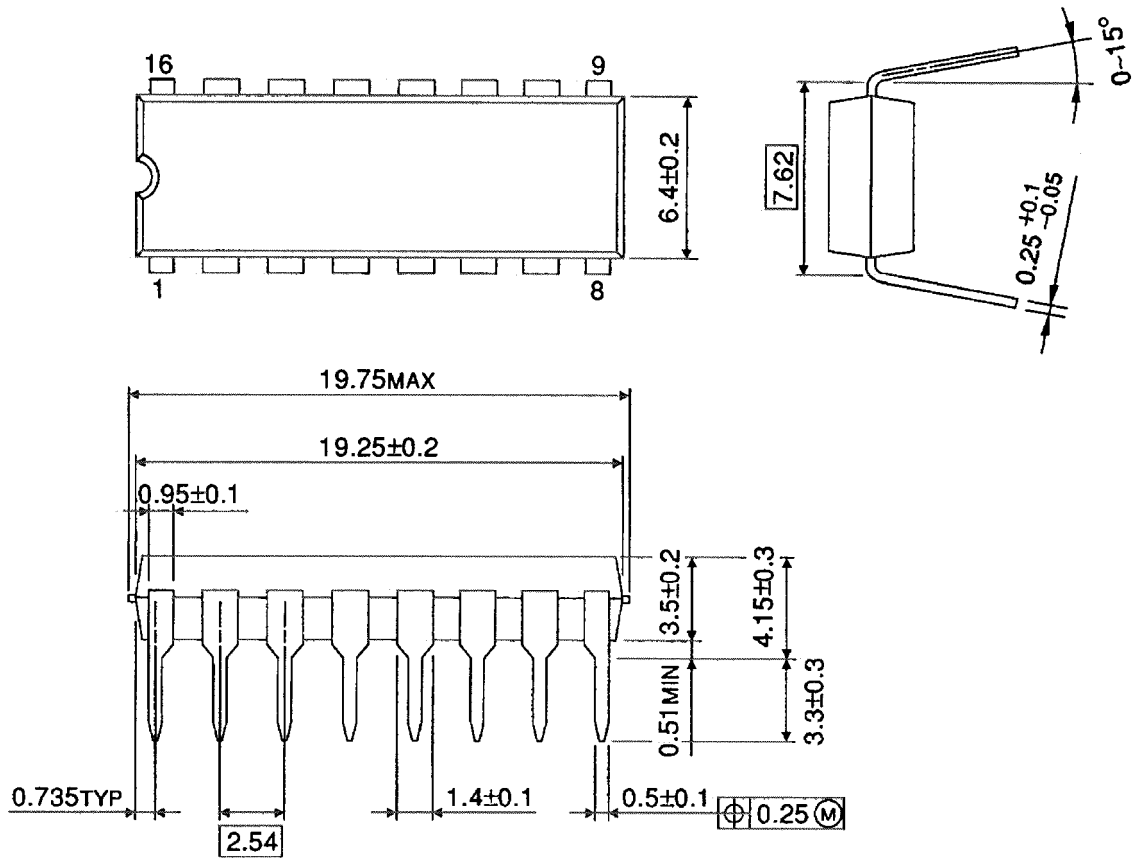
t<sub>WOUT</sub> – C<sub>x</sub> Characteristics (typ.)



## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

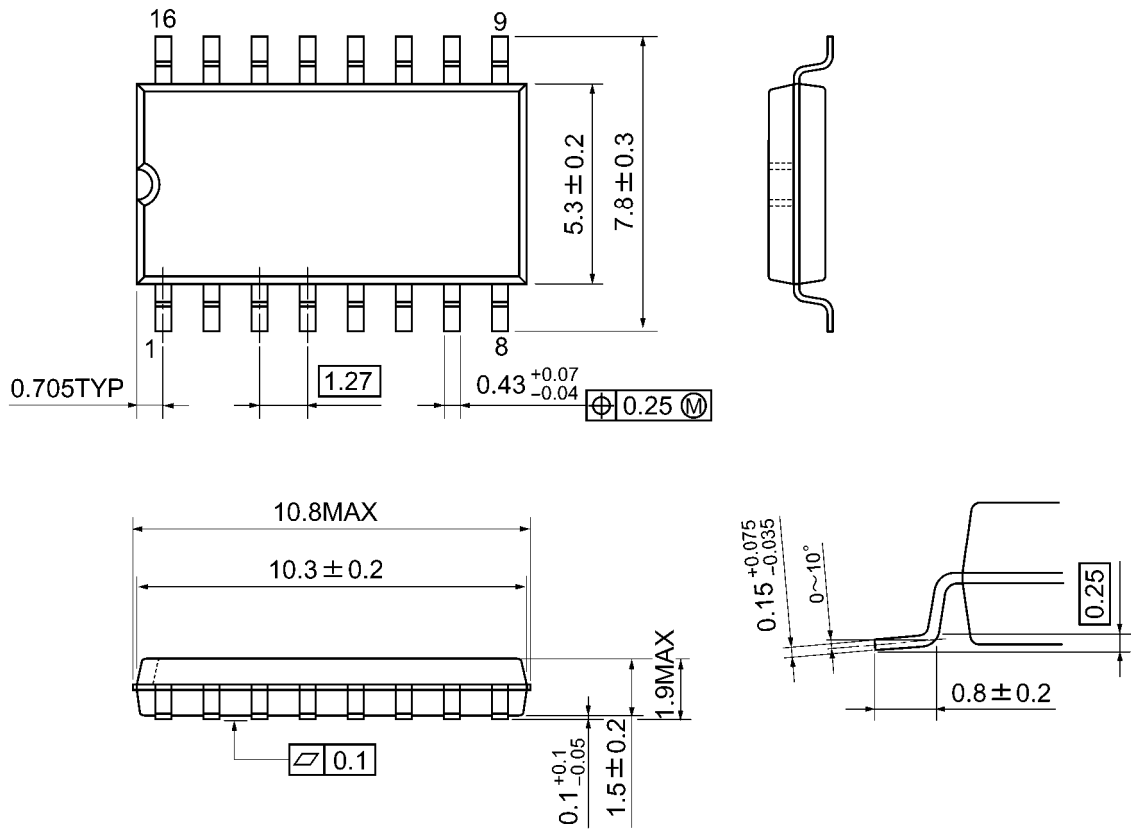


Weight: 1.00 g (typ.)

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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