## intersil

## Radiation Hardened Quad Voltage Comparator

## HS-139RH, HS-139EH

The Radiation Hardened HS-139RH, HS-139EH consists of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground, even when operated from a single supply and the low supply current makes these comparators suitable for low power applications. These types were designed to directly interface with TTL and CMOS.

The HS-139RH, HS-139EH are fabricated on our dielectrically isolated Rad Hard Silicon Gate (RSG) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-139RH, HS-139EH are contained in SMD 5962-98613. A "hot-link" is provided on our homepage with instructions for downloading. www.intersil.com/spacedefense/newsafclasst.asp

## Features

- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
- Latch-up free under any conditions
- Total dose (Max). . . . . . . . . . . . . . . . . . . . . . . $3 \times 10^{5}$ RAD(Si)
- SEU LET threshold . . . . . . . . . . . . . . . . . . . . 20MeV/cm²/mg
- Low dose rate effects immunity
- 100V output voltage withstand capability
- ESD protection to $>3000 \mathrm{~V}$
- Differential input voltage range equal to the supply voltage
- Input offset voltage ( $\mathrm{V}_{10}$ ).

2mV (Max)

- Quiescent supply current . ........................ 2mA (Max)
- Pb-Free (RoHS Compliant)


## Applications

- Pulse generators
- Timing circuitry
- Level shifting
- Analog-to-digital conversion


## Pin Configurations

HS-139RH, HS-139EH
(SBDIP CDIP2-T14)
TOP VIEW


HS-139RH, HS-139EH
(FLATPACK CDFP3-F14) TOP VIEW


## Ordering Information

| ORDERING SMD NUMBER <br> (Note 1) | PART NUMBER (Note 2) | PART MARKING | TEMP. RANGE $\left({ }^{\circ} \mathrm{C}\right)$ | PACKAGE <br> (RoHS Compliant) | PKG. DWG. \# |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5962F9861303VCC | HS1-139EH-Q | Q 5962F98 61303VCC | -55 to +125 | 14 Ld SBDIP | D14.3 |
| 5962F9861301VCC | HS1-139RH-Q | Q 5962F98 61301VCC | -55 to +125 | 14 Ld SBDIP | D14.3 |
| 5962F9861301QCC | HS1-139RH-8 | Q 5962F98 61301QCC | -55 to +125 | 14 Ld SBDIP | D14.3 |
| HS1-139RH/PROTO | HS1-139RH/PROTO | HS1-139RH/PROTO | -55 to +125 | 14 Ld SBDIP | D14.3 |
| 5962F9861301VXC | HS9-139RH-Q | Q 5962F98 61301VXC | -55 to +125 | 14 Ld FLATPACK | K14.A |
| 5962F9861301QXC | HS9-139RH-8 | Q 5962F98 61301QXC | -55 to +125 | 14 Ld FLATPACK | K14.A |
| 5962F9861303VXC | HS9-139EH-Q | Q 5962F98 61303VXC | -55 to +125 | 14 Ld FLATPACK | K14.A |
| HS9-139RH/PROTO | HS9-139RH/PROTO | HS9-139RH / PROTO | -55 to +125 | 14 Ld FLATPACK | K14.A |
| 5962F9861303V9A | HSO-139EH-Q |  | -55 to +125 | Die |  |
| 5962F9861301V9A | HSO-139RH-Q |  | -55 to +125 | Die |  |
| HSO-139RH/SAMPLE | HS0-139RH/SAMPLE |  | -55 to +125 | Die |  |

## NOTES:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table on page 2 must be used when ordering.
2. These Intersil Pb-free Hermetic packaged products employ 100\% Au plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb -free soldering operations.

## Die Characteristics

## DIE DIMENSIONS:

$3750 \mu \mathrm{~m} \times 2820 \mu \mathrm{~m}$ ( 148 mils $\times 111$ mils)
$483 \mu \mathrm{~m} \pm 25.4 \mu \mathrm{~m}$ ( $19 \mathrm{mils} \pm 1 \mathrm{mil}$ )

## INTERFACE MATERIALS:

## Glassivation:

Type: Silox $\left(\mathrm{SiO}_{2}\right)$
Thickness: $8.0 \mathrm{k} \AA \AA \pm 1.0 \mathrm{k} \AA$

## Top Metallization:

Type: AlSiCu
Thickness: $16.0 \mathrm{k} \AA$ 土2k $\AA$

## Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

## Backside Finish:

Silicon

## ASSEMBLY RELATED INFORMATION:

## Substrate Potential:

Unbiased (DI)
ADDITIONAL INFORMATION:
Worst Case Current Density:
$<2.0 \times 10^{5} \mathrm{~A} / \mathrm{cm}^{2}$
Transistor Count:
49

## Metallization Mask Layout



## TABLE 1. HS-139RH, HS-139EH PAD COORDINATES

|  |  | RELATIVE TO PIN 1 |  |
| :---: | :---: | :---: | :---: |
| PIN NUMBER | PAD NAME | $\mathbf{X}$ <br> COORDINATES | $\mathbf{Y}$ <br> COORDINATES |
| 1 | OUT 2 | 0 | 0 |
| 2 | OUT 1 | 0 | -535 |
| 3 | $\mathrm{~V}+$ | 1323 | -688 |
| 4 | $-\operatorname{IN~1}$ | 1862 | -670 |
| 5 | $+\operatorname{IN~1}$ | 2439 | -670 |
| 6 | $-\operatorname{IN} 2$ | 3084 | -299 |
| 7 | $+\operatorname{IN} 2$ | 3084 | 278 |
| 8 | $-\operatorname{IN} 3$ | 3084 | 518 |
| 9 | + IN 3 | 3084 | 1095 |
| 10 | $-\operatorname{IN} 4$ | 2439 | 1466 |
| 11 | +IN 4 | 1862 | 1466 |
| 12 | GND | 1550 | 1503 |
| 13 | OUT 4 | 0 | 1331 |
| 14 | OUT 3 | 0 | 796 |

NOTE: Dimensions in microns

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[^0]Ceramic Dual-In-Line Metal Seal Packages (SBDIP)


NOTES:
3. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
4. The maximum limits of lead dimensions $b$ and $c$ or $M$ shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
6. Corner leads ( $1, \mathrm{~N}, \mathrm{~N} / 2$, and $\mathrm{N} / 2+1$ ) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
7. Dimension $Q$ shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. Measure dimension S 2 from the top of the ceramic body to the nearest metallization or lead.
10. $N$ is the maximum number of terminal positions.
11. Braze fillets shall be concave.
12. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
13. Controlling dimension: $\operatorname{INCH}$.

D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C) 14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

| SYMBOL | INCHES |  | MILLIMETERS |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.785 | - | 19.94 | - |
| E | 0.220 | 0.310 | 5.59 | 7.87 | - |
| e | 0.10 | SC |  | BSC | - |
| eA | 0.30 | SC |  | 3SC | - |
| eA/2 | 0.15 | SC |  | BSC | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 5 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| S2 | 0.005 | - | 0.13 | - | 7 |
| $\alpha$ | $90^{\circ}$ | $105^{\circ}$ | $90^{\circ}$ | $105^{\circ}$ | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 14 |  | 14 |  | 8 |

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## Ceramic Metal Seal Flatpack Packages (Flatpack)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions $b$ and $c$ or $M$ shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. $N$ is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension $Q$ shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension $Q$ minimum shall be reduced by 0.0015 inch $(0.038 \mathrm{~mm})$ maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B) 14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

| SYMBOL | INCHES |  | MILLIMETERS |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |  |  |  |  |  |  |  |
| A | 0.045 | 0.115 | 1.14 | 2.92 | - |  |  |  |  |  |  |  |
| b | 0.015 | 0.022 | 0.38 | 0.56 | - |  |  |  |  |  |  |  |
| b1 | 0.015 | 0.019 | 0.38 | 0.48 | - |  |  |  |  |  |  |  |
| c | 0.004 | 0.009 | 0.10 | 0.23 | - |  |  |  |  |  |  |  |
| c1 | 0.004 | 0.006 | 0.10 | 0.15 | - |  |  |  |  |  |  |  |
| D | - | 0.390 | - | 9.91 | 3 |  |  |  |  |  |  |  |
| E | 0.235 | 0.260 | 5.97 | 6.60 | - |  |  |  |  |  |  |  |
| E1 | - | 0.290 | - | 7.11 | 3 |  |  |  |  |  |  |  |
| E2 | 0.125 | - | 3.18 | - | - |  |  |  |  |  |  |  |
| E3 | 0.030 | - | 0.76 | - | 7 |  |  |  |  |  |  |  |
| e | 0.050 |  | BSC |  | 1.27 |  |  |  |  |  |  |  |
| k BSC | - |  |  |  |  |  |  |  |  |  |  |  |
| L | 0.008 | 0.015 | 0.20 | 0.38 | 2 |  |  |  |  |  |  |  |
| Q | 0.270 | 0.370 | 6.86 | 9.40 | - |  |  |  |  |  |  |  |
| S1 | 0.026 | 0.045 | 0.66 | 1.14 | 8 |  |  |  |  |  |  |  |
| M | - |  |  |  |  |  |  | 0.0015 | - | 0.13 | - | 6 |
| N | 14 |  |  |  |  |  |  |  | - |  |  |  |

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[^0]:    For information regarding Intersil Corporation and its products, see www.intersil.com

