Data Sheet | September 3, 2009 | FN6387.1

Power Line Communication (PLC)

The ISL1571 is a dual operational amplifier designed for PLC line driving in OFDM and SSC based solutions. This device features a high drive capability of 750mA while consuming only 6mA of supply current per amplifier and operating from a single 4.5V to 12V supply. The driver achieves a typical distortion of -80dBc, at 150kHz into a 25Ω load.

The ISL1571 is available in the thermally-enhanced 16 Ld QFN or 10 Ld HMSOP package and is specified for operation over the full -40°C to +85°C temperature range. The ISL1571 has control pins $BIAS_0$ and $BIAS_1$ for controlling the bias and enable/disable of the outputs. These controls allow for lowering the power to fit the performance/power ratio for the application.

The ISL1571 is ideal for line driving applications following the Homeplug 1.0, Homeplug AV and UPA standard based PLC.

Features

- 21dBm output power capability
- Drives up to 750mA from a +12V supply
- $20V_{P-P}$ differential output drive into 21Ω
- Very low noise floor
- -75dBc typical driver output distortion at 4MHz
- -80dBc typical driver output distortion at 10MHz
- -79dBc typical driver output distortion at 17MHz
- Low quiescent current of 6mA per amplifier
- Supply range
  - For ISL1571IUEZ 4.5V to 12V
  - For ISL1571IRZ ±2.25V to ±6V, 4.5V to 12V
- 250MHz bandwidth
- Thermal shutdown
- Pb-free (RoHS compliant)

Applications

- Homeplug 1.0
- Homeplug AV
- UPA digital home standard

Ordering Information

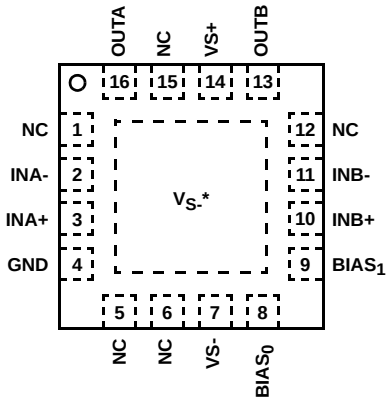
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL1571IRZ	157 1IRZ	-40 to +85	16 Ld QFN	MDP0046
ISL1571IRZ-T7*	157 1IRZ	-40 to +85	16 Ld QFN (Tape and Reel)	MDP0046
ISL1571IUEZ	BBBDA	-40 to +85	10 Ld HMSOP	MDP0050
ISL1571IUEZ-T7*	BBBDA	-40 to +85	10 Ld HMSOP (Tape and Reel)	MDP0050

*Please refer to TB347 for details on reel specifications

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

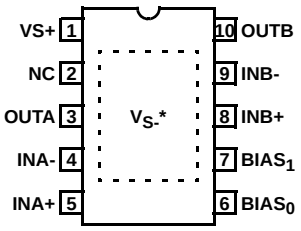
Pinouts

ISL1571
16 LD QFN
TOP VIEW



***THERMAL PAD MUST BE CONNECTED TO NEGATIVE SUPPLY: V_{S-}. QFN PACKAGE CAN BE USED IN SINGLE AND DUAL SUPPLY APPLICATIONS.**

ISL1571
(10 LD HMSOP)
TOP VIEW



***THERMAL PAD MUST BE CONNECTED TO NEGATIVE SUPPLY: V_{S-}. HMSOP PACKAGE CAN BE USED IN SINGLE SUPPLY APPLICATIONS ONLY.**

Pin Descriptions

16 LD QFN	10 LD HMSOP	PIN NAME	FUNCTION
1, 5, 6, 12, 15	2	NC	No Connect
2	4	INA-	Inverting Input of Amplifier A
3	5	INA+	Non-Inverting Input of Amplifier A
4	Thermal Pad	GND	Ground Connect
7	Thermal Pad	VS-	Negative Supply
8	6	$BIAS_0$ (Note 1)	Current Control Bias Pin
9	7	$BIAS_1$ (Note 1)	Current Control Bias Pin
10	8	INB+	Non-Inverting Input of Amplifier B
11	9	INB-	Inverting Input of Amplifier B
13	10	OUTB	Output of Amplifier B
14	1	VS+	Positive Supply
16	3	OUTA	Output of Amplifier A

NOTE:

1. Single DSL port is comprised of amplifiers A and B. $BIAS_0$ and $BIAS_1$ control I_S settings for the DSL port.

Absolute Maximum Ratings (T_A = +25°C)

V_S+ Voltage to Ground . . . . . -0.3V to +13.2V
V_{IN}+ Voltage . . . . . GND to V_S+
Current into any Input 8mA
Continuous Output Current 75mA
$BIAS_0$, $BIAS_1$ to Ground . . . . . +6.6V
ESD Rating
Human Body Model 1kV*
Charge Device Model. 1.5kV

Thermal Information

Ambient Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -60°C to +150°C
Operating Junction Temperature . . . . . +150°C
Power Dissipation . . . . . See Curves
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*Excludes C0 and C1 pins which show less than 1kV of HBM ESD sensitivity.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 12V, R_F = 750Ω, $R_{L\text{-}DIFF}$ = 50Ω, $BIAS_0$ = $BIAS_1$ = 0V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	R_F = 750Ω, A_V = +5		250		MHz
		R_F = 750Ω, A_V = +10		200		MHz
THD	Total Harmonic Distortion, Differential	f = 4MHz, $V_O = 4V_{P\text{-}P\_DIFF}$, $R_{L\text{-}DIFF}$ = 100Ω		-75		dBc
		f = 10MHz, $V_O = 4V_{P\text{-}P\_DIFF}$, $R_{L\text{-}DIFF}$ = 100Ω		-80		dBc
		f = 17MHz, $V_O = 4V_{P\text{-}P\_DIFF}$, $R_{L\text{-}DIFF}$ = 100Ω		-79		dBc
SR	Slew Rate, Single-ended	V_{OUT} from -3V to +3V	750	1200		V/µs
DC PERFORMANCE						
V_{OS_CM}	Offset Voltage Common Mode		-40		+40	mV
V_{OS_DM}	Offset Voltage Differential Mode		-7.5		+7.5	mV
R_{OL}	Differential Transimpedance	$V_{OUT} = 12V_{P\text{-}P}$ differential, unloaded		3.0		MΩ
INPUT CHARACTERISTICS						
I_B+	Non-Inverting Input Bias Current		-7.0		+7.0	µA
$I_{B\text{-}\ DM}$	Inverting Input Bias Current Differential Mode		-75	3	+75	µA
e_N	Input Noise Voltage			6		$nV/\sqrt{Hz}$
i_N	-Input Noise Current			13		$pA/\sqrt{Hz}$
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing (single ended)	V_S = ±6V, $R_{L\ DIFF}$ = 50Ω	±4.8	±5.0		V
		V_S = ±6V, $R_{L\ DIFF}$ = 20Ω	±4.35	±4.7		V
I_{OUT}	Output Current	R_L = 0Ω		1000		mA
SUPPLY						
V_S	Supply Voltage	Single supply	4.5		13.2	V
I_S+ (Full Bias)	Positive Supply Current per Amplifier	All outputs at 0V, $BIAS_0$ = $BIAS_1$ = 0V	12	15	21.5	mA
I_S+ (Medium Bias)	Positive Supply Current per Amplifier	All outputs at 0V, $BIAS_0$ = 5V, $BIAS_1$ = 0V		11		mA
I_S+ (Low Bias)	Positive Supply Current per Amplifier	All outputs at 0V, $BIAS_0$ = 0V, $BIAS_1$ = 5V		6.0		mA
I_S+ (Power-down)	Positive Supply Current per Amplifier	All outputs at 0V, $BIAS_0$ = $BIAS_1$ = 5V		0.6	1.0	mA
I_{INH}, $BIAS_0$ or $BIAS_1$	$BIAS_0$, $BIAS_1$ Input Current, High	$BIAS_0$, $BIAS_1$ = 6V	100	175	250	µA
I_{INL}, $BIAS_0$ or $BIAS_1$	$BIAS_0$, $BIAS_1$ Input Current, Low	$BIAS_0$, $BIAS_1$ = 0V	-5		+5	µA
V_{INH}, $BIAS_0$ or $BIAS_1$	$BIAS_0$, $BIAS_1$ Input Voltage, High		2.0			V
V_{INL}, $BIAS_0$ or $BIAS_1$	$BIAS_0$, $BIAS_1$ Input Voltage, Low				0.8	V

Typical Performance Curves

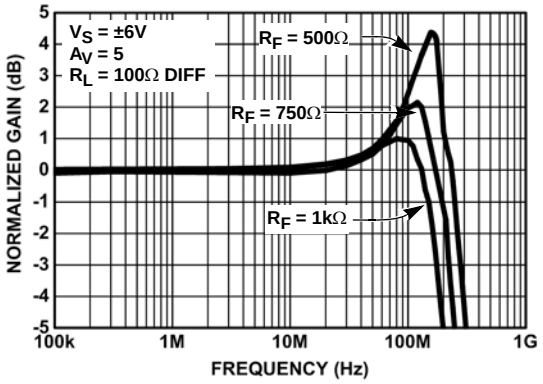


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (FULL BIAS MODE)

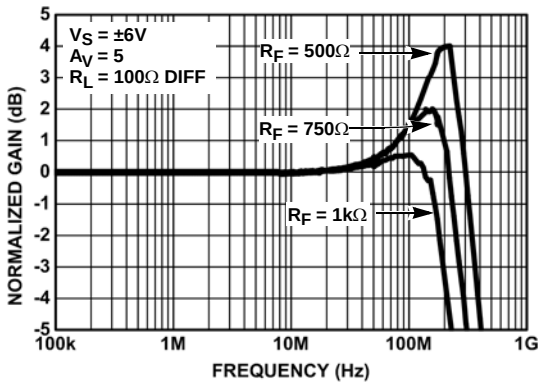


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (MEDIUM BIAS MODE)

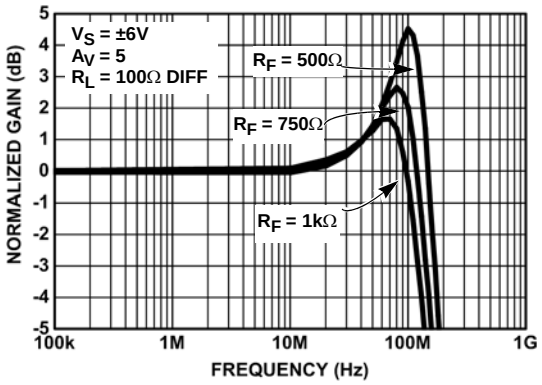


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (LOW BIAS MODE)

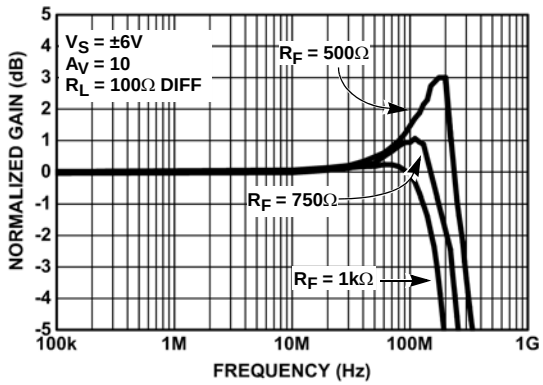


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (FULL BIAS MODE)

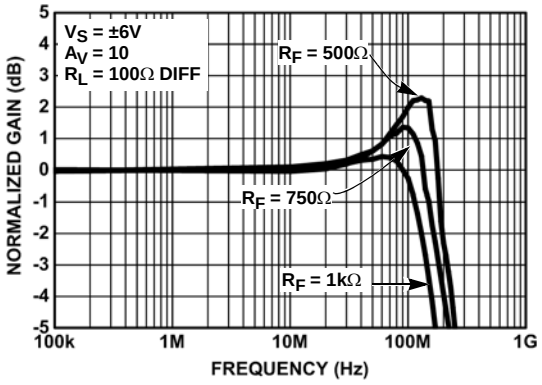


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (MEDIUM BIAS MODE)

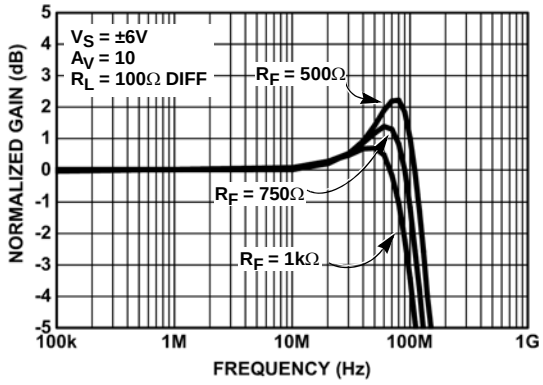


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (LOW BIAS MODE)

Typical Performance Curves (Continued)

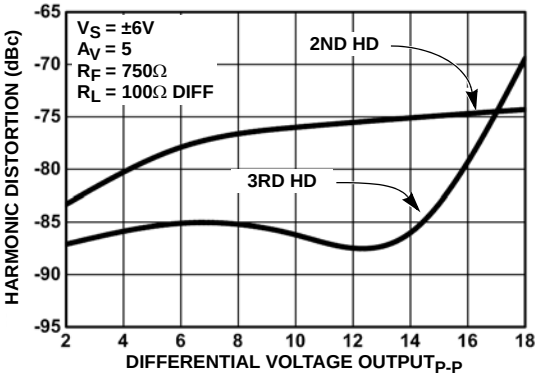


FIGURE 7. HARMONIC DISTORTION @ 2MHz

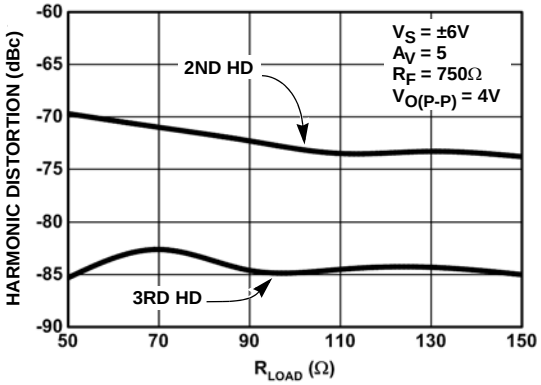


FIGURE 8. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} @ 2MHz

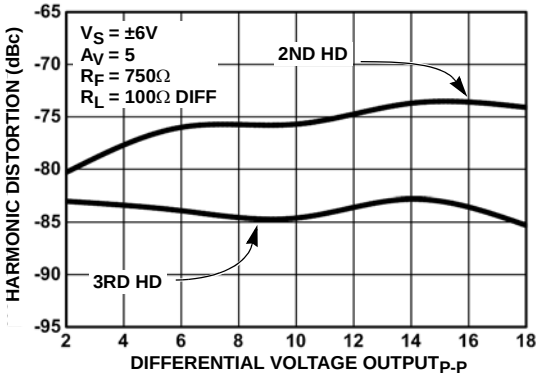


FIGURE 9. HARMONIC DISTORTION @ 3MHz

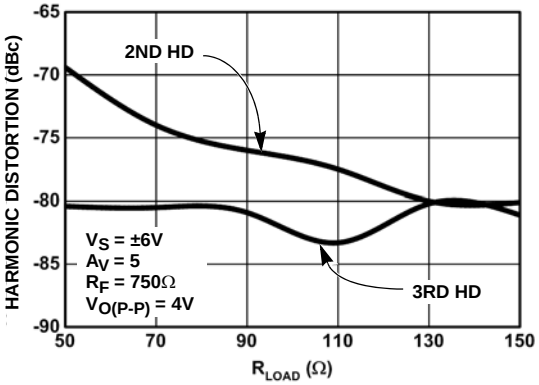


FIGURE 10. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} @ 3MHz

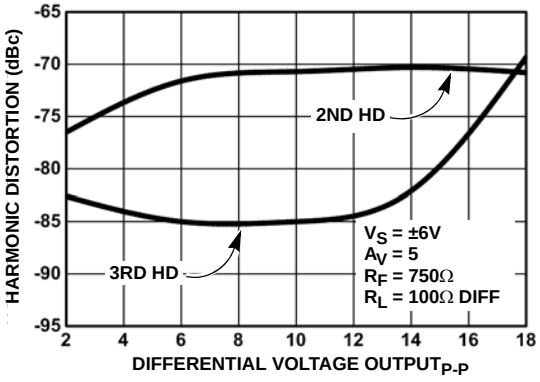


FIGURE 11. HARMONIC DISTORTION @ 5MHz

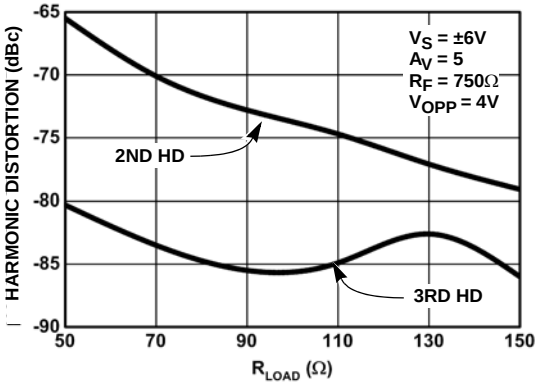


FIGURE 12. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} @ 5MHz

Typical Performance Curves (Continued)

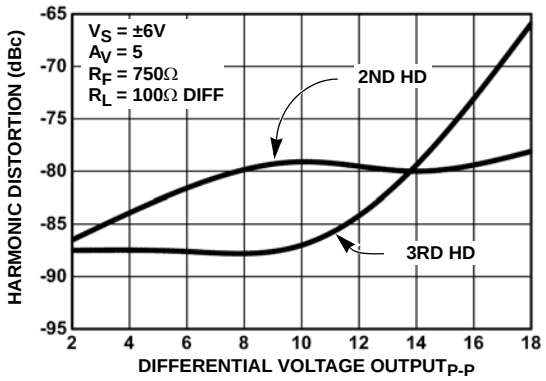


FIGURE 13. HARMONIC DISTORTION @ 10MHz

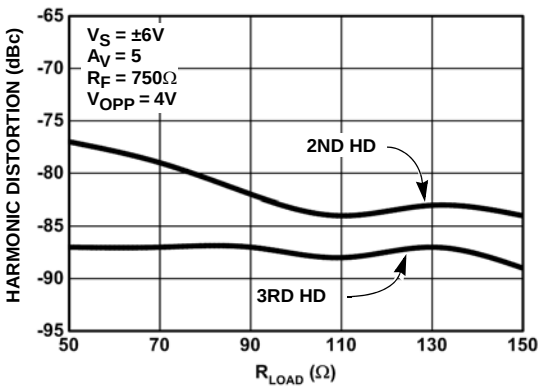


FIGURE 14. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} @ 10MHz

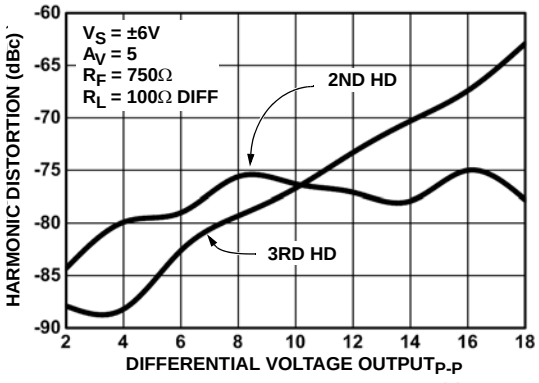


FIGURE 15. HARMONIC DISTORTION @ 17MHz

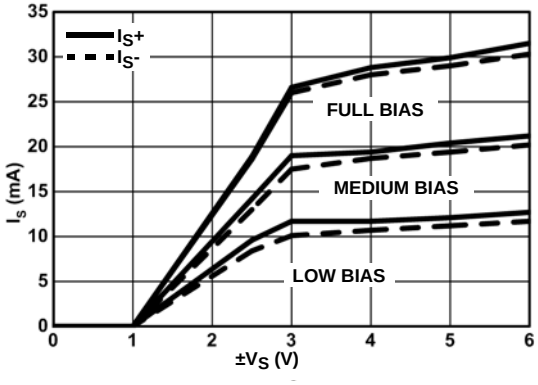


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

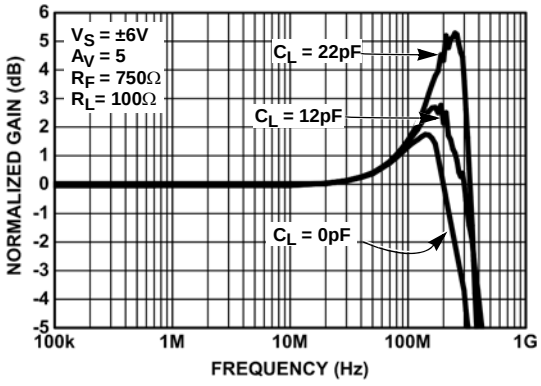


FIGURE 17. FREQUENCY RESPONSE WITH VARIOUS C_L (FULL BIAS MODE)

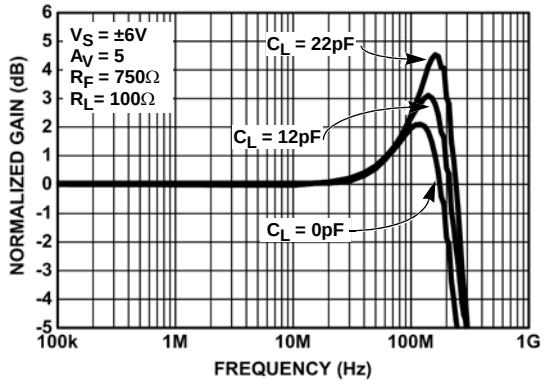


FIGURE 18. FREQUENCY RESPONSE vs VARIOUS C_L (MEDIUM BIAS MODE)

Typical Performance Curves (Continued)

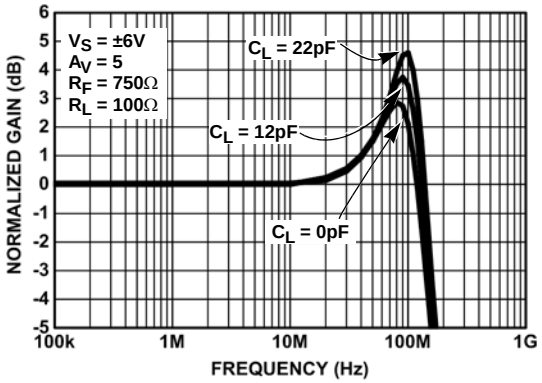


FIGURE 19. FREQUENCY RESPONSE WITH VARIOUS C_L (LOW BIAS MODE)

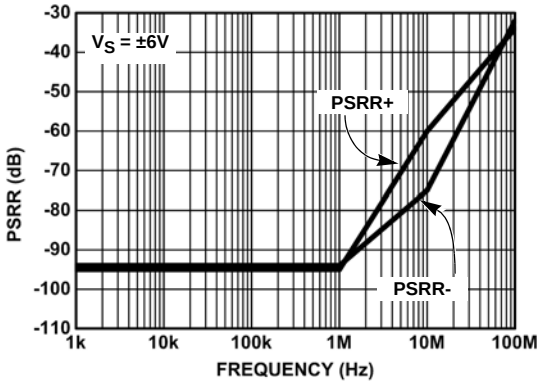


FIGURE 20. PSRR vs FREQUENCY

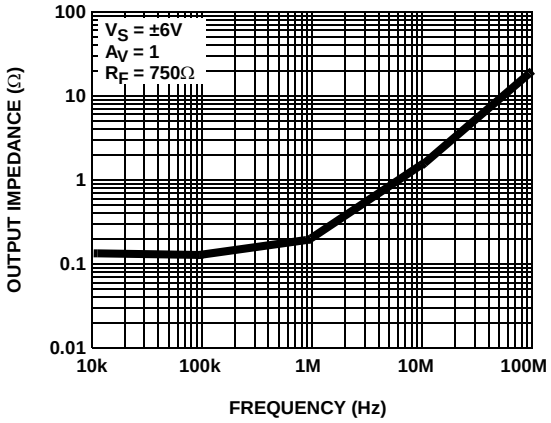


FIGURE 21. OUTPUT IMPEDANCE vs FREQUENCY

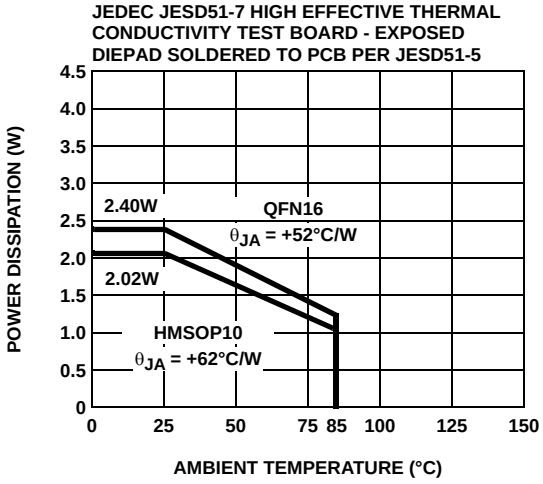


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Product Description

The ISL1571 is a dual operational amplifier designed for line driving in OFDM and PLC solutions. It is a dual current mode feedback amplifier with low distortion while drawing moderately low supply current. It is built using Intersil's proprietary complimentary bipolar process and is offered in industry standard pinouts. Due to the current feedback architecture, the ISL1571 closed-loop 3dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the "Typical Performance Curves" on page 4, show the effect of varying both R_F and R_G. The 3dB bandwidth is somewhat dependent on the power supply voltage.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below 0.25". The power supply pins must be well bypassed to reduce the risk of oscillation. A 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor is adequate for each supply pin. During power-up, it is necessary to limit the slew rate of the rising power supply to within 1V/µs. If the power supply rising time is undetermined, a series 10Ω resistor on the power supply line can be used to ensure the proper power supply rise time.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input. This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors

should be avoided because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the ISL1571 when operating in the non-inverting configuration.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not “seen” by the amplifier.

Feedback Resistor Values

The ISL1571 has been designed and specified with $R_F = 750\Omega$ for $A_V = +5$. This value of feedback resistor yields extremely flat frequency response with 1dB peaking out to 250MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. See the curves in the “Typical Performance Curves” section, beginning on page 4, which show 3dB bandwidth and peaking vs frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3dB bandwidth drop off at high temperature, the ISL1571 was designed to have little supply current variations with temperature. An immediate benefit is the 3dB bandwidth does not drop off drastically with temperature.

Supply Voltage Range

The ISL1571IRZ has been designed to operate with supply voltages from ±2.25V to ±6V nominal. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages.

Single Supply Operation

If a single supply is desired, values from +4.5V to +12V nominal can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either:

1. DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or:
2. Ensure the driving signal is within the common mode range of the ISL1571. ISL1571IUEZ must be used in single supply applications.

PLC Modem Applications

The ISL1571 is designed as a line driver for PLC modems. It is capable of outputting 450mA of output current with a typical supply voltage headroom of 1.3V. It can achieve -85dBc of distortion at low 7.1mA of supply current per amplifier.

The average line power requirement for the PLC application is 13dBm (20mW) into a 100Ω line. The average line voltage is $1.41V_{RMS}$. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:2 is selected. The circuit configuration is shown in Figure 23.

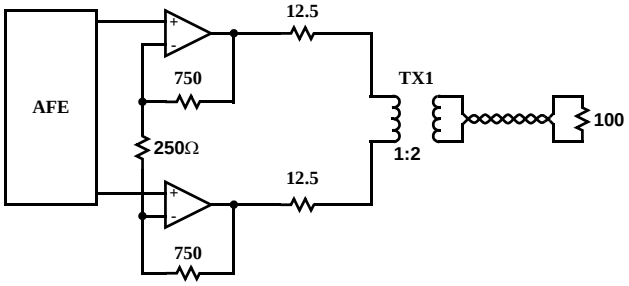
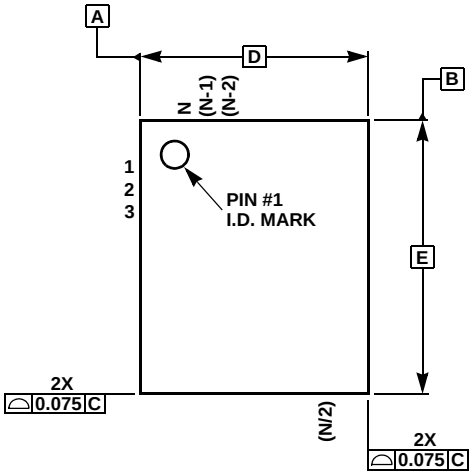
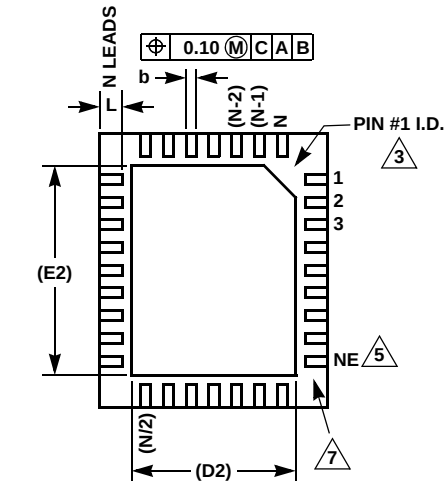


FIGURE 23. CIRCUIT CONFIGURATION

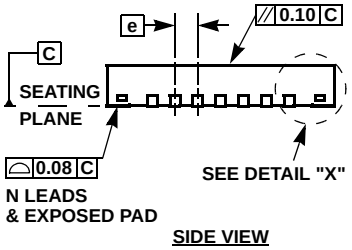
QFN (Quad Flat No-Lead) Package Family



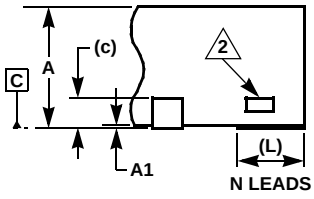
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN38	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	MILLIMETERS					TOLERANCE	NOTES
	QFN28	QFN24	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

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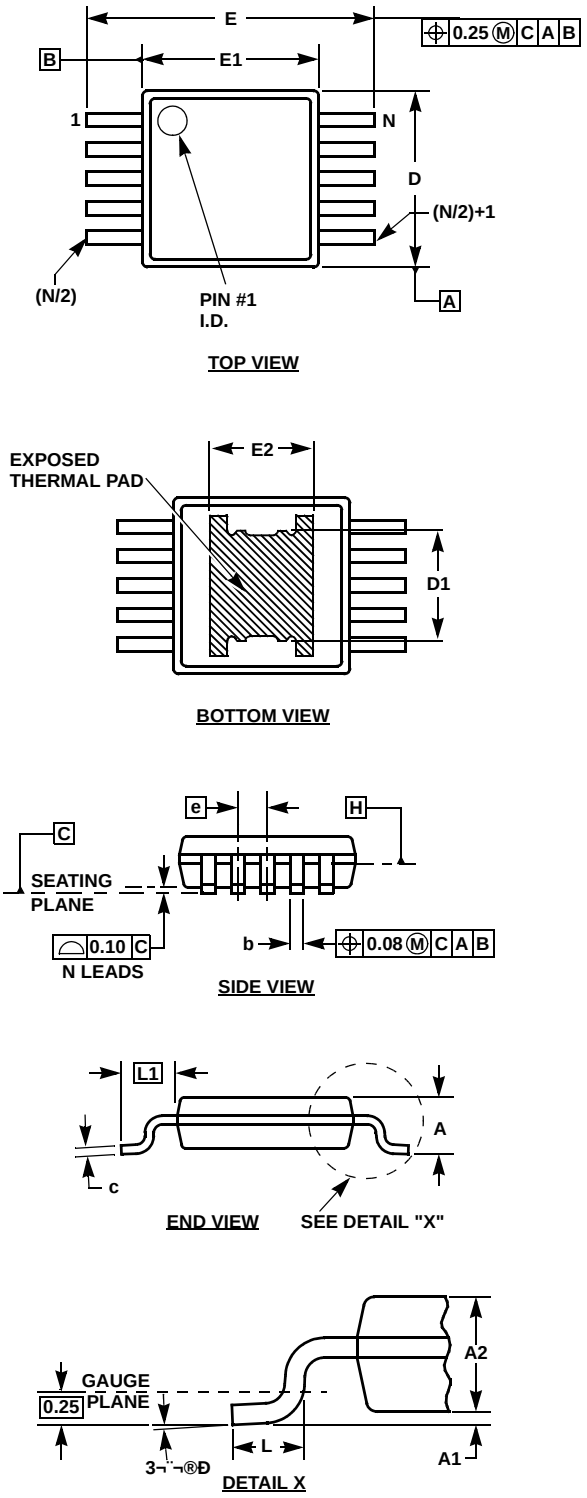
NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

HMSOP (Heat-Sink MSOP) Package Family



MDP0050

HMSOP (HEAT-SINK MSOP) PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	HMSOP8	HMSOP10		
A	1.00	1.00	Max.	-
A1	0.075	0.075	+0.025/-0.050	-
A2	0.86	0.86	±0.09	-
b	0.30	0.20	+0.07/-0.08	-
c	0.15	0.15	±0.05	-
D	3.00	3.00	±0.10	1, 3
D1	1.85	1.85	Reference	-
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
E2	1.73	1.73	Reference	-
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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