Single Event and Total Dose Hardened, High-Speed, Dual Output PWMs

IS-1825ASRH, IS-1825BSRH, IS-1825BSEH, ISL71823ASRH, ISL71823BSRH

The single event and total dose hardened pulse width modulators are designed to be used in high frequency, switching power supplies in either voltage or current-mode configurations. These designs include a precision voltage reference, a low power start-up circuit, a high frequency oscillator, a wide-band error amplifier and a fast current-limit comparator.

The IS-1825ASRH, IS-1825BSRH and IS-1825BSEH feature dual, alternating output operating from zero to less than 50% duty-cycle, while the ISL71823ASRH and ISL71823BSRH features dual, in-phase output operating from zero to less than 100% duty cycle. The “B” versions test the delay from clock out to PWM output switching after power has been applied to the modulator (t_{PWM}) (see Figure 3). The ISL-825BSEH is wafer-by-wafer acceptance tested to 50krad(Si) at a low dose rate of 10mrad(Si)/s.

Constructed with the Intersil Rad-hard Silicon Gate (RSG) dielectrically isolated BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide a high level of immunity to single event transients. All specified parameters are guaranteed and tested for 300krad(Si) total dose performance.

Related Literature

- IS-1825ASRH Radiation Test Report
- IS-1825ASRH Single Event Effects Report

Features

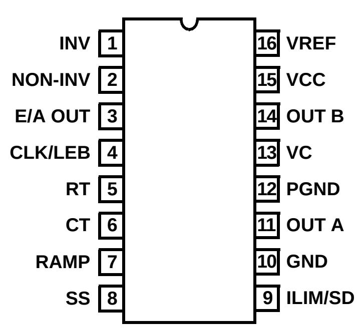
- Electrically screened to DLA SMD# 5962-02511
- QML qualified per MIL-PRF-38535 requirements
- EH version is wafer-by-wafer acceptance tested to 50krad(Si) (LDR)
- Radiation environment
  - High dose rate (50-300rad(Si)/s). . . . . 300krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . .50krad(Si)
  - Latch-up immune. . . . . dielectrically isolated
  - SEU immune. . . . . LET = 35MeV/mg/cm^2 (max)
- Oscillator frequency . . . . 1MHz (max)
- High output drive current . . . . 1A peak (typ)
- Low start-up current. . . . . 300µA (max)
- Undervoltage lockout
  - Start threshold . . . . 8.8V (max)
  - Stop threshold . . . . 7.6V (min)
  - Hysteresis . . . . 300mV (min)
- Pulse-by-pulse current limiting
- Programmable leading edge blanking

Applications

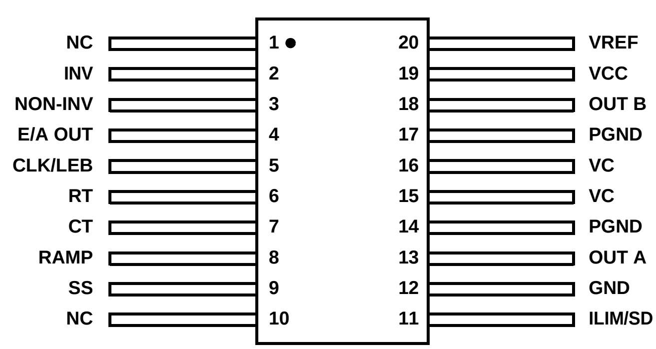
- Voltage or current-mode switching power supplies
- Control of high current MOSFET drivers
- Motor speed and direction control

Pin Configurations

IS1-1825ASRH, IS1-1825BSRH, IS-1825BSEH
ISL71823BSRHVD, ISL71823ASRHQD
(CDIP2-T16 SBDIP)
TOP VIEW



IS9-1825ASRH, IS9-1825BSRH, IS9-1825BSEH
ISL71823ASRHQF, ISL71823BSRHVF
(CDFP4-F20 FLATPACK)
TOP VIEW



Ordering Information

ORDERING/SMD NUMBERS (Note 1)	PART NUMBER (Notes 2, 3)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
IS0-1825ASRH/SAMPLE	IS0-1825ASRH/SAMPLE	-50 to +125		
5962F0251101V9A	IS0-1825ASRH-Q	-50 to +125	DIE	
5962F0251101QEC	IS1-1825ASRH-8	-50 to +125	16 Ld SBDIP	D16.3
5962F0251101QXC	IS9-1825ASRH-8	-50 to +125	20 Ld Flatpack	K20.A
5962F0251101VEC	IS1-1825ASRH-Q	-50 to +125	16 Ld SBDIP	D16.3
5962F0251101VXC	IS9-1825ASRH-Q	-50 to +125	20 Ld Flatpack	K20.A
IS1-1825ASRH/PROTO	IS1-1825ASRH/PROTO	-50 to +125	16 Ld SBDIP	D16.3
IS9-1825ASRH/PROTO	IS9-1825ASRH/PROTO	-50 to +125	20 Ld Flatpack	K20.A
5962F0251102QEC	ISL71823ASRHQD	-50 to +125	16 Ld SBDIP	D16.3
5962F0251102QXC	ISL71823ASRHQF	-50 to +125	20 Ld Flatpack	K20.A
5962F0251102VEC	ISL71823ASRHVD	-50 to +125	16 Ld SBDIP	D16.3
5962F0251102VXC	ISL71823ASRHVF	-50 to +125	20 Ld Flatpack	K20.A
5962F0251102V9A	ISL71823ASRHVX	-50 to +125	DIE	
ISL71823ASRHD/PROTO	ISL71823ASRHD/PROTO	-50 to +125	16 Ld SBDIP	D16.3
ISL71823ASRHF/PROTO	ISL71823ASRHF/PROTO	-50 to +125	20 Ld Flatpack	K20.A
ISL71823ASRHX/SAMPLE	ISL71823ASRHX/SAMPLE	-50 to +125	DIE	
5962F0251103V9A	IS0-1825BSRH-Q	-50 to +125	DIE	
5962F0251103QEC	IS1-1825BSRH-8	-50 to +125	16 Ld SBDIP	D16.3
5962F0251103QXC	IS9-1825BSRH-8	-50 to +125	20 Ld Flatpack	K20.A
5962F0251103VEC	IS1-1825BSRH-Q	-50 to +125	16 Ld SBDIP	D16.3
5962F0251103VXC	IS9-1825BSRH-Q	-50 to +125	20 Ld Flatpack	K20.A
5962F0251104QEC	ISL71823BSRHQD	-50 to +125	16 Ld SBDIP	D16.3
5962F0251104QXC	ISL71823BSRHQF	-50 to +125	20 Ld Flatpack	K20.A
5962F0251104VEC	ISL71823BSRHVD	-50 to +125	16 Ld SBDIP	D16.3
5962F0251104VXC	ISL71823BSRHVF	-50 to +125	20 Ld Flatpack	K20.A
5962F0251104V9A	ISL71823BSRHVX	-50 to +125	DIE	
5962F0251105V9A	IS0-1825BSEH-Q	-50 to +125	DIE	
5962F0251105VEC	IS1-1825BSEH-Q	-50 to +125	16 Ld SBDIP	D16.3
5962F0251105VXC	IS9-1825BSEH-Q	-50 to +125	20 Ld Flatpack	K20.A
5962F1222801VXC	ISL70417SEHVF	-55 to +125	14 Ld Flatpack	K14.A

NOTES:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.
2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. For Moisture Sensitivity Level (MSL), please see device information page for IS-1825ASRH, IS-1825BSRH IS-1825BSEH ISL71823ASRH ISL71823BSRH. For more information on MSL please see tech brief TB363.

Typical Performance Curves

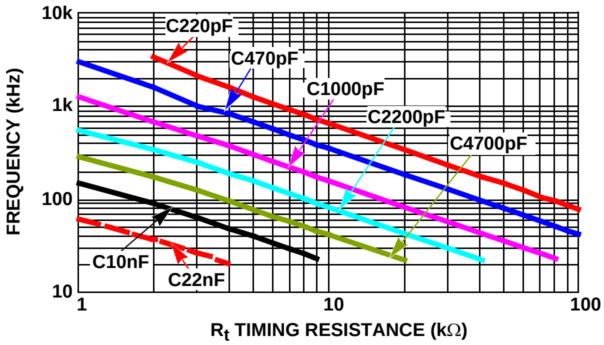


FIGURE 1. OSCILLATOR FREQUENCY vs R_t AND C_t

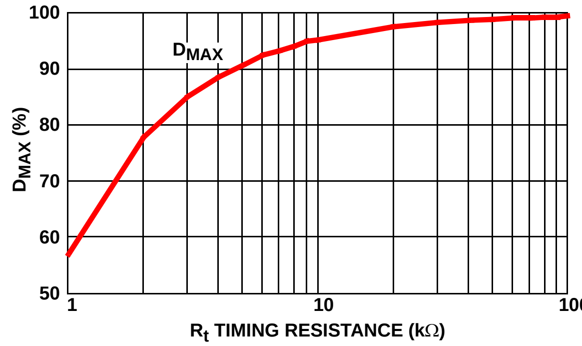


FIGURE 2. MAXIMUM DUTY CYCLE vs R_t

Timing Diagram

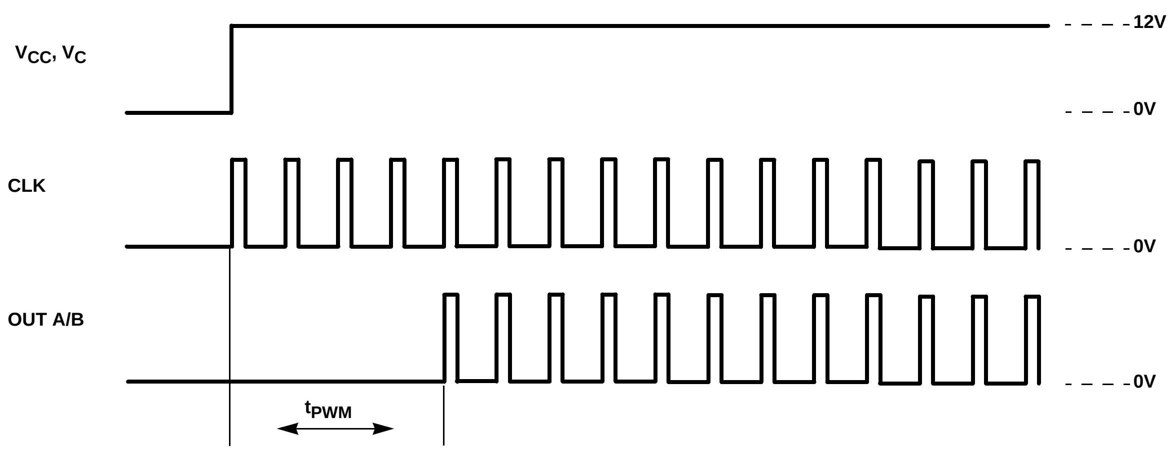


FIGURE 3. t_{PWM} DELAY TIMING DIAGRAM

Die Characteristics

Die Dimensions

4310µm x 5840µm (170 mils x 230 mils)
Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kA ± 1.0kA

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 16.0kA ± 2kA

BACKSIDE FINISH

Silicon

PROCESS

Radiation Hardened Silicon Gate,
Dielectric Isolation

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Unbiased (DI)

ADDITIONAL INFORMATION

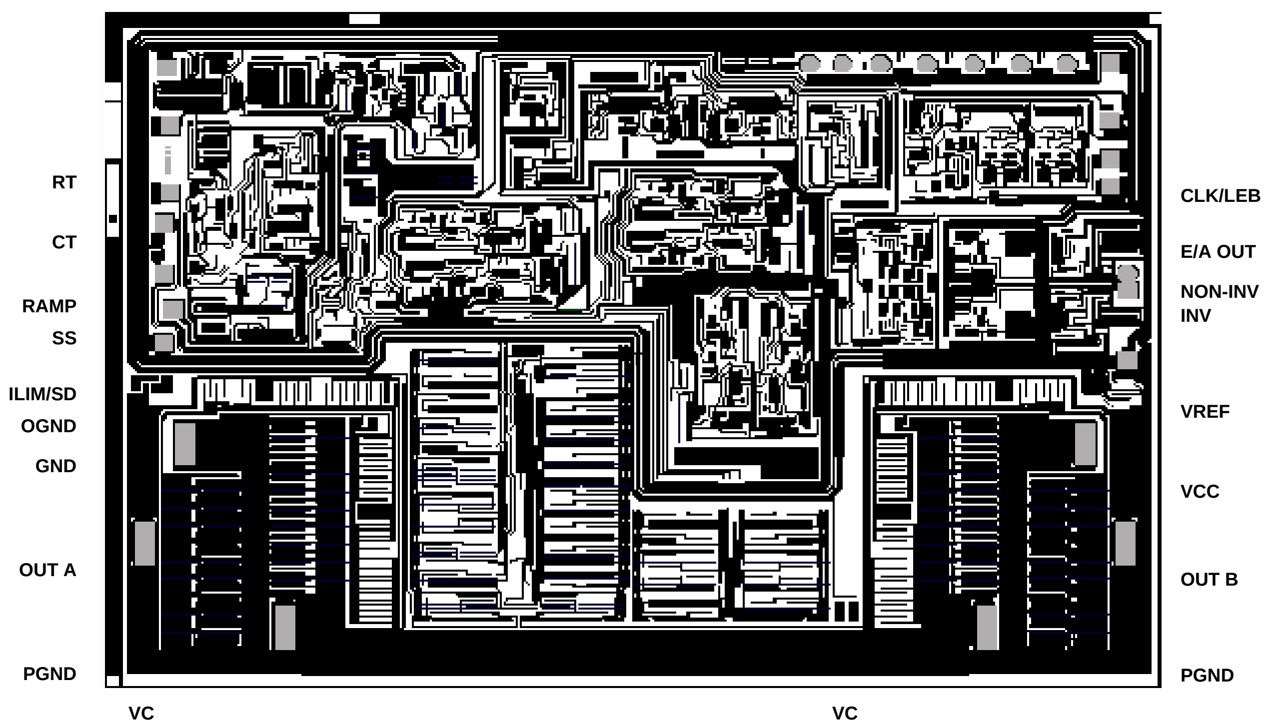
WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

Transistor Count:

585

Metallization Mask Layout



NOTES:

1. Both the OGND (oscillator ground) and the GND (control circuit ground) pads must be bonded to ground. These pads are both bonded to the GND pin on the packaged devices.
2. All double-sized bond pads must be double bonded for current sharing purposes.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Revision.

DATE	REVISION	CHANGE
April 23, 2013	FN9065.5	Removed Part number IS-1825ASEH and added part numbers IS-1825BSEH, IS-1825BSRH, and ISL71823BSRH to ordering information table on page page 2. SMD numbers in Ordering Information table corrected. Added timing diagram for CLK to OUT delay t_{PWM}
April 5, 2012	FN9065.4	Updated to new Intersil template Added Part IS-1825ASEH to Title and ordering information Changed DSCC to DLA.
September 25, 2008	FN9065.4	Added typical oscillator performance curves. Updated ordering information by adding pkg and pkg dwg number and also added sample parts.
February 19, 2008	FN9065.3	Added ISL71823ASRH which is a metal option of the IS-1825ASRH.
June 14, 2005	FN9065.2	Cosmetic edit only. Changed "u" to "µ" on pg 1 Features Added ISL71823ASRH which is a metal option of the IS-1825ASRH.
June 14, 2005	FN9065.1	Removed "Trimmed Oscillator Discharge Current" from the Features section of both datasheets since the oscillator is not trimmed. Cosmetic edit only. Changed "u" to "µ" on pg 1 Features
June 21, 2002	FN9065.0	Initial Release

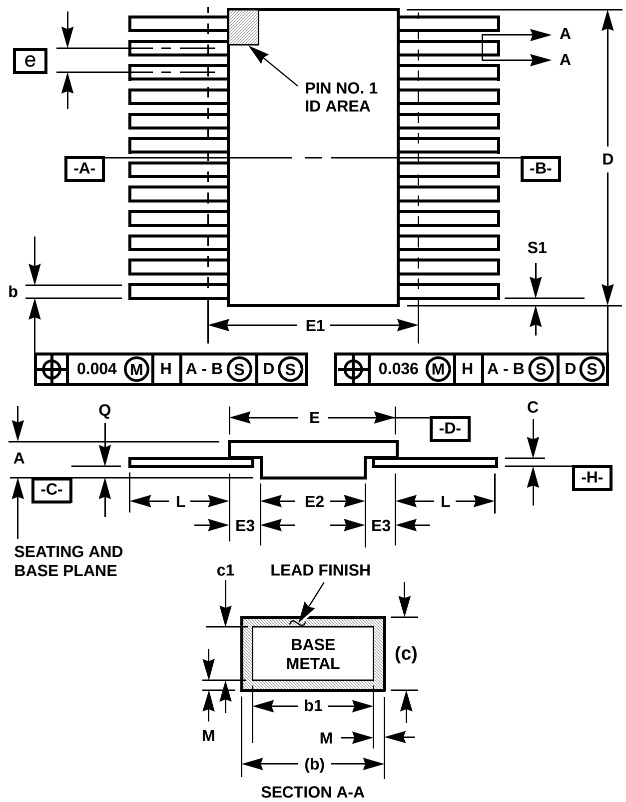
About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

Ceramic Metal Seal Flatpack Packages (Flatpack)



K20.A MIL-STD-1835 CDFP4-F20 (F-9A, CONFIGURATION B)
20 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.540	-	13.72	3
E	0.245	0.300	6.22	7.62	-
E1	-	0.330	-	8.38	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	20		20		-

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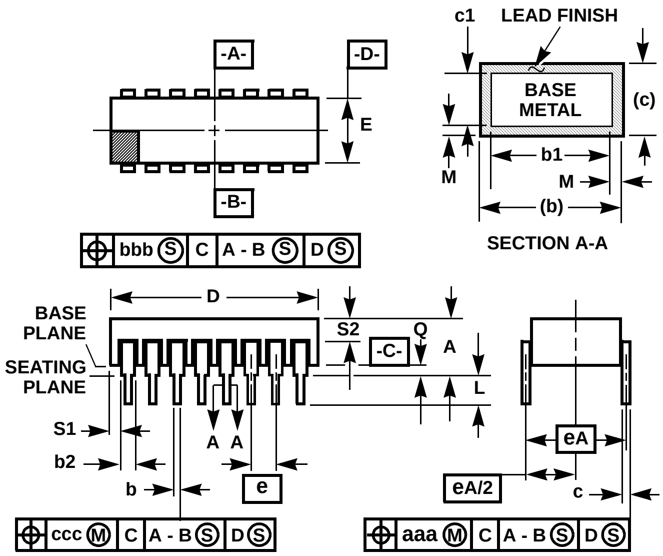
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Package Outline Drawing

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.