AS1312

Ultra Low Quiescent Current, Hysteretic DC-DC Step-Up Converter

1 General Description

The AS1312 is an ultra low I_Q hysteretic step-up DC-DC converter.

The AS1312 achieves an efficiency of up to 94% and is designed to operate from a +0.7V to +5.0V supply, the output voltage is fixed in 50mV steps from +2.5V to 5.0V.

In order to save power the AS1312 features a shutdown mode, where it draws less than 100nA. In shutdown mode the battery is not connected to the output.

If the input voltage exceeds the output voltage the device is in a feedthrough mode and the input is directly connected to the output voltage.

In light load operation, the device enters a sleep mode when most of the internal operating blocks are turned off in order to save power. This mode is active approximately 50µs after a current pulse provided that the output is in regulation.

The AS1312 also offers an adjustable low battery detection. If the battery voltage decreases below a threshold defined by two external resistors on pin LBI, the LBO output is pulled to logic low. LBO is working as Power-OK when LBI is connected to GND.

The AS1312 is available in a 8-pin (2x2) TDFN and a 0.4mm pitch 8-pin WL-CSP package.

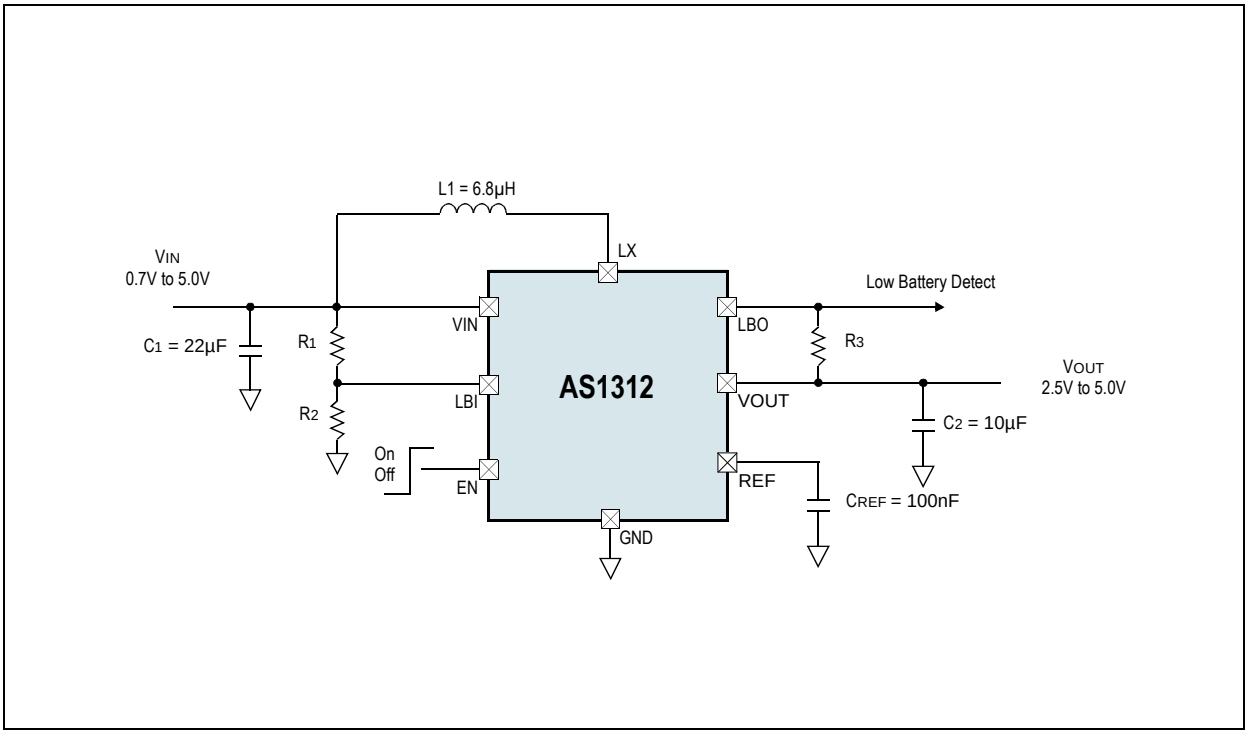
2 Key Features

- Input voltage range: 0.7V to 5.0V
- Fixed output voltage range: 2.5V to 5.0V
- Peak output current: 200mA
- Quiescent current: 1µA
- Shutdown current: < 100nA
- Up to 94% efficiency
- Output disconnect in shutdown
- Feedthrough mode when V_{IN} > V_{OUT}
- Adjustable low battery detection or Power-OK output selectable
- No external diode or transistor required
- Over temperature protection
- Packages:
  - 8-pin (2x2) TDFN
  - 8-pin WL-CSP with 0.4mm pitch

3 Applications

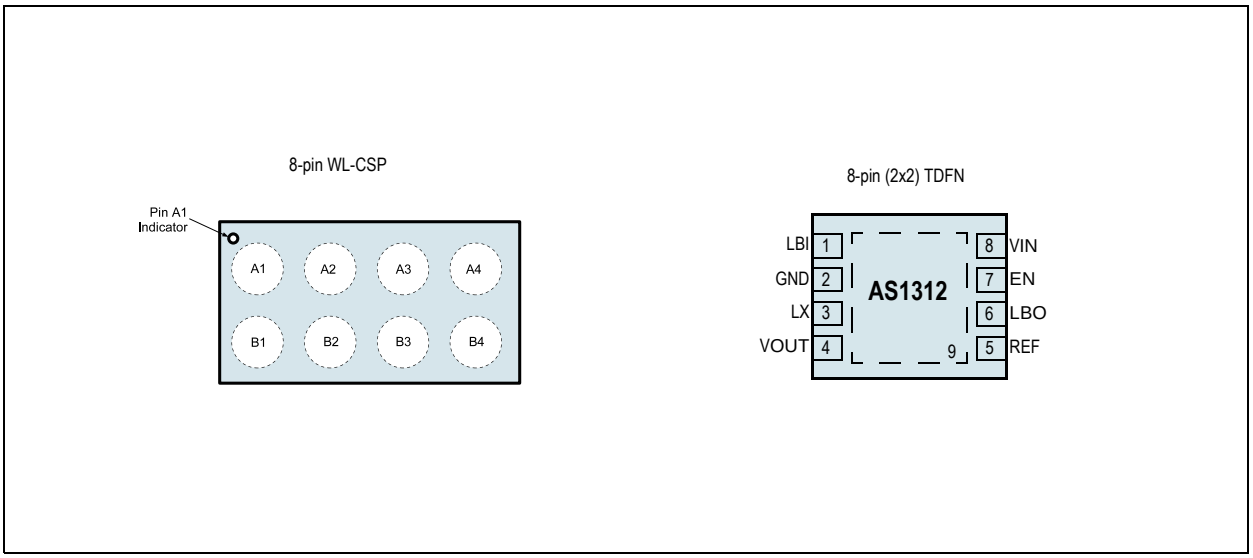
The AS1312 is an ideal solution for handheld devices and battery powered products.

Figure 1. AS1312 - Typical Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number		Pin Name	Description
WL-CSP	TDFN		
A1	1	LBI	**Low Battery Comparator Input**. 0.6V Threshold. May not be left floating. If connected to GND, LBO is working as Power Output OK.
A2	2	GND	**Ground**
A3	3	LX	**External Inductor Connector.**
A4	4	VOUT	**Output Voltage.** Decouple VOUT with a ceramic capacitor as close as possible to VOUT and **GND**.
B4	5	REF	**Reference Pin.** Connect a 100nF ceramic capacitor to this pin.
B3	6	LBO	**Low Battery Comparator Output**. Open-drain output.
B2	7	EN	**Enable Pin**. Logic controlled shutdown input. 1 = Normal operation; 0 = Shutdown; shutdown current <100nA.
B1	8	VIN	**Battery Voltage Input.** Decouple VIN with a ceramic capacitor as close as possible to VIN and GND.
-	9	NC	**Exposed Pad.** This pad is not connected internally. Can be left floating or connect to **GND** to achieve an optimal thermal performance.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
Electrical Parameters					
VIN, VOUT, EN, LBI, LBO to GND		-0.3	+7	V	
LX, REF to GND		-0.3	VOUT + 0.3	V	
Input Current (latch-up immunity)		-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge					
Electrostatic Discharge HBM		±2		kV	Norm: MIL 883 E method 3015
Temperature Ranges and Storage Conditions					
Thermal Resistance θ_{JA}	TDFN	60		°C/W	Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design.
	WL-CSP	97			
Junction Temperature			+125	°C	
Storage Temperature Range		-55	+150	°C	for 8-pin (2x2) TDFN
		-55	+125	°C	for 8-pin WL-CSP
Package Body Temperature			+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing		5	85	%	
Moisture Sensitive Level		1			Represents a maximum floor life time of unlimited

6 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed by production tests or SQC (Statistical Quality Control) methods.

V_{IN} = *1.5V, C1 = C2 = 22µF,* C_{REF} *= 100nF, Typical values are at* T_{AMB} *= +25ºC. Unless otherwise specified.* All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{AMB}	Operating Temperature Range		-40		85	°C
T_J	Operating Junction Temperature Range		-40		125	°C
Input						
V_{IN}	Input Voltage Range		0.7		5.0	V
	Minimum Startup Voltage	T_{AMB} = +25°C		0.9		V
Regulation						
V_{OUT}	Output Voltage Range		2.5		5.0	V
	Output Voltage Tolerance	I_{LOAD} = 0mA to 10mA, T_{AMB} = +25°C	-2		+2	%
		I_{LOAD} = 0mA to 10mA	-4		+4	%
		I_{LOAD} = 0mA to 30mA, T_{AMB} = -20°C to +60°C	-2		+2	%
	V_{OUT} Lockout Threshold[1]	Rising Edge		2.45		V
Operating Current						
I_Q	Quiescent Current V_{IN}	V_{OUT} = 1.02xV_{OUTNOM}, REF = 0.99xV_{OUTNOM}, T_{AMB} = +25°C			100	nA
	Quiescent Current V_{OUT}	V_{OUT} = 5V, No load, T_{AMB} = +25°C	0.7	1	1.3	µA
I_{SHDN}	Shutdown Current	T_{AMB} = +25ºC			100	nA
Switches						
R_{ON}	NMOS	V_{OUT} = 5V		0.4		Ω
	PMOS			0.45		Ω
	NMOS maximum on-time		3.3	4.0	4.6	µs
I_{PEAK}	Peak current limit			400		mA
	Zero crossing current		5	20	35	mA
Enable, Reference						
V_{ENH}	EN input voltage 'high'		0.7			V
V_{ENL}	EN input voltage 'low'				0.1	V
I_{EN}	EN input bias current	EN = 5V, T_{AMB} = +25°C			100	nA
I_{REF}	REF input bias current	REF = 0.99xV_{OUTNOM}, T_{AMB} = +25°C			100	nA
Low Battery & Power-OK						
V_{LBI}	LBI threshold	Falling edge	0.57	0.6	0.63	V
	LBI hysteresis			25		mV
I_{LBI}	LBI leakage current	LBI ≤ V_{IN} or V_{OUT} (which ever is higher), T_{AMB} = +25°C			100	nA
V_{LBO}	LBO voltage low[2]	I_{LBO} = 1mA		5	20	mV

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LBO}	LBO leakage current	T_{AMB} = +25°C			100	nA
	Power-OK threshold	LBI = 0V, Falling Edge	87	91	95	%
Thermal Protection						
	Thermal shutdown[3]	10°C Hysteresis		150		°C

1. The regulator is in startup mode until this voltage is reached.

Caution: Do not apply full load current until the device output > 2.5V

2. LBO goes low in startup mode as well as during normal operation if,
   (i) The voltage at the LBI pin is higher than LBI threshold.
   (ii) The voltage at the LBI pin is below 0.1V (connected to GND) and V_{OUT} is below 92.5% of its nominal value.
3. Further switching is inhibited.

7 Typical Operating Characteristics

VOUT = 5.0V, TAMB = +25°C, unless otherwise specified.

Figure 3. Efficiency vs. Output Current

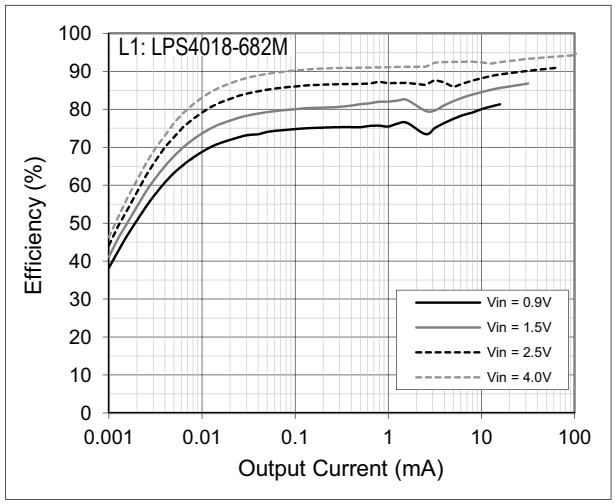


Figure 4. Efficiency vs. Output Current

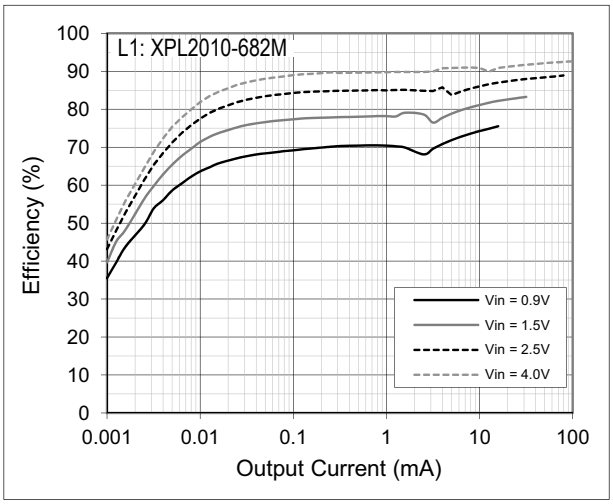


Figure 5. Efficiency vs. Input Voltage

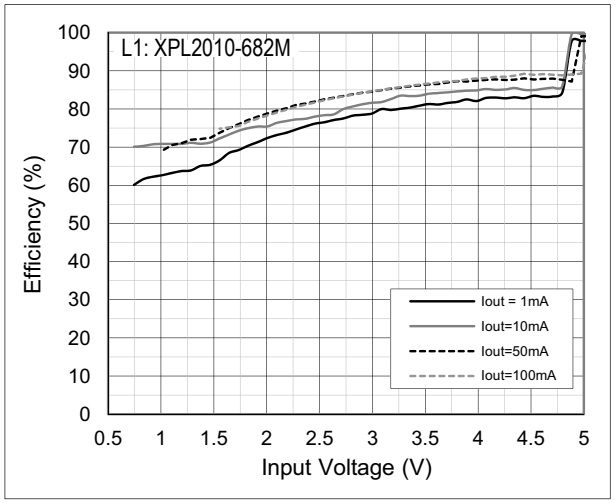


Figure 6. Maximum Output Current vs. Input Voltage

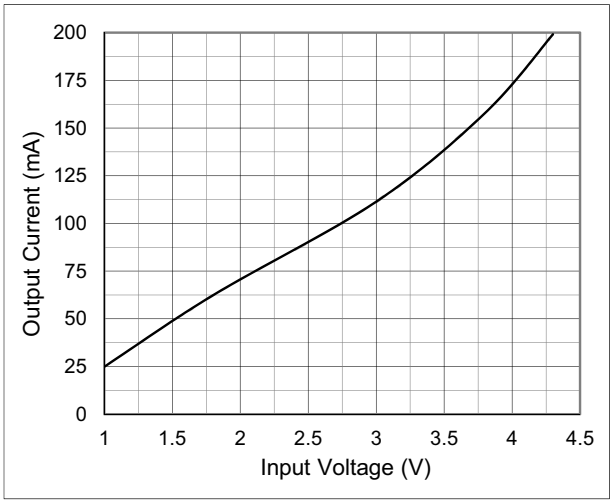


Figure 7. Start-up Voltage vs. Output Current

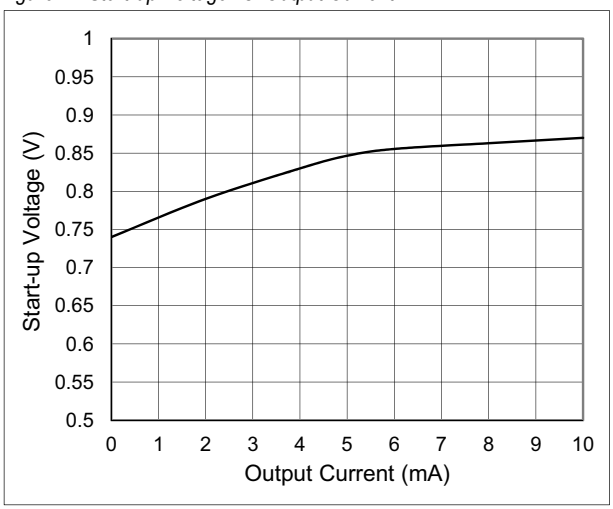
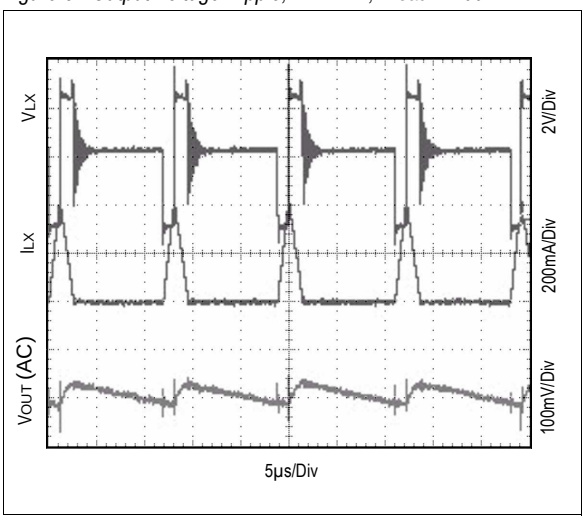


Figure 8. Output Voltage Ripple; VIN = 2V, Rload = 100Ω



8 Detailed Description

8.1 Hysteretic Boost Converter

Hysteretic boost converters are so called because comparators are the active elements used to determine on-off timing via current and voltage measurements. There is no continuously operating fixed oscillator, providing an independent timing reference. As a result, a hysteretic or comparator based converter has a very low quiescent current. In addition, because there is no fixed timing reference, the operating frequency is determined by external component (inductor and capacitors) and also the loading on the output.

Ripple at the output is an essential operating component. A power cycle is initiated when the output regulated voltage drops below the nominal value of VOUT (0.99 x VOUT).

Inductor current is monitored by the control loop, ensuring that operation is always dis-continuous.

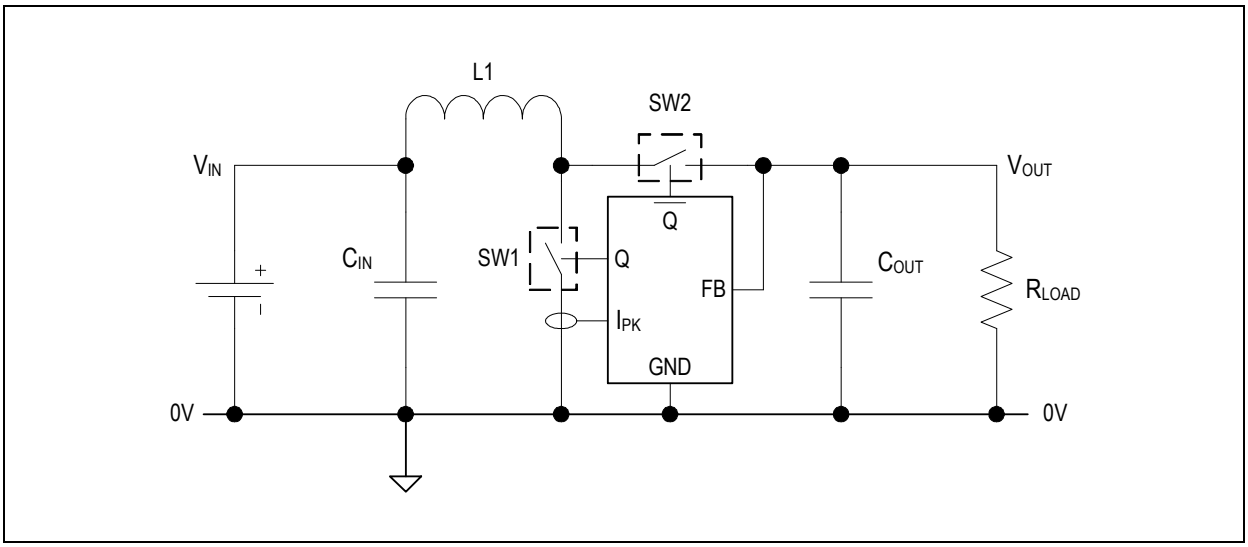
The application circuit shown in Figure 1 will support many requirements. However, further optimization may be useful, and the following is offered as a guide to changing the passive components to more closely match the end requirement.

8.1.1 Input Loop Timing

The input loop consists of the source dc supply, the input capacitor, the main inductor, and the N-channel power switch. The on timing of the N-channel switch is determined by a peak current measurement or a maximum on time. In the AS1312, peak current is 400mA (typ) and maximum on time is 4.2µs (typ). Peak current measurement ensures that the on time varies as the input voltage varies. This imparts line regulation to the converter.

The fixed on-time measurement is something of a safety feature to ensure that the power switch is never permanently on. The fixed on-time is independent of input voltage changes. As a result, no line regulation exists.

Figure 9. Simplified Boost DCDC Architecture



On time of the power switch (Faraday's Law) is given by:

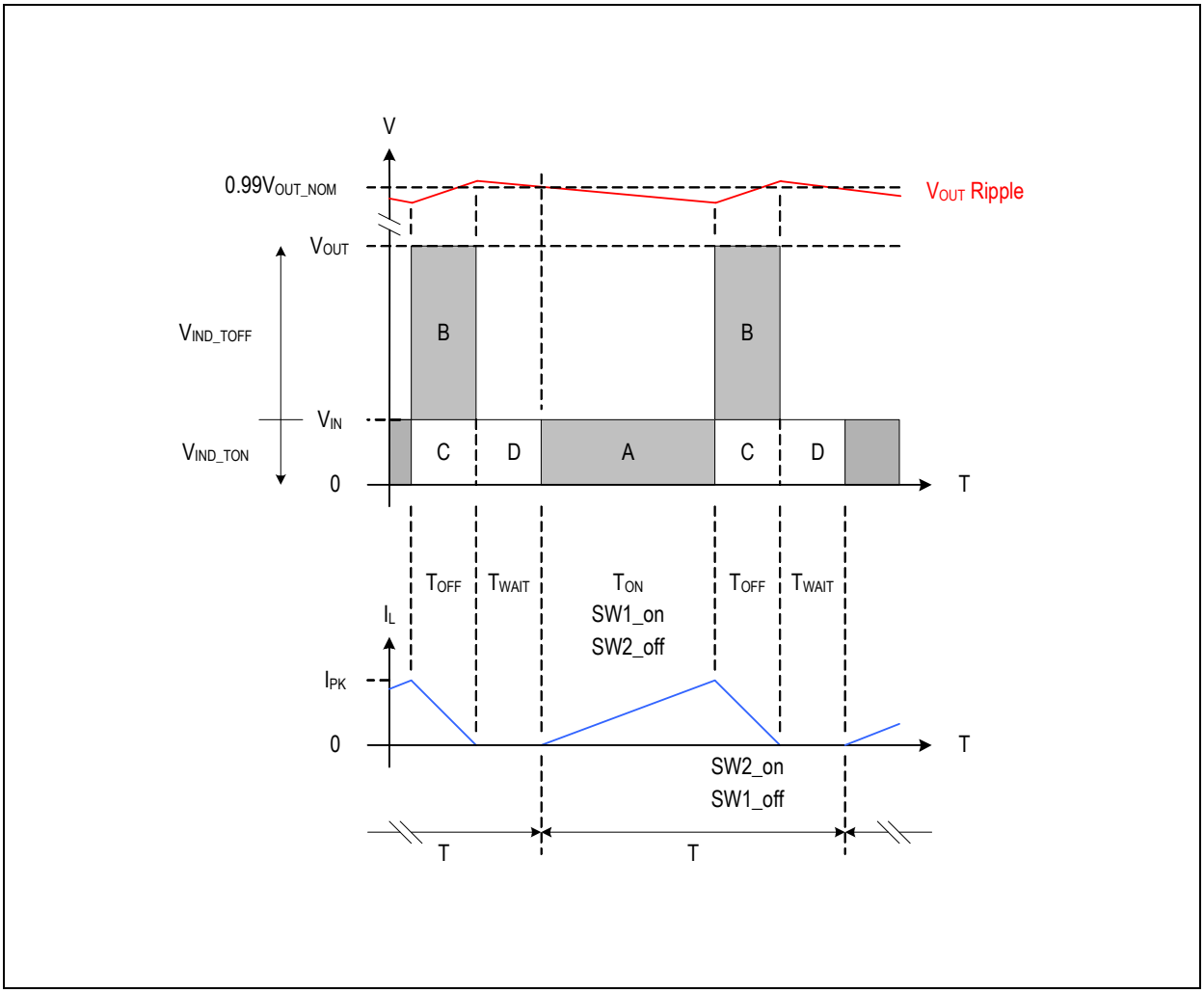
$$T_{ON} = \frac{LI_{PK}}{V_{IN} - (I_{PK}R_{SW1} + I_{PK}R_{L1})} \text{ sec [volts, amps, ohms, Henry]} \quad \textit{(EQ 1)}$$

Applying Min and Max values and neglecting the resistive voltage drop across L1 and SW1;

$$T_{ON\_MIN} = \frac{L_{MIN} I_{PK\_MIN}}{V_{IN\_MAX}} \quad \textit{(EQ 2)}$$

$$T_{ON\_MAX} = \frac{L_{MAX} I_{PK\_MAX}}{V_{IN\_MIN}} \quad \textit{(EQ 3)}$$

Figure 10. Simplified Voltage and Current Waveforms



Another important relationship is the “volt-seconds” law. Expressed as following:

$$V_{ON}T_{ON} = V_{OFF}T_{OFF} \quad \textit{(EQ 4)}$$

Voltages are those measured across the inductor during each time segment. Figure 10 shows this graphically with the shaded segments marked “A & B”. Re-arranging (EQ 4):

$$\frac{T_{ON}}{T_{OFF}} = \frac{V_{OUT} - V_{IN}}{V_{IN}} \quad \textit{(EQ 5)}$$

The time segment called T_{WAIT} in Figure 10 is a measure of the “hold-up” time of the output capacitor. While the output voltage is above the threshold (0.99xV_{OUT}), the output is assumed to be in regulation and no further switching occurs.

8.1.2 Inductor Choice Example

For the AS1312 V_{IN_MIN} = 0.9V, V_{OUT_MAX} = 3.3V, (EQ 5) gives Ton=2.66T_{OFF}.

Let the maximum operating on-time = 1µs.
Note that this is shorter than the minimum limit on-time of 3.6µs. Therefore from (EQ 5), T_{OFF} = 0.376µs. Using (EQ 3), L_{MAX} is obtained:

L_{MAX} = 1.875µH. The nearest preferred value is 2.2µH.

This value provides the maximum energy storage for the chosen fixed on-time limit at the minimum V_{IN}.

Energy stored during the on time is given by:

$$E = 0{,}5L(I_{PK})^2 \quad \textit{Joules (Region A in Figure 10)} \qquad \textit{(EQ 6)}$$

If the overall time period (T_{ON} + T_{OFF}) is T, the power taken from the input is:

$$P_{IN} = \frac{0{,}5L(I_{PK})^2}{T} \quad \textit{Watts} \qquad \textit{(EQ 7)}$$

Assume output power is 0.8 P_{IN} to establish an initial value of operating period T.

T_{WAIT} is determined by the time taken for the output voltage to fall to 0.99xV_{OUT}. The longer the wait time, the lower will be the supply current of the converter. Longer wait times require increased output capacitance. Choose T_{WAIT} = 10% T as a minimum starting point for maximum energy transfer. For very low power load applications, choose T_{WAIT} ≥ 50% T.

8.1.3 Output Loop Timing

The output loop consists of the main inductor, P-channel synchronous switch (or diode if fitted), output capacitor and load. When the input loop is interrupted, the voltage on the LX pin rises (Lenz's Law). At the same time a comparator enables the synchronous switch, and energy stored in the inductor is transferred to the output capacitor and load. Inductor peak current supports the load and replenishes the charge lost from the output capacitor. The magnitude of the current from the inductor is monitored, and as it approaches zero, the synchronous switch is turned off. No switching action continues until the output voltage falls below the output reference point (0.99 x V_{OUT}).

Output power is composed of the dc component (Region C in Figure 10):

$$P_{REGION\_C} = V_{IN}\frac{I_{PK}}{2}\frac{T_{OFF}}{T} \qquad \textit{(EQ 8)}$$

Output power is also composed of the inductor component (Region B in Figure 10), neglecting efficiency loss:

$$P_{REGION\_B} = \frac{0{,}5L(I_{PK})^2}{T} \qquad \textit{(EQ 9)}$$

Total power delivered to the load is the sum of (EQ 8) and (EQ 9):

$$P_{TOTAL} = V_{IN}\frac{I_{PK}}{2}\frac{T_{OFF}}{T} + \frac{0{,}5L(I_{PK})^2}{T} \qquad \textit{(EQ 10)}$$

From (EQ 3) (using nominal values) peak current is given by:

$$I_{PK} = \frac{T_{ON}V_{IN}}{L} \qquad \textit{(EQ 11)}$$

Substituting (EQ 11) into (EQ 10) and re-arranging:

$$P_{TOTAL} = \frac{V^2{}_{IN}T_{ON}}{2TL}(0{,}9T) \qquad \textit{(EQ 12)}$$

0.9T incorporates a wait time T_{WAIT} = 10% T

Output power in terms of regulated output voltage and load resistance is:

$$P_{OUT} = \frac{V^2{}_{OUT}}{R_{LOAD}} \qquad \textit{(EQ 13)}$$

Combining (EQ 12) and (EQ 13):

$$\frac{V^2{}_{OUT}}{R_{LOAD}} = \frac{V^2{}_{IN}T_{ON}}{2TL}(0{,}9T)\eta \qquad \textit{(EQ 14)}$$

Symbol η reflects total energy loss between input and output and is approximately 0.8 for these calculations. Use (EQ 14) to plot duty cycle (T_{ON}/T) changes for various output loadings and changes to V_{IN}.

8.1.4 Input Capacitor Selection

The input capacitor supports the triangular current during the on-time of the power switch, and maintains a broadly constant input voltage during this time. The capacitance value is obtained from choosing a ripple voltage during the on-time of the power switch. Additionally, ripple voltage is generated by the equivalent series resistance (ESR) of the capacitor. For worst case, use maximum peak current values from the datasheet.

$$C_{IN} = \frac{I_{PEAK} T_{ON}}{V_{RIPPLE}} \quad \text{(EQ 15)}$$

Using T_{ON} = 1µs, and I_{PEAK} = 400mA (typ), and V_{RIPPLE} = 50mV, EQ 15 yields:

C_{IN} = 8.0µF

Nearest preferred would be 10µF.

$$V_{PK\_RIPPLE\_ESR} = I_{PK} R_{ESR} \quad \text{(EQ 16)}$$

Typically, the ripple due to ESR is not dominant. ESR for the recommended capacitors (Murata GMR), ESR = 5mΩ to 10mΩ. For the AS1312, maximum peak current is 400mA. Ripple due to ESR is 2.0mV to 4.0mV.

Ripple at the input propagates through the common supply connections, and if too high in value can cause problems elsewhere in the system. The input capacitance is an important component to get right.

8.1.5 Output Capacitor Selection

The output capacitor supports the triangular current during the off-time of the power switch (inductor discharge period), and also the load current during the wait time (Region D in Figure 10) and on-time (Region A in Figure 10) of the power switch.

$$C_{OUT} = \frac{I_{LOAD}(T_{ON} + T_{WAIT})}{(1-0.99)V_{OUT\_NOM}} \quad \text{(EQ 17)}$$

Note: There is also a ripple component due to the equivalent series resistance (ESR) of the capacitor.

8.2 Summary

User Application Defines: V_{IN}min, V_{IN}max, V_{OUT}min, V_{OUT}max, I_{LOAD}min, I_{LOAD}max

Inductor Selection:

Select Max on-time = 0.5µs to 3µs for AS1312. Use (EQ 3) to calculate inductor value.

Use (EQ 5) to determine off-time.

Use (EQ 6) to check that power delivery matches load requirements assume 70% conversion efficiency.

Use (EQ 13) to find overall timing period value of T at min V_{IN} and max V_{OUT} for maximum load conditions.

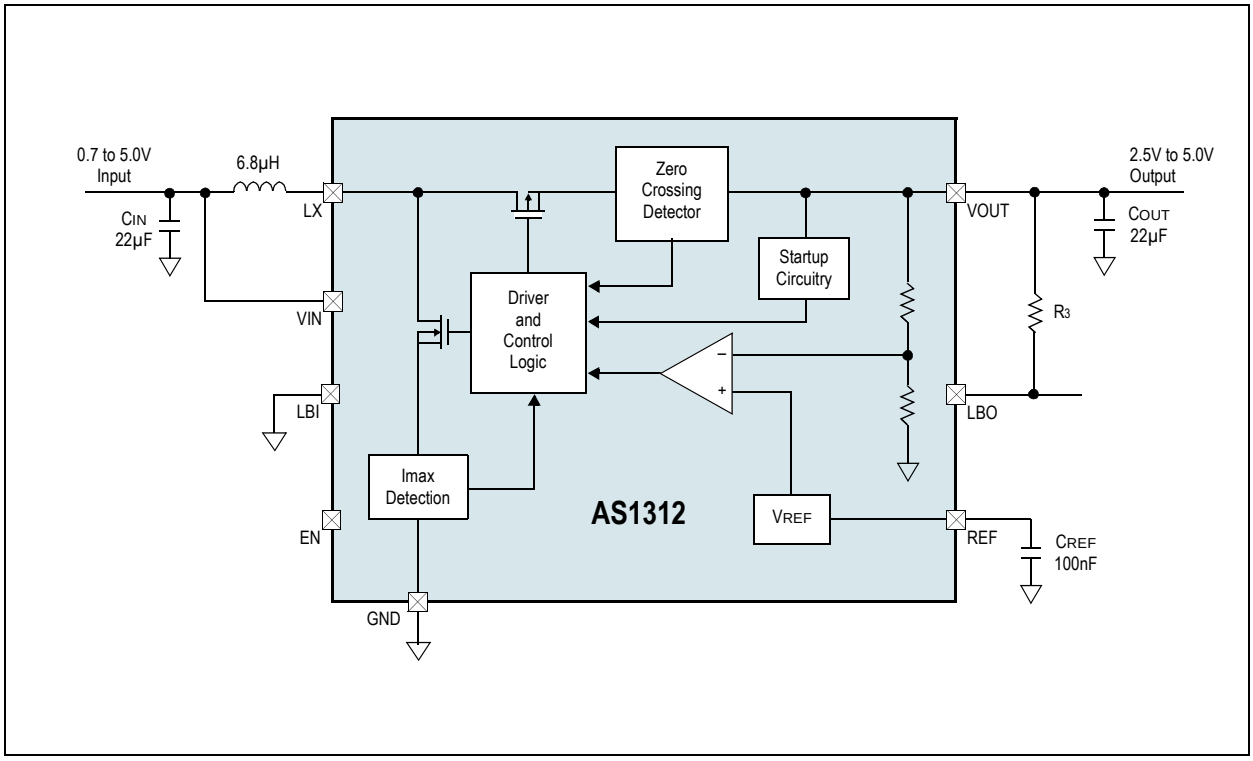
Input Capacitor Selection: Choose a ripple value and use (EQ 14) to find the value.

Output Capacitor Selection: Determine T_{WAIT} via (EQ 6) or (EQ 13), and use (EQ 16) to find the value.

9 Application Information

The AS1312 is available with fixed output voltages from 2.5V to 5.0V in 50mV steps.

Figure 11. AS1312 - Block Diagram



9.1 AS1312 Features

Shutdown.

The part is in shutdown mode while the voltage at pin EN is below 0.1V and is active when the voltage is higher than 0.7V.

Note: EN can be driven above VIN or VOUT, as long as it is limited to less than 5.0V.

Output Disconnect.

During shutdown VOUT is going to 0V and no current from the input source is running through the device.

Feedthrough Mode.

If the input voltage is higher than the output voltage (and the AS1312 is enabled) the supply voltage is connected to the load through the device. To guarantee a proper function of the AS1312 it is not allowed that the supply exceeds the maximum allowed input voltage (5.0V).

In this feedthrough mode the quiescent current is 35µA (typ.). The device goes back into step-up mode when the output voltage is 4% (typ.) below VOUTNOM.

9.1.1 Power-OK and Low-Battery-Detect Functionality

LBO goes low in startup mode as well as during normal operation if:

- The voltage at the LBI pin is below LBI threshold (0.6V). This can be used to monitor the battery voltage.
- LBI pin is connected to GND and VOUT is below 92.5% of its nominal value. LBO works as a power-OK signal in this case.

The LBI pin can be connected to a resistive-divider to monitor a particular definable voltage and compare it with a 0.6V internal reference. If LBI is connected to GND an internal resistive-divider is activated and connected to the output. Therefore, the Power-OK functionality can be realized with no additional external components.

The Power-OK feature is not active during shutdown and provides a power-on-reset function that can operate down to VIN = 0.7V. A capacitor to GND may be added to generate a power-on-reset delay. To obtain a logic-level output, connect a pull-up resistor R3 from pin LBO to pin VOUT. Larger values for this resistor will help to minimize current consumption; a 100kΩ resistor is perfect for most applications (see Figure 13 on page 12).

For the circuit shown in the left of Figure 12, the input bias current into LBI is very low, permitting large-value resistor-divider networks while maintaining accuracy. Place the resistor-divider network as close to the device as possible. Use a defined resistor for R2 and then calculate R1 as:

$$R_1 = R_2 \cdot \left(\frac{V_{IN}}{V_{LBI}} - 1\right) \qquad \text{(EQ 18)}$$

Where:

V_{LBI} is 0.6V

Figure 12. Typical Application with adjustable Battery Monitoring

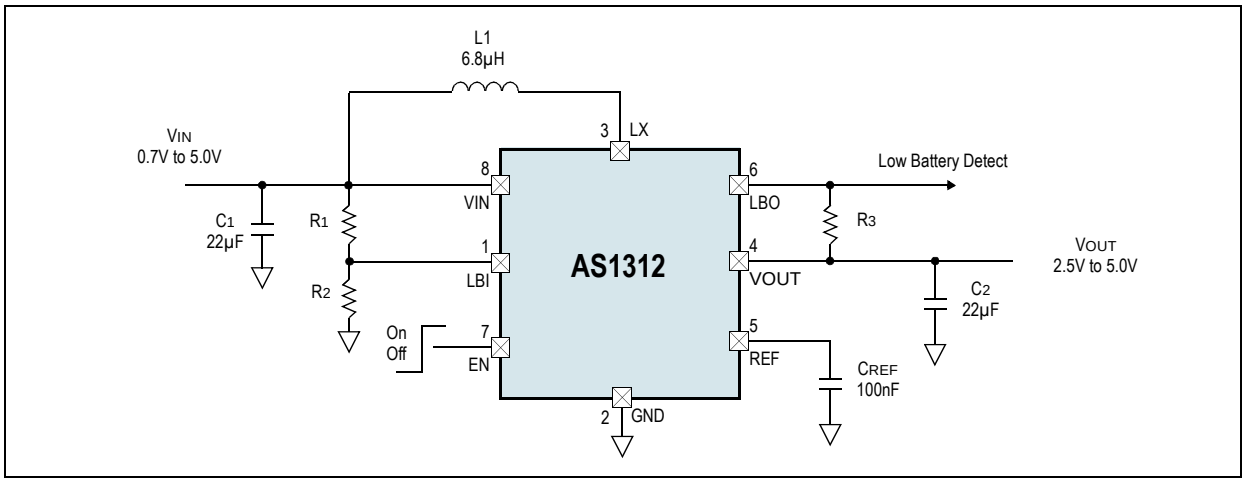
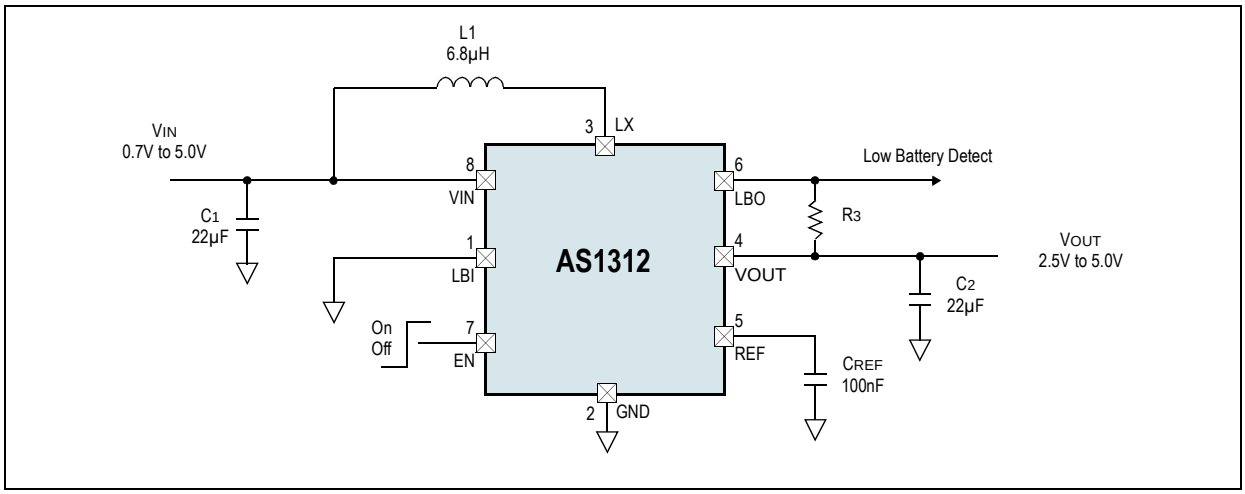


Figure 13. Typical Application with LBO working as Power-OK



9.1.2 Thermal Shutdown

To prevent the AS1312 from short-term misuse and overload conditions the chip includes a thermal overload protection. To block the normal operation mode all further switching is inhibited for output voltage above VOUT lockout threshold. The device is in thermal shutdown when the junction temperature exceeds 150°C. To resume the normal operation the temperature has to drop below 140°C.

A good thermal path has to be provided to dissipate the heat generated within the package. Otherwise it's not possible to operate the AS1312 at its usable maximal power. To dissipate as much heat as possible from the package into a copper plane with as much area as possible, it's recommended to use multiple vias in the printed circuit board. It's also recommended to solder the Exposed Pad (pin 9) to the GND plane.

Note: Continuing operation in thermal overload conditions may damage the device and is considered bad practice.

9.2 Component Selection

Only four components are required to complete the design of the step-up converter. The low peak currents of the AS1312 allow the use of low value, low profile inductors and tiny external ceramic capacitors.

9.3 Inductor Selection

For best efficiency, choose an inductor with high frequency core material, such as ferrite, to reduce core losses. The inductor should have low DCR (DC resistance) to reduce the I²R losses, and must be able to handle the peak inductor current without saturating. A 6.8µH inductor with a > 500mA current rating and < 500mΩ DCR is recommended.

Table 4. Recommended Inductors

Part Number	L	DCR	Current Rating	Dimensions (L/W/T)	Manufacturer
XPL2010-682M	6.8µH	421mΩ	0.62A	2.0x1.9x1.0mm	Coilcraft www.coilcraft.com
EPL2014-682M	6.8µH	287mΩ	0.59A	2.0x2.0x1.4mm	
LPS3015-682M	6.8µH	300mΩ	0.86A	3.0x3.0x1.5mm	
LPS3314-682M	6.8µH	240mΩ	0.9A	3.3x3.3x1.3mm	
LPS4018-682M	6.8µH	150mΩ	1.3A	3.9x3.9x1.7mm	
LQH32CN6R8M53L	6.8µH	250mΩ	0.54A	3.2x2.5x1.55mm	Murata www.murata.com
LQH3NPN6R8NJ0L	6.8µH	210mΩ	0.7A	3.0x3.0x1.1mm	
LQH44PN6R8MJ0L	6.8µH	143mΩ	0.72A	4.0x4.0x1.1mm	

9.4 Capacitor Selection

The convertor requires three capacitors. Ceramic X5R or X7R types will minimize ESL and ESR while maintaining capacitance at rated voltage over temperature. The VIN capacitor should be 22µF. The VOUT capacitor should be between 22µF and 47µF. A larger output capacitor should be used if lower peak to peak output voltage ripple is desired. A larger output capacitor will also improve load regulation on VOUT. See Table 5 for a list of capacitors for input and output capacitor selection.

Table 5. Recommended Input and Output Capacitors

Part Number	C	TC Code	Rated Voltage	Dimensions (L/W/T)	Manufacturer
GRM21BR60J226ME99	22µF	X5R	6.3V	0805, T=1.25mm	Murata www.murata.com
GRM31CR61C226KE15	22µF	X5R	16V	1206, T=1.6mm	
GRM31CR60J475KA01	47µF	X5R	6.3V	1206, T=1.6mm	

On the pin REF a 100nF capacitor with an Insulation resistance >1GΩ is recommended.

Table 6. Recommended Capacitors for REF

Part Number	C	TC Code	Insulation Resistance	Rated Voltage	Dimensions (L/W/T)	Manufacturer
GRM188R71C104KA01	100nF	X7R	>5GΩ	16V	0603, T=0.8mm	Murata www.murata.com

9.5 Layout Considerations

Relatively high peak currents of 400mA (typ) circulate during normal operation of the AS1312. Long printed circuit tracks can generate additional ripple and noise that mask correct operation and prove difficult to “de-bug” during production testing. Referring to Figure 1, the input loop formed by C1, VIN and GND pins should be minimized. Similarly, the output loop formed by C2, VOUT and GND should also be minimized. Ideally both loops should connect to GND in a “star” fashion. Finally, it is important to return CREF to the GND pin directly.

10 Package Drawings and Markings

The device is available in a 8-pin (2x2) TDFN and 8-pin WL-CSP package.

Figure 14. 8-pin (2x2) TDFNMarking

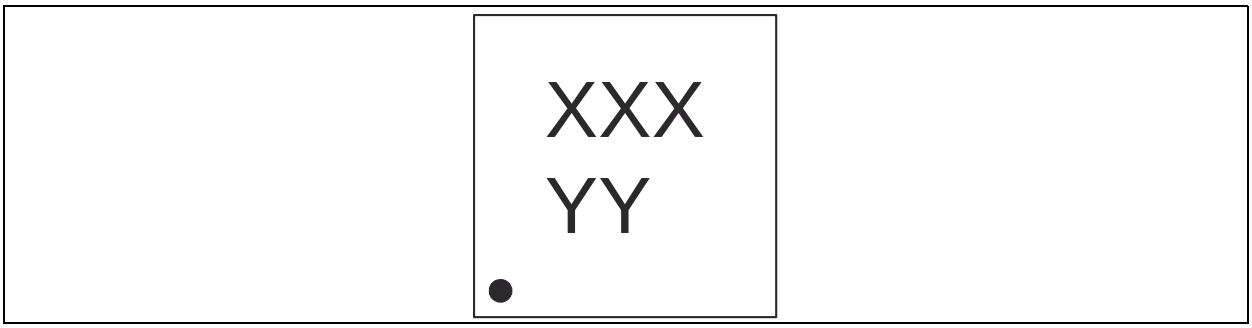


Figure 15. 8-pin WL-CSP Marking

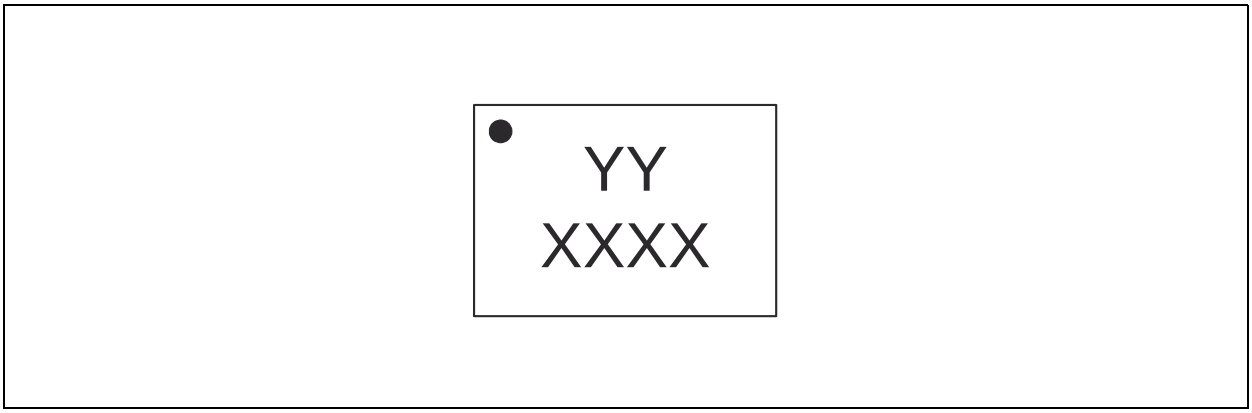
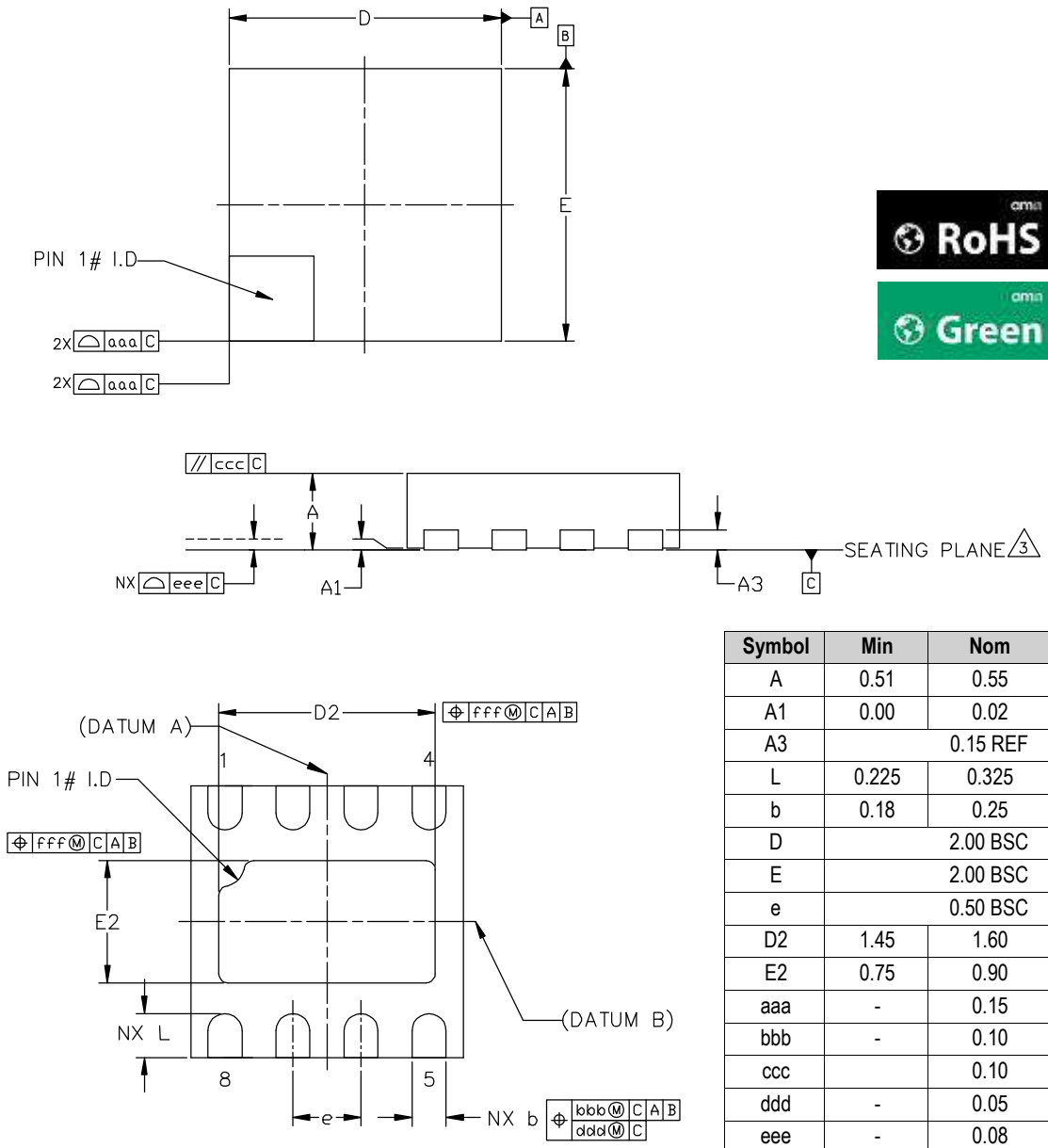


Table 7. Packaging Code

XXX	XXXX	YY
encoded datecode for TDFN	encoded datecode for WL-CSP	marketing code

Figure 16. 8-pin (2x2) TDFN Drawings and Dimensions

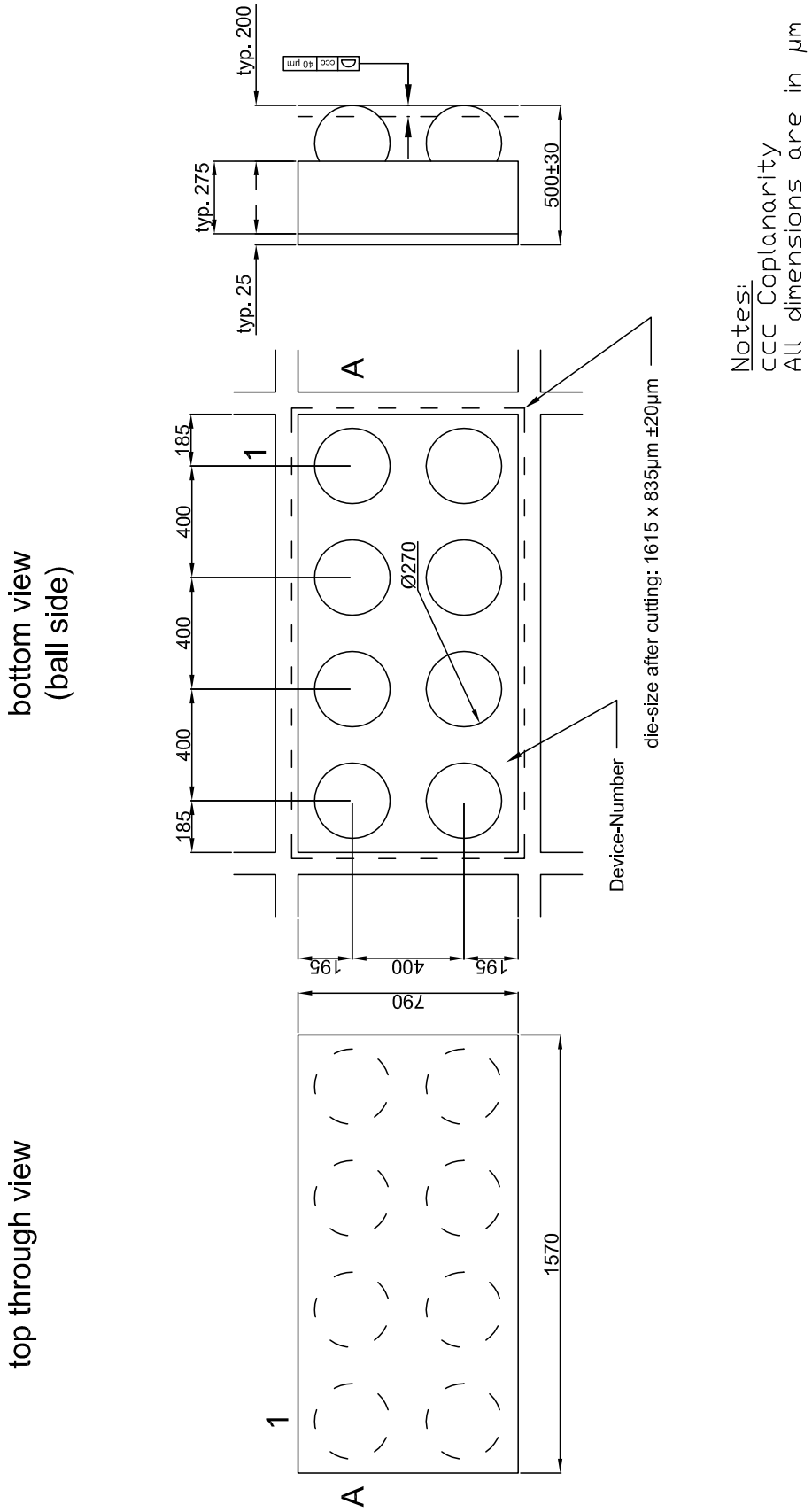


Symbol	Min	Nom	Max
A	0.51	0.55	0.60
A1	0.00	0.02	0.05
A3		0.15 REF	
L	0.225	0.325	0.425
b	0.18	0.25	0.30
D		2.00 BSC	
E		2.00 BSC	
e		0.50 BSC	
D2	1.45	1.60	1.70
E2	0.75	0.90	1.00
aaa	-	0.15	-
bbb	-	0.10	-
ccc		0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		8	

Notes:

1. Dimensioning & tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Figure 17. 8-pin WL-CSP Drawings and Dimensions



Revision History

Revision	Date	Owner	Description
1.0		afe	Initial revision
1.5	26 Mar, 2012		Updated Detailed Description and Application Information sections
1.6			
1.7	27 Apr, 2012		Detailed Description section updated
1.8	19 Jul, 2012		Added info on Thermal resistance, conditions for Output Voltage Tolerance. Updated ordering table.
1.9	10 Aug, 2012		Updated storage temp values for WL-CSP
1.10	17 Aug, 2012		Updated (EQ 17)
1.11	14 Sep, 2012		Updated conditions for 'Output Voltage Tolerance' parameter (see page 4)
1.12	14 Oct, 2013	tka	Update Green & ROHS logo, update ordering information

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The device is available as the standard products listed below.

Table 8. Ordering Information

Ordering Code	Marking	VOUT	Description	Delivery Form	Package
AS1312-BTDT-50	BE	5.0V	Ultra Low Quiescent Current, Hysteretic DC-DC Step-Up Converter	Tape and Reel	8-pin (2x2) TDFN
AS1312-BTDT-33	BX	3.3V		Tape and Reel	8-pin (2x2) TDFN
AS1312-BWLT-50	BF	5.0V		Tape and Reel	8-pin WL-CSP
AS1312-BWLT-45	BQ	4.5V		Tape and Reel	8-pin WL-CSP
AS1312 [1]	tbd	xx		Tape and Reel	tbd

1. Non-standard devices from 2.5V to 5.0V are available in 50mV steps.
For more information and inquiries contact http://www.ams.com/contact

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