

# 74AVC8T245-Q100

8-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 2 — 6 September 2013

Product data sheet

## 1. General description

The 74AVC8T245-Q100 is an 8-bit, dual supply transceiver that enables bidirectional level translation. It features two 8-bit input-output ports (An and Bn), a direction control input (DIR), an output enable input ( $\overline{\text{OE}}$ ) and dual supply pins ( $V_{\text{CC(A)}}$  and  $V_{\text{CC(B)}}$ ). Both  $V_{\text{CC(A)}}$  and  $V_{\text{CC(B)}}$  can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins An,  $\overline{\text{OE}}$  and DIR are referenced to  $V_{\text{CC(A)}}$  and pins Bn are referenced to  $V_{\text{CC(B)}}$ . A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input ( $\overline{\text{OE}}$ ) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using  $I_{\text{OFF}}$ . The  $I_{\text{OFF}}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{\text{CC(A)}}$  or  $V_{\text{CC(B)}}$  are at GND level, both An and Bn are in the high-impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range:
  - ◆  $V_{\text{CC(A)}}$ : 0.8 V to 3.6 V
  - ◆  $V_{\text{CC(B)}}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - ◆ MIL-STD-883, method 3015 class 3B exceeds 8000 V
  - ◆ HBM JESD22-A114E class 3B exceeds 8000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )
- Maximum data rates:
  - ◆ 380 Mbit/s ( $\geq 1.8\text{ V}$  to  $3.3\text{ V}$  translation)



- ◆ 260 Mbit/s ( $\geq 1.1\text{ V}$  to  $3.3\text{ V}$  translation)
- ◆ 260 Mbit/s ( $\geq 1.1\text{ V}$  to  $2.5\text{ V}$  translation)
- ◆ 210 Mbit/s ( $\geq 1.1\text{ V}$  to  $1.8\text{ V}$  translation)
- ◆ 150 Mbit/s ( $\geq 1.1\text{ V}$  to  $1.5\text{ V}$  translation)
- ◆ 100 Mbit/s ( $\geq 1.1\text{ V}$  to  $1.2\text{ V}$  translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC8T245PW-Q100	−40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74AVC8T245BQ-Q100	−40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

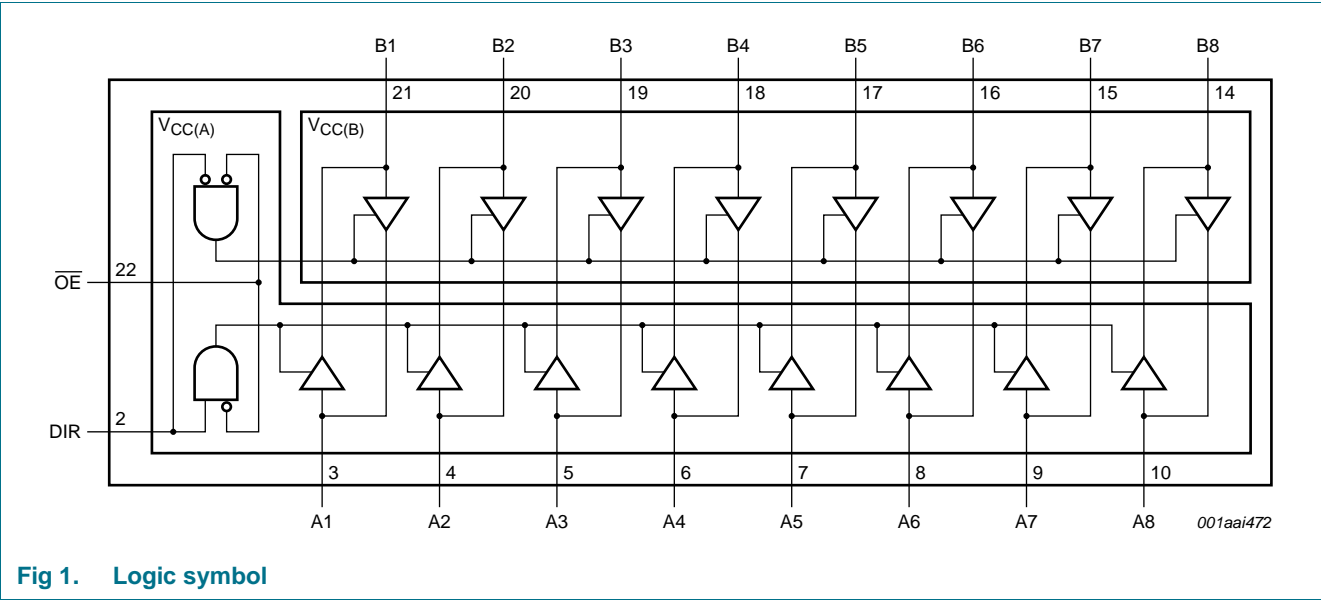


Fig 1. Logic symbol

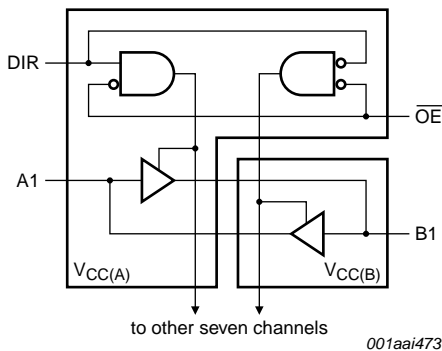


Fig 2. Logic diagram (one channel)

5. Pinning information

5.1 Pinning

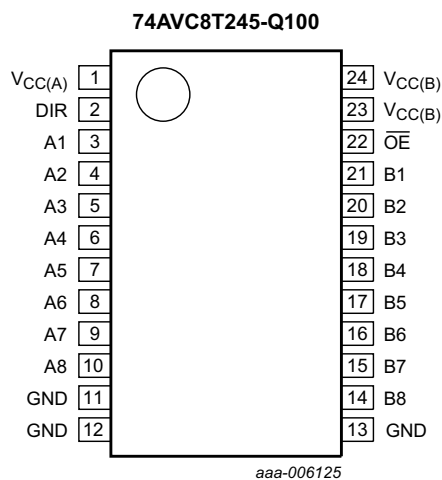
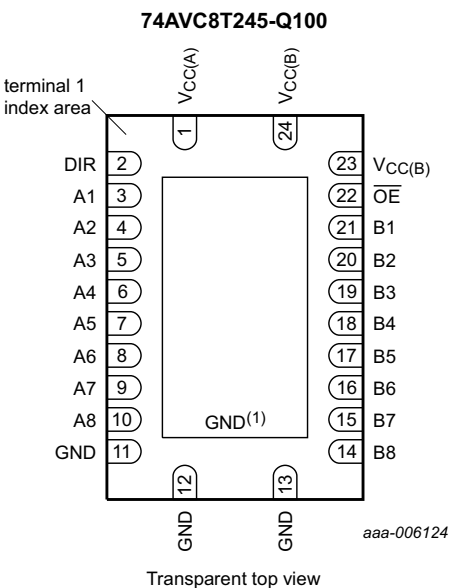


Fig 3. Pin configuration TSSOP24



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 4. Pin configuration DHVQFN24

## 5.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A (An, $\overline{OE}$ and DIR inputs are referenced to $V_{CC(A)}$ )
DIR	2	direction control
A1 to A8	3, 4, 5, 6, 7, 8, 9, 10	data input or output
GND <sup>[1]</sup>	11	ground (0 V)
GND <sup>[1]</sup>	12	ground (0 V)
GND <sup>[1]</sup>	13	ground (0 V)
B1 to B8	21, 20, 19, 18, 17, 16, 15, 14	data input or output
$\overline{OE}$	22	output enable input (active LOW)
$V_{CC(B)}$	23	supply voltage B (Bn inputs are referenced to $V_{CC(B)}$ )
$V_{CC(B)}$	24	supply voltage B (Bn inputs are referenced to $V_{CC(B)}$ )

[1] All GND pins must be connected to ground (0 V).

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

Supply voltage	Input		Input/output <sup>[3]</sup>	
$V_{CC(A)}$ , $V_{CC(B)}$	$\overline{OE}$ <sup>[2]</sup>	DIR <sup>[2]</sup>	An <sup>[2]</sup>	Bn
0.8 V to 3.6 V	L	L	An = Bn	input
0.8 V to 3.6 V	L	H	input	Bn = An
0.8 V to 3.6 V	H	X	Z	Z
GND <sup>[3]</sup>	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The An, DIR and  $\overline{OE}$  input circuit is referenced to  $V_{CC(A)}$ ; the Bn input circuit is referenced to  $V_{CC(B)}$ .

[3] If at least one of  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into suspend mode.

## 7. Limiting values

**Table 4.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		<sup>[1]</sup> -0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode	<sup>[1][2][3]</sup> -0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	<sup>[1]</sup> -0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin	-	100	mA

**Table 4.** Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{\text{GND}}$	ground current	per GND pin	-100	-	mA
$T_{\text{stg}}$	storage temperature		-65	+150	°C
$P_{\text{tot}}$	total power dissipation	$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$	[4] -	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{\text{CCO}}$  is the supply voltage associated with the output port.[3]  $V_{\text{CCO}} + 0.5\text{ V}$  should not exceed 4.6 V.[4] For TSSOP24 package:  $P_{\text{tot}}$  derates linearly at 5.5 mW/K above 60 °C.  
For DHVQFN24 package:  $P_{\text{tot}}$  derates linearly at 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5.** Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{\text{CC(A)}}$	supply voltage A		0.8	3.6	V
$V_{\text{CC(B)}}$	supply voltage B		0.8	3.6	V
$V_{\text{I}}$	input voltage		0	3.6	V
$V_{\text{O}}$	output voltage	Active mode	[1] 0	$V_{\text{CCO}}$	V
		Suspend or 3-state mode	0	3.6	V
$T_{\text{amb}}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{\text{CCI}} = 0.8\text{ V to }3.6\text{ V}$	[2] -	5	ns/V

[1]  $V_{\text{CCO}}$  is the supply voltage associated with the output port.[2]  $V_{\text{CCI}}$  is the supply voltage associated with the input port.

## 9. Static characteristics

**Table 6.** Typical static characteristics at  $T_{\text{amb}} = 25\text{ °C}$  [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{OH}}$	HIGH-level output voltage	$V_{\text{I}} = V_{\text{IH}}$ or $V_{\text{IL}}$ $I_{\text{O}} = -1.5\text{ mA}$ ; $V_{\text{CC(A)}} = V_{\text{CC(B)}} = 0.8\text{ V}$	-	0.69	-	V
$V_{\text{OL}}$	LOW-level output voltage	$V_{\text{I}} = V_{\text{IH}}$ or $V_{\text{IL}}$ $I_{\text{O}} = 1.5\text{ mA}$ ; $V_{\text{CC(A)}} = V_{\text{CC(B)}} = 0.8\text{ V}$	-	0.07	-	V
$I_{\text{I}}$	input leakage current	DIR, $\overline{\text{OE}}$ input; $V_{\text{I}} = 0\text{ V or }3.6\text{ V}$ ; $V_{\text{CC(A)}} = V_{\text{CC(B)}} = 0.8\text{ V to }3.6\text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
$I_{\text{OZ}}$	OFF-state output current	A or B port; $V_{\text{O}} = 0\text{ V or }V_{\text{CCO}}$ ; $V_{\text{CC(A)}} = V_{\text{CC(B)}} = 3.6\text{ V}$	[3] -	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode A port; $V_{\text{O}} = 0\text{ V or }V_{\text{CCO}}$ ; $V_{\text{CC(A)}} = 3.6\text{ V}$ ; $V_{\text{CC(B)}} = 0\text{ V}$	[3] -	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode B port; $V_{\text{O}} = 0\text{ V or }V_{\text{CCO}}$ ; $V_{\text{CC(A)}} = 0\text{ V}$ ; $V_{\text{CC(B)}} = 3.6\text{ V}$	[3] -	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$

**Table 6.** Typical static characteristics at  $T_{amb} = 25\text{ }^{\circ}\text{C}$  [1][2] ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V}$ to $3.6\text{ V}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V}$ to $3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	DIR, $\overline{OE}$ input; $V_I = 0\text{ V}$ or $3.3\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	1.5	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V}$ or $0\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	4.3	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output port.[2]  $V_{CCI}$  is the supply voltage associated with the data input port.[3] For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.**Table 7.** Static characteristics [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	$0.70V_{CCI}$	-	$0.70V_{CCI}$	-	V
		$V_{CCI} = 1.1\text{ V}$ to $1.95\text{ V}$	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		$V_{CCI} = 2.3\text{ V}$ to $2.7\text{ V}$	1.6	-	1.6	-	V
		$V_{CCI} = 3.0\text{ V}$ to $3.6\text{ V}$	2	-	2	-	V
		DIR, $\overline{OE}$ input					
		$V_{CC(A)} = 0.8\text{ V}$	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)} = 1.1\text{ V}$ to $1.95\text{ V}$	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)} = 2.3\text{ V}$ to $2.7\text{ V}$	1.6	-	1.6	-	V
		$V_{CC(A)} = 3.0\text{ V}$ to $3.6\text{ V}$	2	-	2	-	V
$V_{IL}$	LOW-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	-	$0.30V_{CCI}$	-	$0.30V_{CCI}$	V
		$V_{CCI} = 1.1\text{ V}$ to $1.95\text{ V}$	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		$V_{CCI} = 2.3\text{ V}$ to $2.7\text{ V}$	-	0.7	-	0.7	V
		$V_{CCI} = 3.0\text{ V}$ to $3.6\text{ V}$	-	0.8	-	0.8	V
		DIR, $\overline{OE}$ input					
		$V_{CC(A)} = 0.8\text{ V}$	-	$0.30V_{CC(A)}$	-	$0.30V_{CC(A)}$	V
		$V_{CC(A)} = 1.1\text{ V}$ to $1.95\text{ V}$	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)} = 2.3\text{ V}$ to $2.7\text{ V}$	-	0.7	-	0.7	V
		$V_{CC(A)} = 3.0\text{ V}$ to $3.6\text{ V}$	-	0.8	-	0.8	V

**Table 7. Static characteristics ...continued** [\[1\]\[2\]](#)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -100 µA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 µA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	DIR, $\overline{\text{OE}}$ input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±1	-	±5	µA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V <a href="#">[3]</a>	-	±5	-	±30	µA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V <a href="#">[3]</a>	-	±5	-	±30	µA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V <a href="#">[3]</a>	-	±5	-	±30	µA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	µA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	µA

**Table 7.** Static characteristics ...continued<sup>[1][2]</sup>

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-2	-	-12	-	μA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	10	-	55	μA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	8	-	50	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-2	-	-12	-	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	8	-	50	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	20	-	70	μA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	16	-	65	μA

[1] V<sub>CCO</sub> is the supply voltage associated with the output port.[2] V<sub>CCI</sub> is the supply voltage associated with the data input port.[3] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.**Table 8.** Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

## 10. Dynamic characteristics

**Table 9.** Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$ <sup>[1]</sup>

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	An to Bn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		Bn to An	14.4	12.4	12.1	11.9	11.8	11.8	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	16.2	16.2	16.2	16.2	16.2	16.2	ns
		$\overline{OE}$ to Bn	17.6	10.0	9.0	9.1	8.7	9.3	ns
$t_{en}$	enable time	$\overline{OE}$ to An	21.9	21.9	21.9	21.9	21.9	21.9	ns
		$\overline{OE}$ to Bn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

**Table 10.** Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$ <sup>[1]</sup>

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	An to Bn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		Bn to An	14.4	7.0	6.2	6.0	5.9	6.0	ns
$t_{dis}$	disable time	$\overline{OE}$ to An	16.2	5.9	4.4	4.2	3.1	3.5	ns
		$\overline{OE}$ to Bn	17.6	14.2	13.7	13.6	13.3	13.1	ns
$t_{en}$	enable time	$\overline{OE}$ to An	21.9	6.4	4.4	3.5	2.6	2.3	ns
		$\overline{OE}$ to Bn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

**Table 11. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$  [1][2]**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction An to Bn); output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction An to Bn); output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction Bn to An); output enabled	9	9	10	10	11	13	pF
		A port: (direction Bn to An); output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction An to Bn); output enabled	9	9	10	10	11	13	pF
		B port: (direction An to Bn); output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction Bn to An); output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		B port: (direction Bn to An); output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = load capacitance in pF; $V_{CC}$  = supply voltage in V; $N$  = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.[2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\text{ }\Omega$ .

**Table 12. Dynamic characteristics for temperature range –40 °C to +85 °C<sup>[1]</sup>**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>CC(A)</sub> = 1.1 V to 1.3 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	9.0	0.5	6.7	0.5	5.8	0.5	4.9	0.5	4.8	ns
		Bn to An	0.5	9.0	0.5	8.5	0.5	8.3	0.5	8.0	0.5	7.8	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	ns
		$\overline{\text{OE}}$ to Bn	0.5	12.3	0.5	9.5	0.5	9.4	0.5	8.0	0.5	8.9	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	ns
		$\overline{\text{OE}}$ to Bn	1.1	14.2	1.1	10.4	1.1	9.0	1.0	7.7	1.0	7.3	ns
V <sub>CC(A)</sub> = 1.4 V to 1.6 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	8.5	0.5	5.6	0.5	4.7	0.5	4.4	0.5	4.1	ns
		Bn to An	0.5	6.7	0.5	5.6	0.5	5.3	0.5	5.2	0.5	5.0	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	ns
		$\overline{\text{OE}}$ to Bn	0.5	11.2	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	ns
		$\overline{\text{OE}}$ to Bn	1.1	12.8	1.1	8.1	1.1	7.1	1.0	5.6	1.0	5.2	ns
V <sub>CC(A)</sub> = 1.65 V to 1.95 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	8.3	0.5	5.3	0.5	4.5	0.5	3.8	0.5	3.5	ns
		Bn to An	0.5	5.8	0.5	4.7	0.5	4.5	0.5	4.3	0.5	4.1	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	ns
		$\overline{\text{OE}}$ to Bn	0.5	10.9	0.5	7.8	0.5	6.9	0.5	6.0	0.5	5.8	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		$\overline{\text{OE}}$ to Bn	1.1	12.4	1.1	8.2	1.0	6.7	0.5	5.1	0.5	4.5	ns
V <sub>CC(A)</sub> = 2.3 V to 2.7 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	8.0	0.5	5.2	0.5	4.3	0.5	3.3	0.5	2.9	ns
		Bn to An	0.5	4.9	0.5	4.4	0.5	3.8	0.5	3.3	0.5	3.1	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	ns
		$\overline{\text{OE}}$ to Bn	0.5	10.4	0.5	7.1	0.5	6.3	0.5	5.1	0.5	5.2	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	ns
		$\overline{\text{OE}}$ to Bn	1.1	11.9	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4.0	ns
V <sub>CC(A)</sub> = 3.0 V to 3.6 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	7.8	0.5	5.0	0.5	4.1	0.5	3.1	0.5	2.7	ns
		Bn to An	0.5	4.8	0.5	4.1	0.5	3.5	0.5	2.9	0.5	2.7	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	ns
		$\overline{\text{OE}}$ to Bn	0.5	10.1	0.5	6.9	0.5	6.0	0.5	4.8	0.5	5.0	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{\text{OE}}$ to Bn	1.1	11.7	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

**Table 13. Dynamic characteristics for temperature range –40 °C to +125 °C<sup>[1]</sup>**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>CC(A)</sub> = 1.1 V to 1.3 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	9.9	0.5	7.4	0.5	6.4	0.5	5.4	0.5	5.3	ns
		Bn to An	0.5	9.9	0.5	9.4	0.5	9.2	0.5	8.8	0.5	8.6	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	ns
		$\overline{\text{OE}}$ to Bn	0.5	13.6	0.5	10.5	0.5	10.4	0.5	8.8	0.5	9.8	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	ns
		$\overline{\text{OE}}$ to Bn	1.1	15.7	1.1	11.5	1.1	9.9	1.0	8.5	1.0	8.1	ns
V <sub>CC(A)</sub> = 1.4 V to 1.6 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	9.4	0.5	6.2	0.5	5.2	0.5	4.9	0.5	4.6	ns
		Bn to An	0.5	7.4	0.5	6.2	0.5	5.9	0.5	5.8	0.5	5.5	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	ns
		$\overline{\text{OE}}$ to Bn	0.5	12.4	0.5	9.3	0.5	8.4	0.5	8.0	0.5	8.6	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	ns
		$\overline{\text{OE}}$ to Bn	1.1	14.1	1.1	9.0	1.1	7.9	1.0	6.2	1.0	5.8	ns
V <sub>CC(A)</sub> = 1.65 V to 1.95 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	9.2	0.5	5.9	0.5	5.0	0.5	4.2	0.5	3.9	ns
		Bn to An	0.5	6.4	0.5	5.2	0.5	5.0	0.5	4.8	0.5	4.6	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	ns
		$\overline{\text{OE}}$ to Bn	0.5	12.0	0.5	8.6	0.5	7.6	0.5	6.6	0.5	6.4	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{\text{OE}}$ to Bn	1.1	13.7	1.1	9.1	1.0	7.4	0.5	5.7	0.5	5.0	ns
V <sub>CC(A)</sub> = 2.3 V to 2.7 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	8.8	0.5	5.8	0.5	4.8	0.5	3.7	0.5	3.2	ns
		Bn to An	0.5	5.4	0.5	4.9	0.5	4.2	0.5	3.7	0.5	3.5	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{\text{OE}}$ to Bn	0.5	11.5	0.5	7.9	0.5	7.0	0.5	5.7	0.5	5.8	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		$\overline{\text{OE}}$ to Bn	1.1	13.1	1.1	8.7	0.5	7.1	0.5	5.1	0.5	4.4	ns
V <sub>CC(A)</sub> = 3.0 V to 3.6 V													
t <sub>pd</sub>	propagation delay	An to Bn	0.5	8.6	0.5	5.5	0.5	4.6	0.5	3.5	0.5	3.0	ns
		Bn to An	0.5	5.3	0.5	4.6	0.5	3.9	0.5	3.2	0.5	3.0	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to An	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	ns
		$\overline{\text{OE}}$ to Bn	0.5	11.2	0.5	7.6	0.5	6.6	0.5	5.3	0.5	5.5	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to An	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	ns
		$\overline{\text{OE}}$ to Bn	1.1	12.9	1.1	8.6	0.5	6.9	0.5	5.0	0.5	4.3	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

11. Waveforms and test circuit

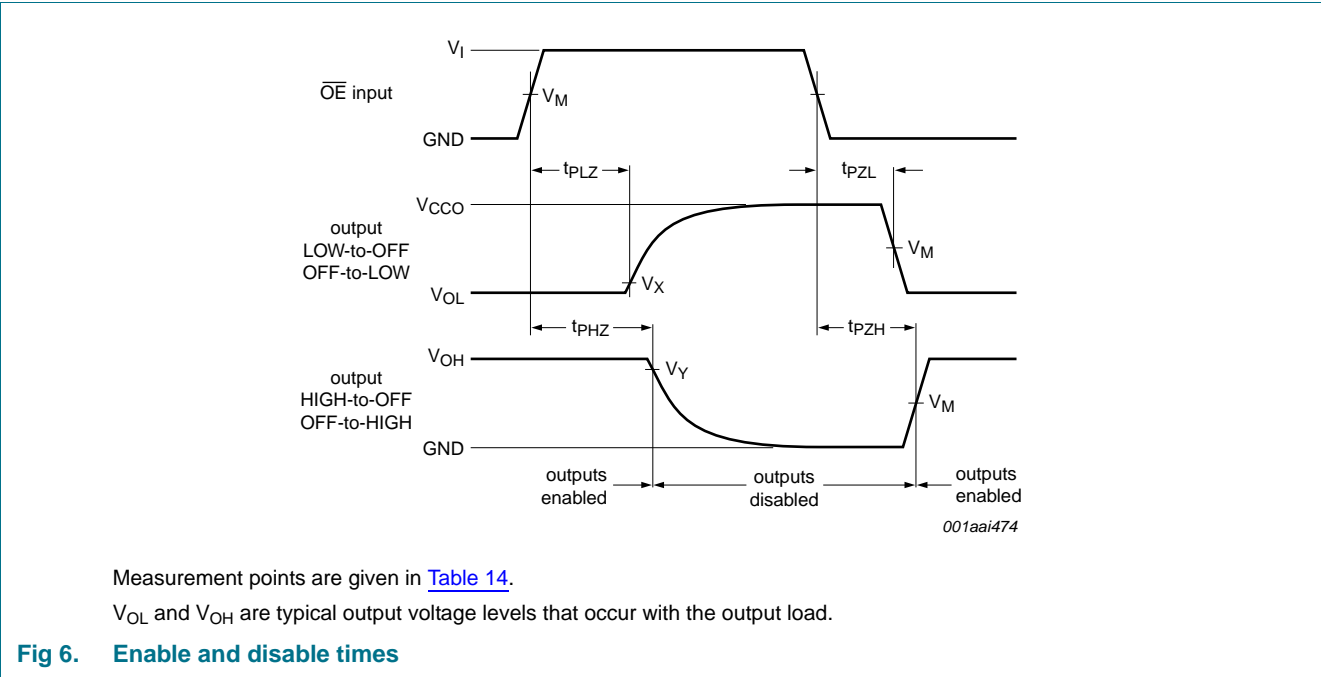
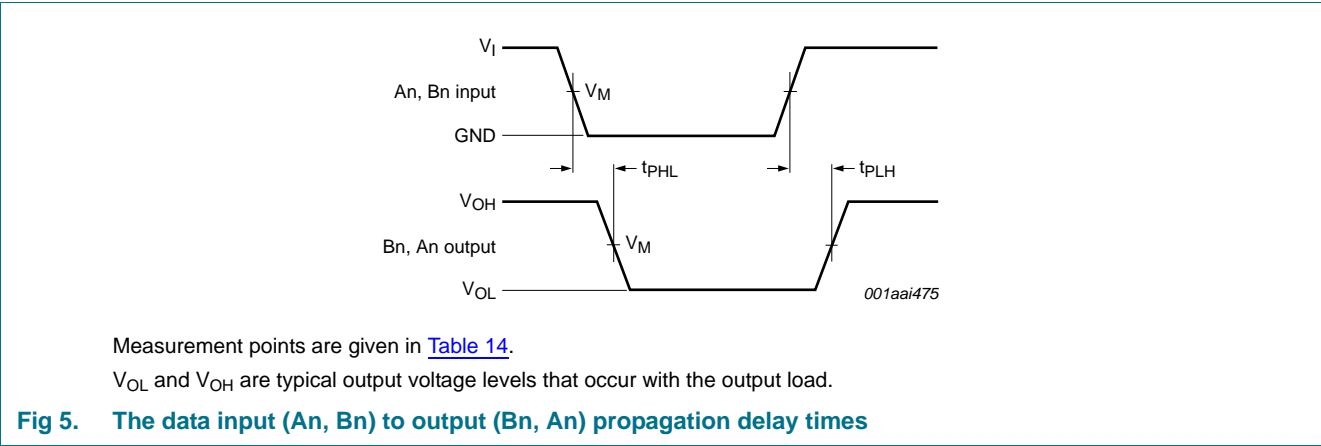
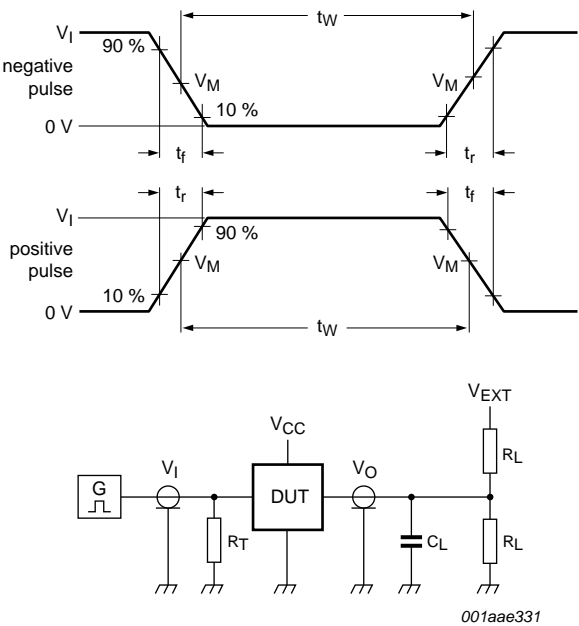


Table 14. Measurement points

Supply voltage	Input <sup>[1]</sup>	Output <sup>[2]</sup>		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.



Test data is given in [Table 15](#).  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance.  
 $V_{EXT}$  = External voltage for measuring switching times.

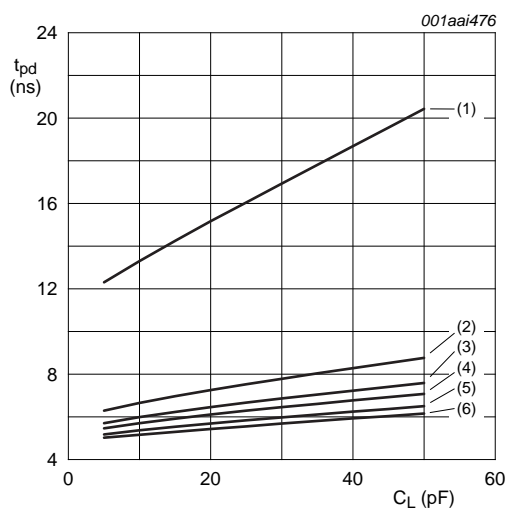
Fig 7. Test circuit for measuring switching times

Table 15. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}, V_{CC(B)}$	$V_I$ <sup>[1]</sup>	$\Delta t/\Delta V$ <sup>[2]</sup>	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ <sup>[3]</sup>
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0$ ns/V	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

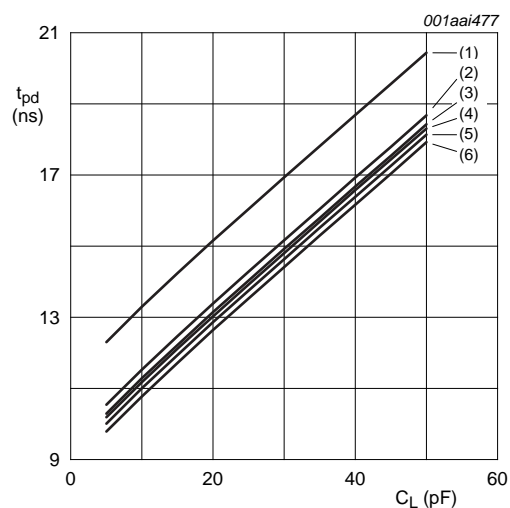
[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
[2]  $dV/dt \geq 1.0$  V/ns  
[3]  $V_{CCO}$  is the supply voltage associated with the output port.

## 12. Typical propagation delay characteristics



a. Propagation delay (An to Bn);  $V_{CC(A)} = 0.8 \text{ V}$

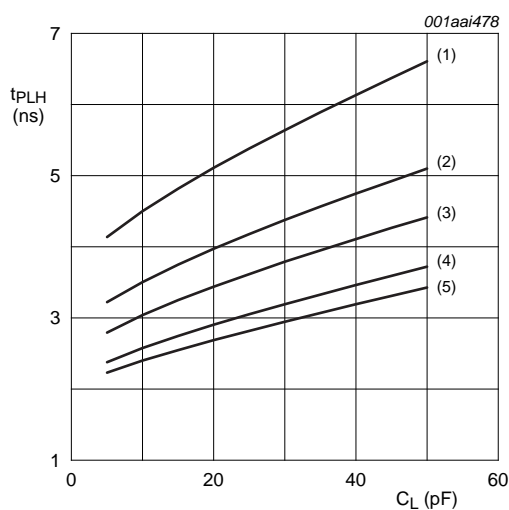
- (1)  $V_{CC(B)} = 0.8 \text{ V}$ .
- (2)  $V_{CC(B)} = 1.2 \text{ V}$ .
- (3)  $V_{CC(B)} = 1.5 \text{ V}$ .
- (4)  $V_{CC(B)} = 1.8 \text{ V}$ .
- (5)  $V_{CC(B)} = 2.5 \text{ V}$ .
- (6)  $V_{CC(B)} = 3.3 \text{ V}$ .



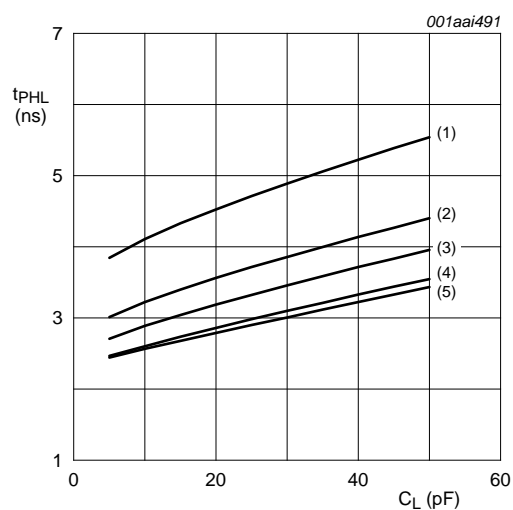
b. Propagation delay (An to Bn);  $V_{CC(B)} = 0.8 \text{ V}$

- (1)  $V_{CC(A)} = 0.8 \text{ V}$ .
- (2)  $V_{CC(A)} = 1.2 \text{ V}$ .
- (3)  $V_{CC(A)} = 1.5 \text{ V}$ .
- (4)  $V_{CC(A)} = 1.8 \text{ V}$ .
- (5)  $V_{CC(A)} = 2.5 \text{ V}$ .
- (6)  $V_{CC(A)} = 3.3 \text{ V}$ .

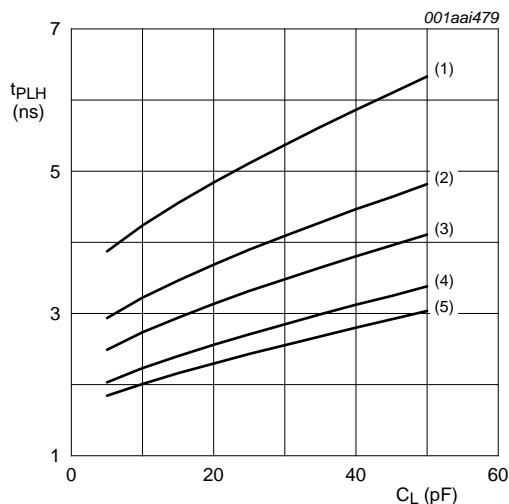
**Fig 8. Typical propagation delay versus load capacitance;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$**



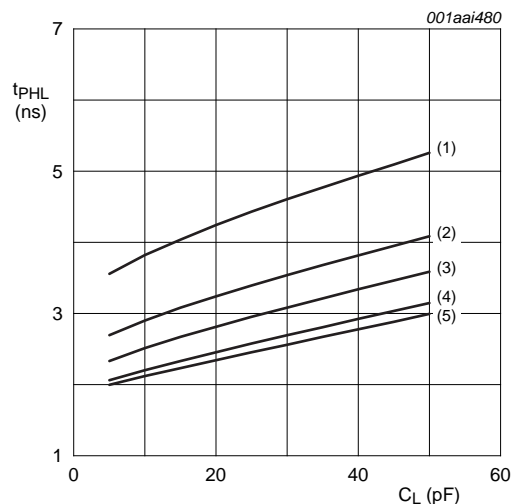
a. LOW to HIGH propagation delay (An to Bn);  
 $V_{CC(A)} = 1.2$  V



b. HIGH to LOW propagation delay (An to Bn);  
 $V_{CC(A)} = 1.2$  V



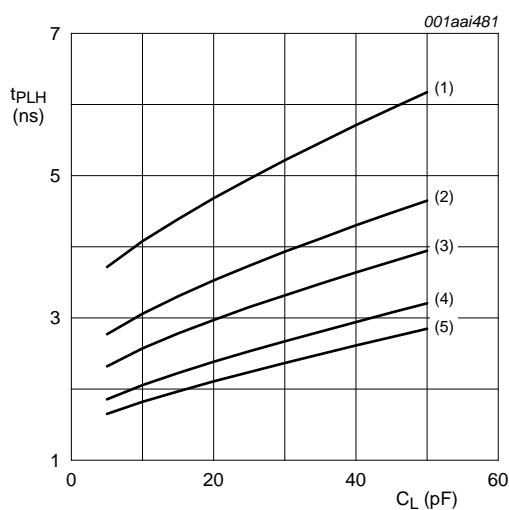
c. LOW to HIGH propagation delay (An to Bn);  
 $V_{CC(A)} = 1.5$  V



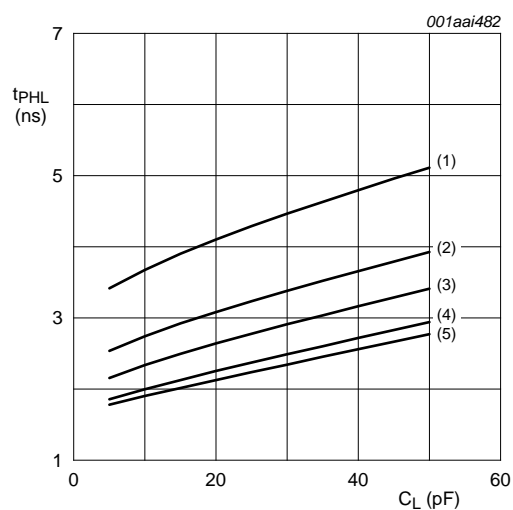
d. HIGH to LOW propagation delay (An to Bn);  
 $V_{CC(A)} = 1.5$  V

- (1)  $V_{CC(B)} = 1.2$  V.
- (2)  $V_{CC(B)} = 1.5$  V.
- (3)  $V_{CC(B)} = 1.8$  V.
- (4)  $V_{CC(B)} = 2.5$  V.
- (5)  $V_{CC(B)} = 3.3$  V.

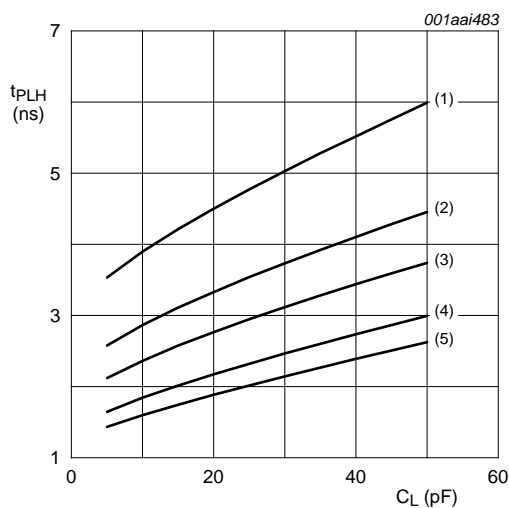
**Fig 9. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C**



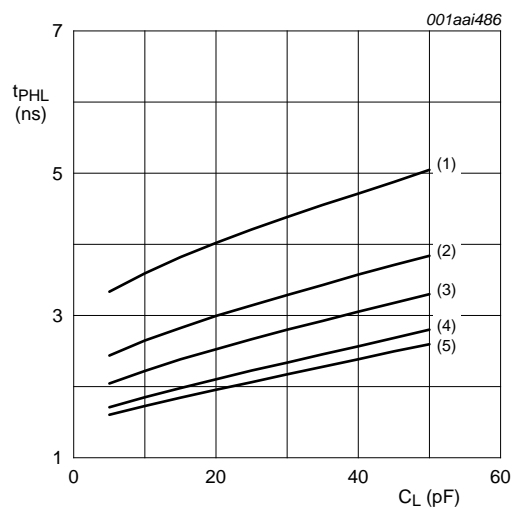
a. LOW to HIGH propagation delay (An to Bn);  
 $V_{CC(A)} = 1.8 \text{ V}$



b. HIGH to LOW propagation delay (An to Bn);  
 $V_{CC(A)} = 1.8 \text{ V}$



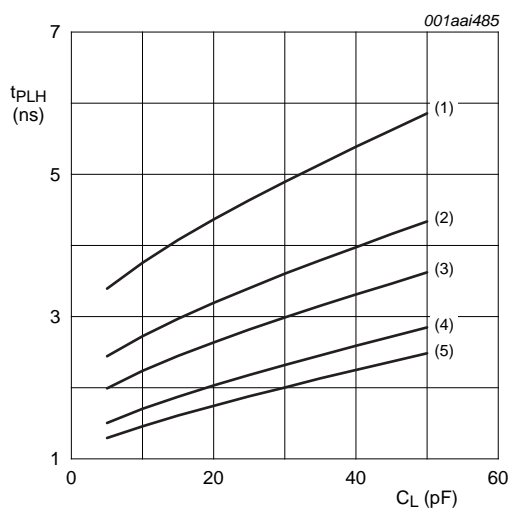
c. LOW to HIGH propagation delay (An to Bn);  
 $V_{CC(A)} = 2.5 \text{ V}$



d. HIGH to LOW propagation delay (An to Bn);  
 $V_{CC(A)} = 2.5 \text{ V}$

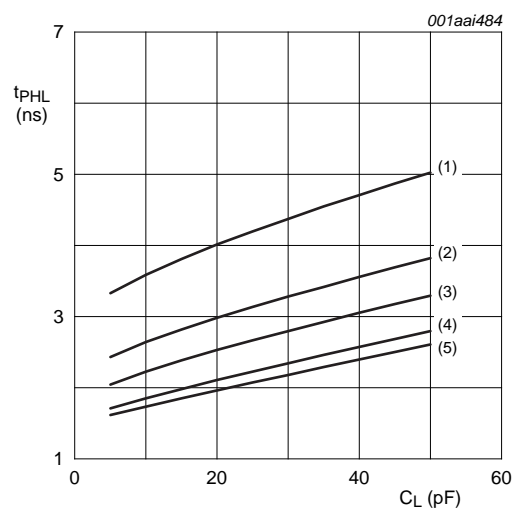
- (1)  $V_{CC(B)} = 1.2 \text{ V}$ .
- (2)  $V_{CC(B)} = 1.5 \text{ V}$ .
- (3)  $V_{CC(B)} = 1.8 \text{ V}$ .
- (4)  $V_{CC(B)} = 2.5 \text{ V}$ .
- (5)  $V_{CC(B)} = 3.3 \text{ V}$ .

**Fig 10. Typical propagation delay versus load capacitance;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$**



a. LOW to HIGH propagation delay (An to Bn);  
 $V_{CC(A)} = 3.3$  V

- (1)  $V_{CC(B)} = 1.2$  V.
- (2)  $V_{CC(B)} = 1.5$  V.
- (3)  $V_{CC(B)} = 1.8$  V.
- (4)  $V_{CC(B)} = 2.5$  V.
- (5)  $V_{CC(B)} = 3.3$  V.



b. HIGH to LOW propagation delay (An to Bn);  
 $V_{CC(A)} = 3.3$  V

**Fig 11. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C**

13. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1

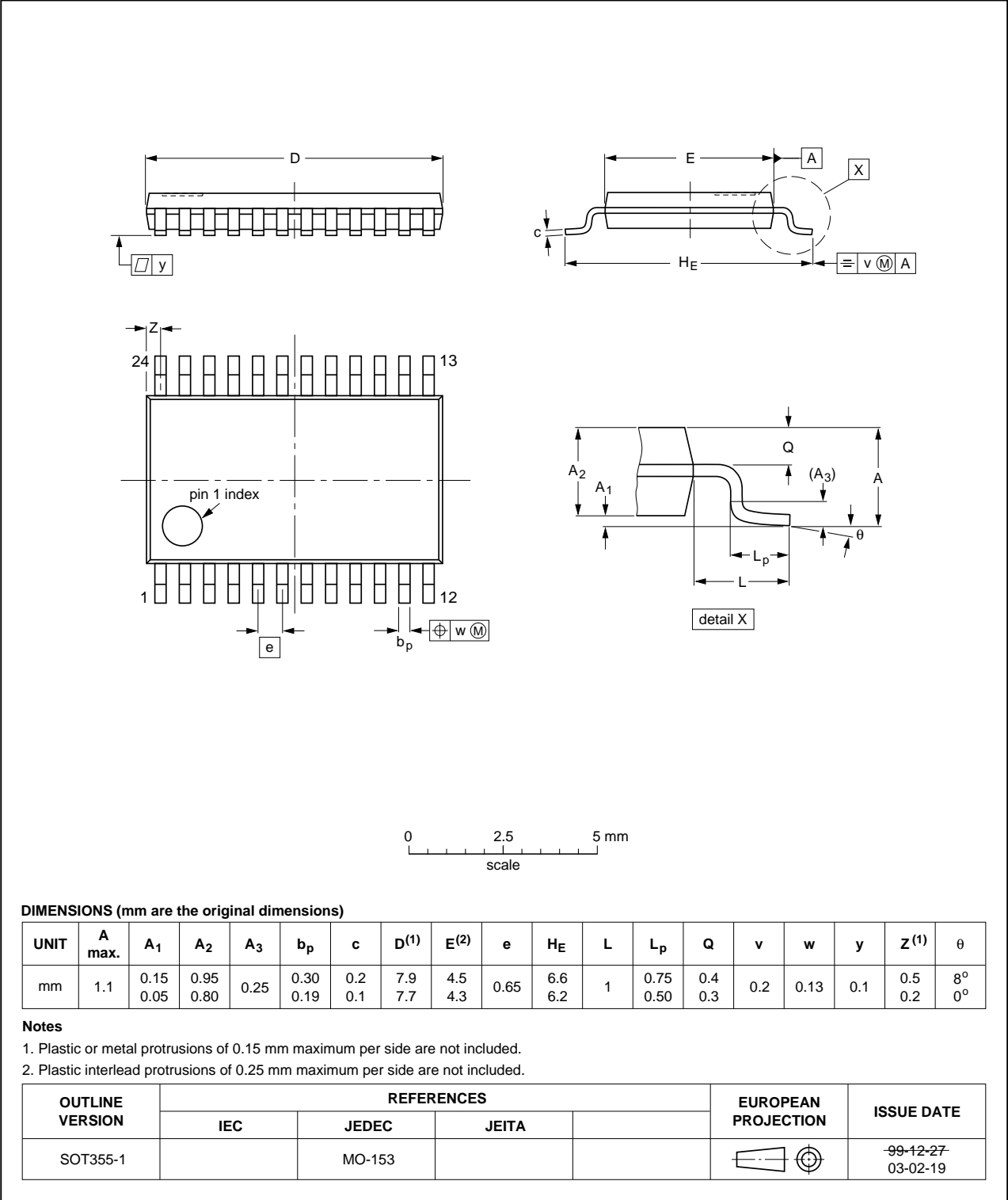


Fig 12. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;  
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

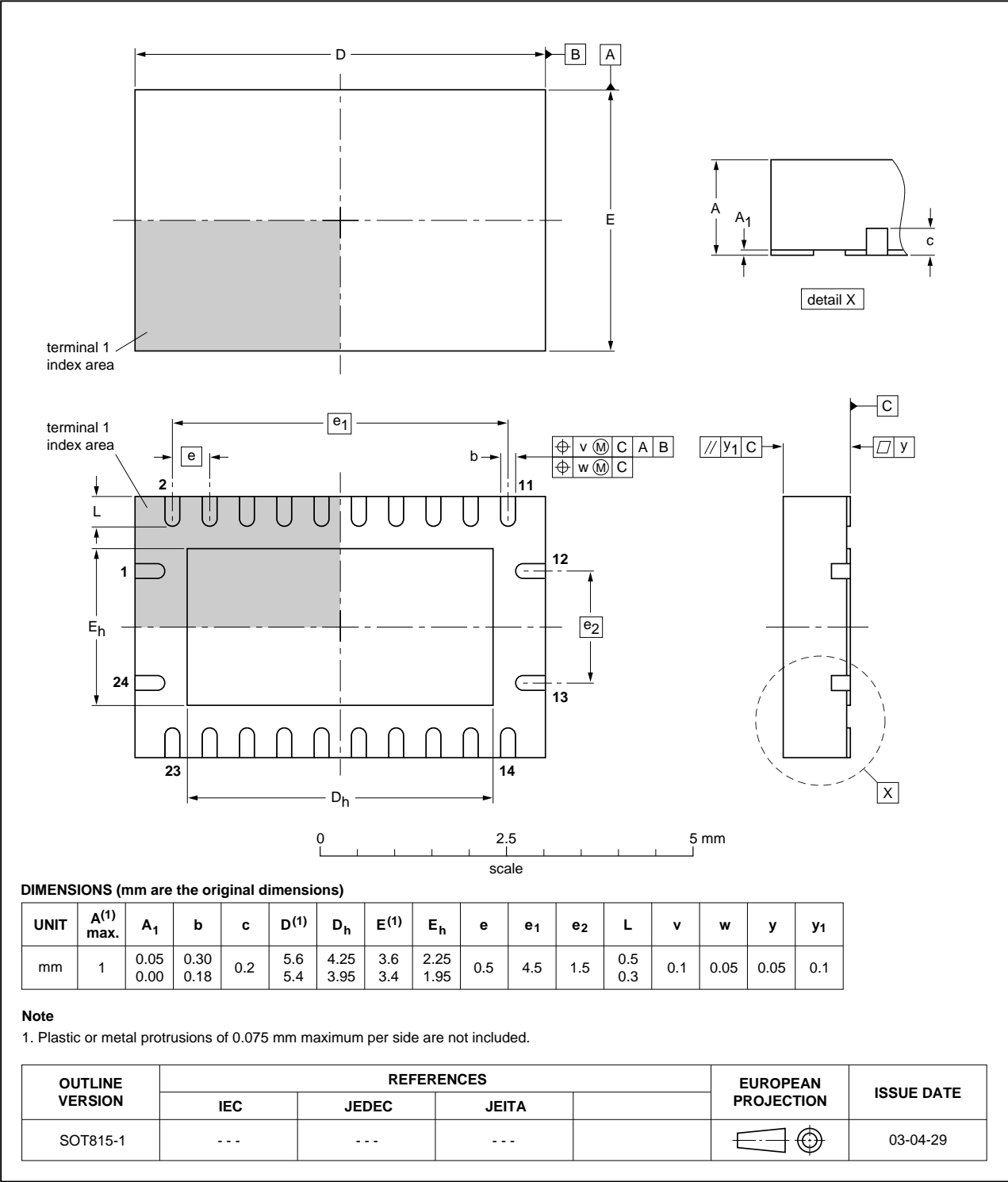


Fig 13. Package outline SOT815-1 (DHVQFN24)

## 14. Abbreviations

Table 16. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military

## 15. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC8T245_Q100 v.2	20130906	Product data sheet	-	74AVC8T245_Q100 v.1
Modifications:	• Legal pages updated (errata).			
74AVC8T245_Q100 v.1	20130226	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 18. Contents

---

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>
5.1	Pinning .....	3
5.2	Pin description .....	4
<b>6</b>	<b>Functional description</b> .....	<b>4</b>
<b>7</b>	<b>Limiting values</b> .....	<b>4</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>9</b>
<b>11</b>	<b>Waveforms and test circuit</b> .....	<b>13</b>
<b>12</b>	<b>Typical propagation delay characteristics</b> ..	<b>15</b>
<b>13</b>	<b>Package outline</b> .....	<b>19</b>
<b>14</b>	<b>Abbreviations</b> .....	<b>21</b>
<b>15</b>	<b>Revision history</b> .....	<b>21</b>
<b>16</b>	<b>Legal information</b> .....	<b>22</b>
16.1	Data sheet status .....	22
16.2	Definitions .....	22
16.3	Disclaimers .....	22
16.4	Trademarks .....	23
<b>17</b>	<b>Contact information</b> .....	<b>23</b>
<b>18</b>	<b>Contents</b> .....	<b>24</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 6 September 2013

Document identifier: 74AVC8T245\_Q100