

# 74HC107-Q100; 74HCT107-Q100

Dual JK flip-flop with reset; negative-edge trigger

Rev. 1 — 18 November 2013

Product data sheet

## 1. General description

The 74HC107-Q100; 74HCT107-Q100 is a dual negative edge triggered JK flip-flop featuring individual J and K inputs, clock ( $\overline{CP}$ ) and reset ( $\overline{R}$ ) inputs and complementary Q and  $\overline{Q}$  outputs. The reset is an asynchronous active LOW input and operates independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Input levels:
  - ◆ For 74HC107-Q100: CMOS level
  - ◆ For 74HCT107-Q100: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )
- Multiple package options

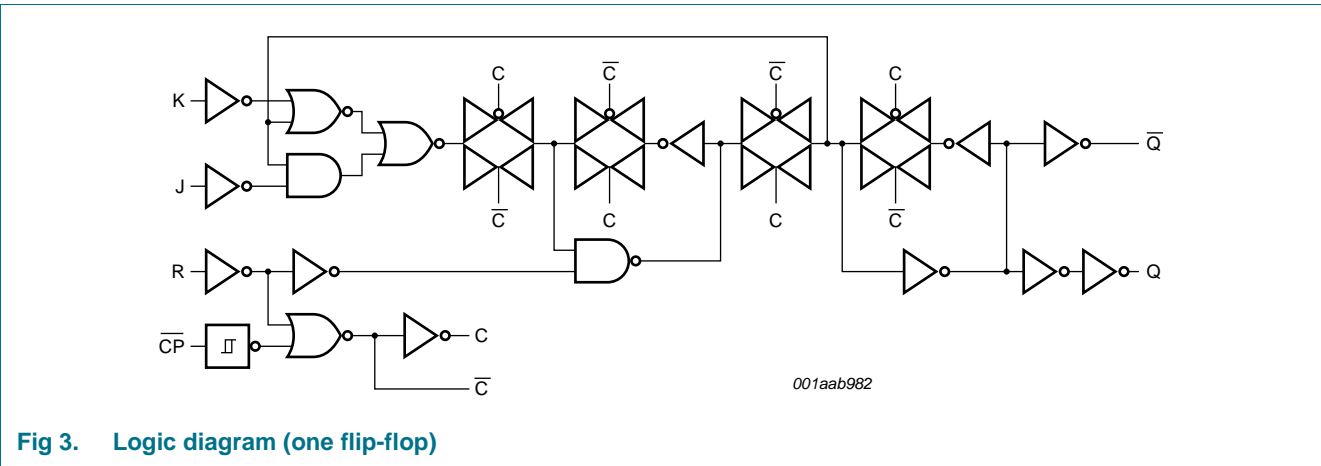
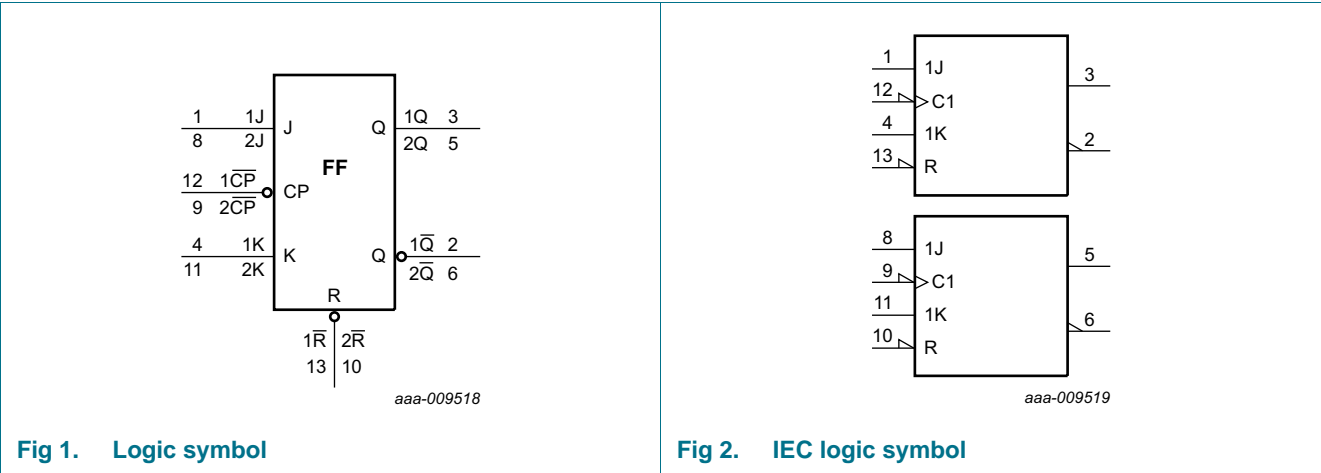
## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC107D-Q100 74HCT107D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC107PW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1



4. Functional diagram



5. Pinning information

5.1 Pinning

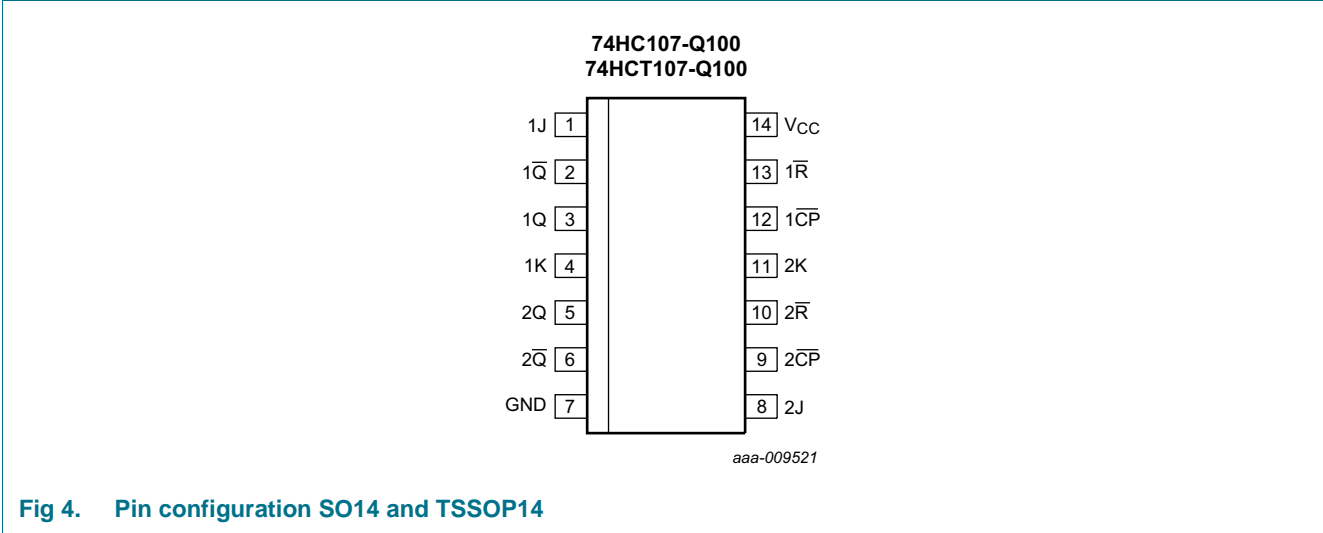


Fig 4. Pin configuration SO14 and TSSOP14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1J, 2J	1, 8	synchronous J input
1Q̄, 2Q̄	2, 6	complement output
1Q, 2Q	3, 5	true output
1K, 2K	4, 11	synchronous K input
1CP̄, 2CP̄	12, 9	clock input (HIGH-to-LOW edge-triggered)
1R̄, 2R̄	13, 10	asynchronous reset input (active LOW)
GND	7	ground (0 V)
VCC	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input				Output		Operating mode
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	$\overline{q}$	q	toggle
H	↓	l	h	L	H	load 0 (reset)
H	↓	h	l	H	L	load 1 (set)
H	↓	l	l	q	$\overline{q}$	hold (no change)

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;  
 q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition;  
 X = don't care;  
 ↓ = HIGH-to-LOW clock transition.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	<sup>[1]</sup> -	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	<sup>[1]</sup> -	±20	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		SO14 package	<sup>[2]</sup> -	500	mW
		TSSOP14 package	<sup>[3]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 [3]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC107-Q100			74HCT107-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC107-Q100										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	4.0	-	40	-	80	μA

**Table 6.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	3.5	-					pF
<b>74HCT107-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = –4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0 A; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		pin nCP, nJ	-	100	360	-	450	-	490	µA
		pin nR	-	65	234	-	293	-	319	µA
		pin nK	-	60	216	-	270	-	294	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 7](#)

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC107-Q100										
t <sub>pd</sub>	propagation delay	nCP to nQ; see <a href="#">Figure 5</a> <a href="#">[1]</a>								
		V <sub>CC</sub> = 2.0 V	-	52	160	-	200	-	240	ns
		V <sub>CC</sub> = 4.5 V	-	19	32	-	40	-	48	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	16	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	15	27	-	34	-	41	ns
		nCP to nQ; see <a href="#">Figure 5</a>								
		V <sub>CC</sub> = 2.0 V	-	52	160	-	200	-	240	ns
		V <sub>CC</sub> = 4.5 V	-	19	32	-	40	-	48	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	16	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	15	27	-	34	-	41	ns
		nR to nQ, nQ; see <a href="#">Figure 6</a>								
		V <sub>CC</sub> = 2.0 V	-	52	155	-	195	-	235	ns
		V <sub>CC</sub> = 4.5 V	-	19	31	-	39	-	47	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	16	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	15	26	-	33	-	40	ns
t <sub>t</sub>	transition time	nQ, nQ; see <a href="#">Figure 5</a> <a href="#">[2]</a>								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
t <sub>w</sub>	pulse width	nCP input, HIGH or LOW; see <a href="#">Figure 5</a>								
		V <sub>CC</sub> = 2.0 V	80	22	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	8	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
		nR input, HIGH or LOW; see <a href="#">Figure 6</a>								
		V <sub>CC</sub> = 2.0 V	80	22	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	8	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
t <sub>rec</sub>	recovery time	nR to nCP; see <a href="#">Figure 6</a>								
		V <sub>CC</sub> = 2.0 V	60	19	-	75	-	90	-	ns
		V <sub>CC</sub> = 4.5 V	12	7	-	15	-	18	-	ns
		V <sub>CC</sub> = 6.0 V	20	6	-	13	-	15	-	ns
t <sub>su</sub>	set-up time	nJ, nK to nCP; see <a href="#">Figure 5</a>								
		V <sub>CC</sub> = 2.0 V	100	22	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	8	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	6	-	21	-	26	-	ns

**Table 7. Dynamic characteristics ...continued**GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 7](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_h$	hold time	nJ, nK to $\overline{nCP}$ ; see <a href="#">Figure 5</a>								
		$V_{CC} = 2.0$ V	3	-6	-	3	-	3	-	ns
		$V_{CC} = 4.5$ V	3	-2	-	3	-	3	-	ns
		$V_{CC} = 6.0$ V	3	-2	-	3	-	3	-	ns
$f_{max}$	maximum frequency	$\overline{nCP}$ input; see <a href="#">Figure 5</a>								
		$V_{CC} = 2.0$ V	6	23	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5$ V	30	70	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	78	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	35	85	-	28	-	24	-	MHz
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_I = GND$ to $V_{CC}$	[3]	-	30	-	-	-	-	pF

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$t_{pd}$	propagation delay	$\overline{nCP}$ to nQ; see <a href="#">Figure 5</a>	[1]							
		$V_{CC} = 4.5$ V	-	19	36	-	45	-	54	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns
		$\overline{nCP}$ to $\overline{nQ}$ ; see <a href="#">Figure 5</a>								
		$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns
		$\overline{nR}$ to nQ, $\overline{nQ}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 4.5$ V	-	20	38	-	48	-	57	ns
$t_t$	transition time	nQ, $\overline{nQ}$ ; see <a href="#">Figure 5</a>	[2]							
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
$t_W$	pulse width	$\overline{nCP}$ input, HIGH or LOW; see <a href="#">Figure 5</a>								
		$V_{CC} = 4.5$ V	16	9	-	20	-	24	-	ns
		$\overline{nR}$ input, HIGH or LOW; see <a href="#">Figure 6</a>								
$t_{rec}$	recovery time	$\overline{nR}$ to $\overline{nCP}$ ; see <a href="#">Figure 6</a>								
		$V_{CC} = 4.5$ V	14	8	-	18	-	21	-	ns
$t_{su}$	set-up time	nJ, nK to $\overline{nCP}$ ; see <a href="#">Figure 5</a>								
		$V_{CC} = 4.5$ V	20	7	-	25	-	30	-	ns
$t_h$	hold time	nJ, nK to $\overline{nCP}$ ; see <a href="#">Figure 5</a>								
		$V_{CC} = 4.5$ V	5	-2	-	5	-	5	-	ns

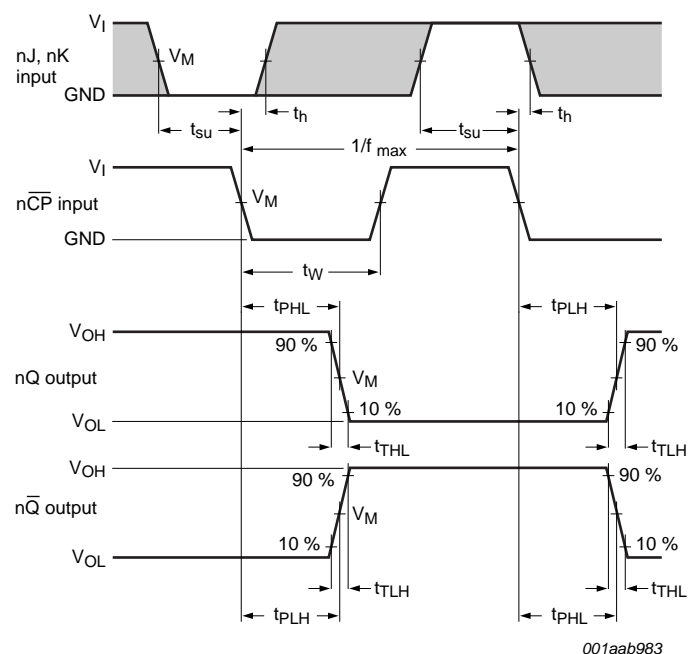


**Table 7. Dynamic characteristics ...continued**GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 7](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$f_{\max}$	maximum frequency	nCP input; see <a href="#">Figure 5</a>								
		$V_{CC} = 4.5$ V	30	66	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	73	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_I = \text{GND to } V_{CC}$	[3]	30	-	-	-	-	-	pF

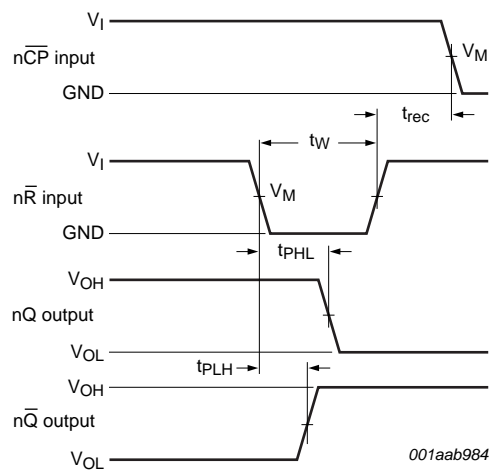
[1]  $t_{pd}$  is the same as  $t_{PHL}$ ,  $t_{PLH}$ .[2]  $t_t$  is the same as  $t_{THL}$ ,  $t_{TLH}$ .[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where: $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V; $N$  = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms



The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in [Table 8](#). $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.**Fig 5. Waveforms showing the clock propagation delays, pulse width, nJ and nK to  $\overline{nCP}$  set-up and hold times, output transition times and maximum clock frequency**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6.** Waveforms showing reset ( $n\overline{R}$ ) input to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays and pulse width, and  $n\overline{R}$  to  $n\overline{CP}$  recovery time

**Table 8.** Measurement points

Type	Input		Output
	$V_I$	$V_M$	$V_M$
74HC107-Q100	$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$
74HCT107-Q100	3 V	1.3 V	1.3 V

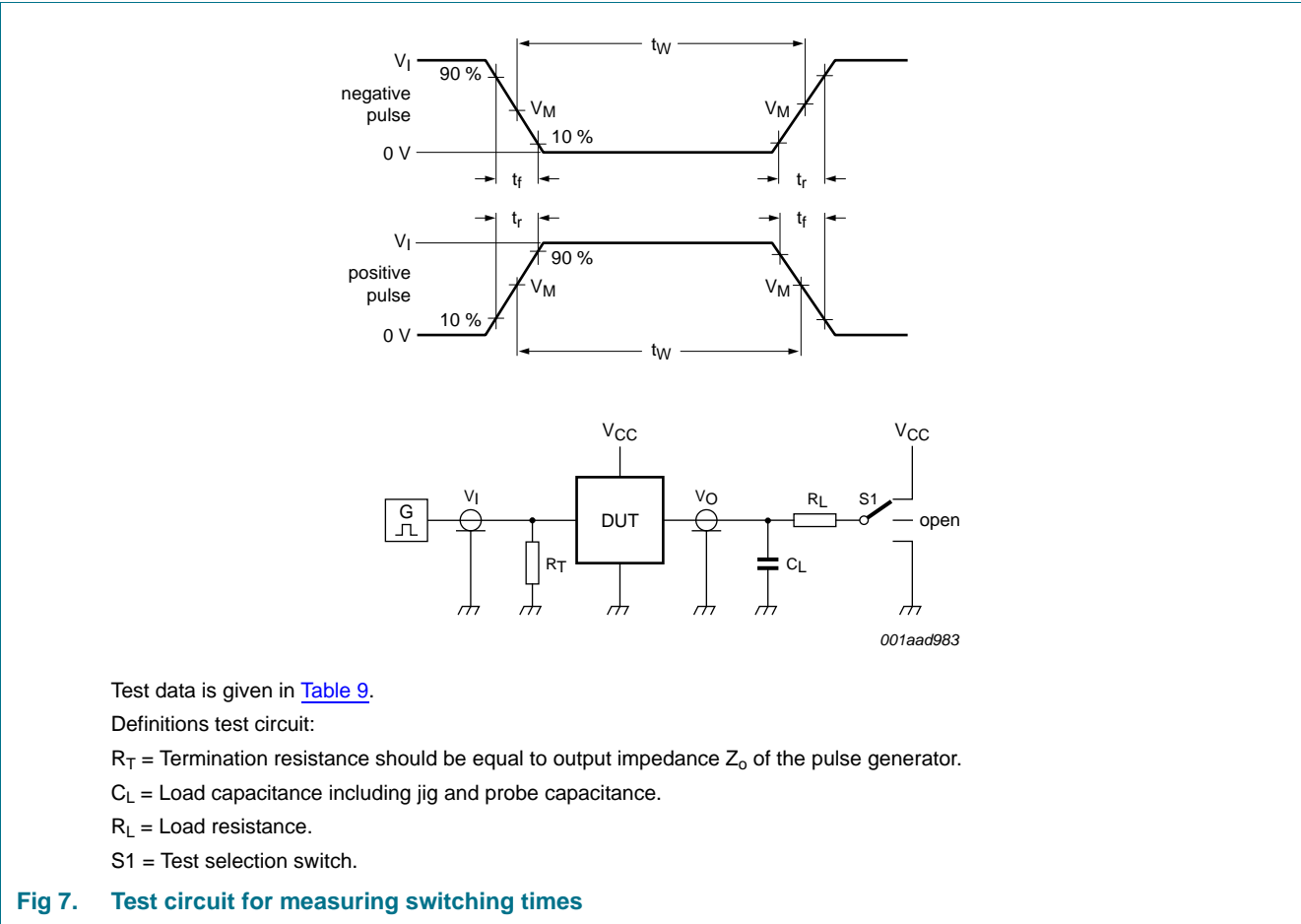


Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC107-Q100	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT107-Q100	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

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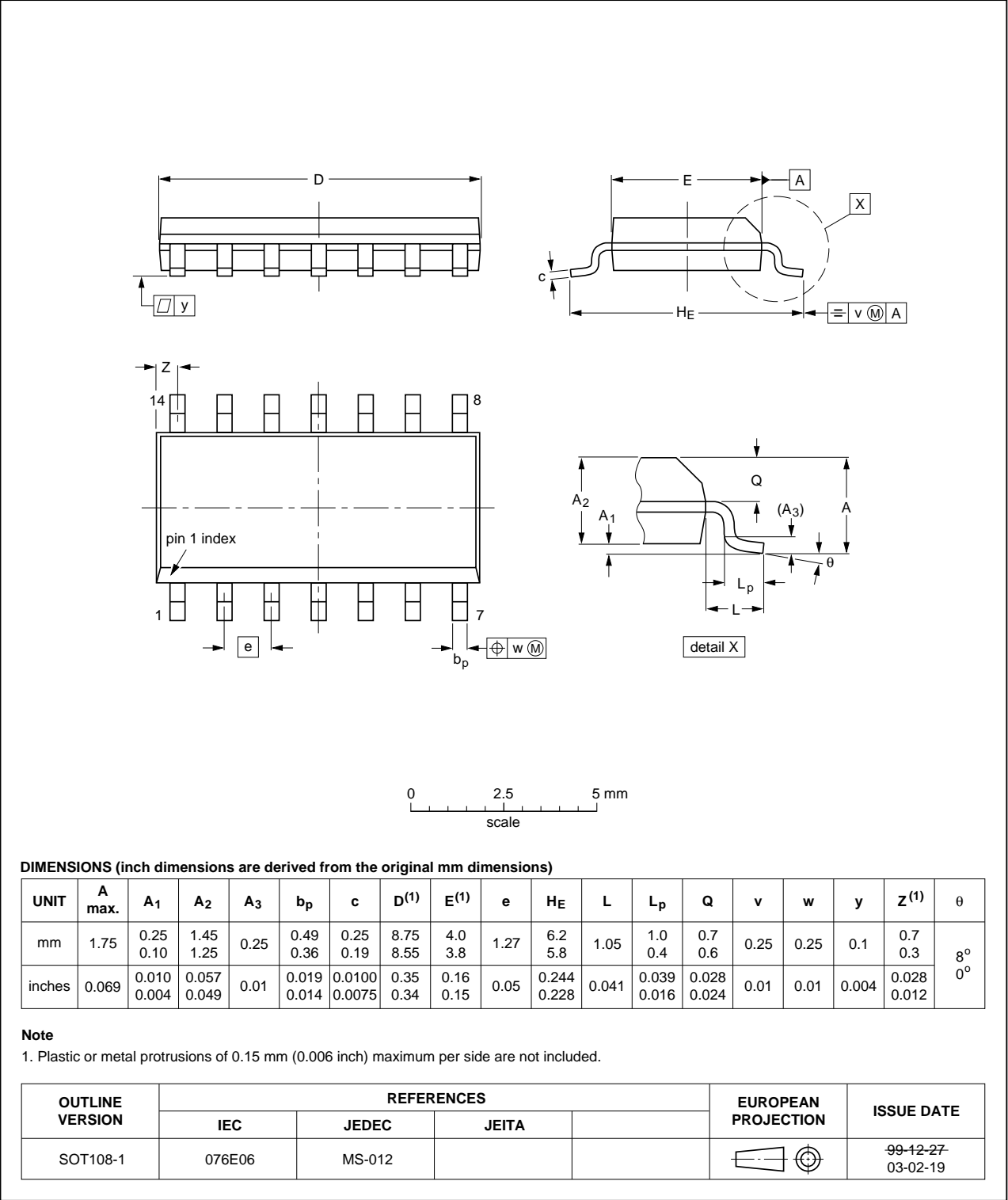


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

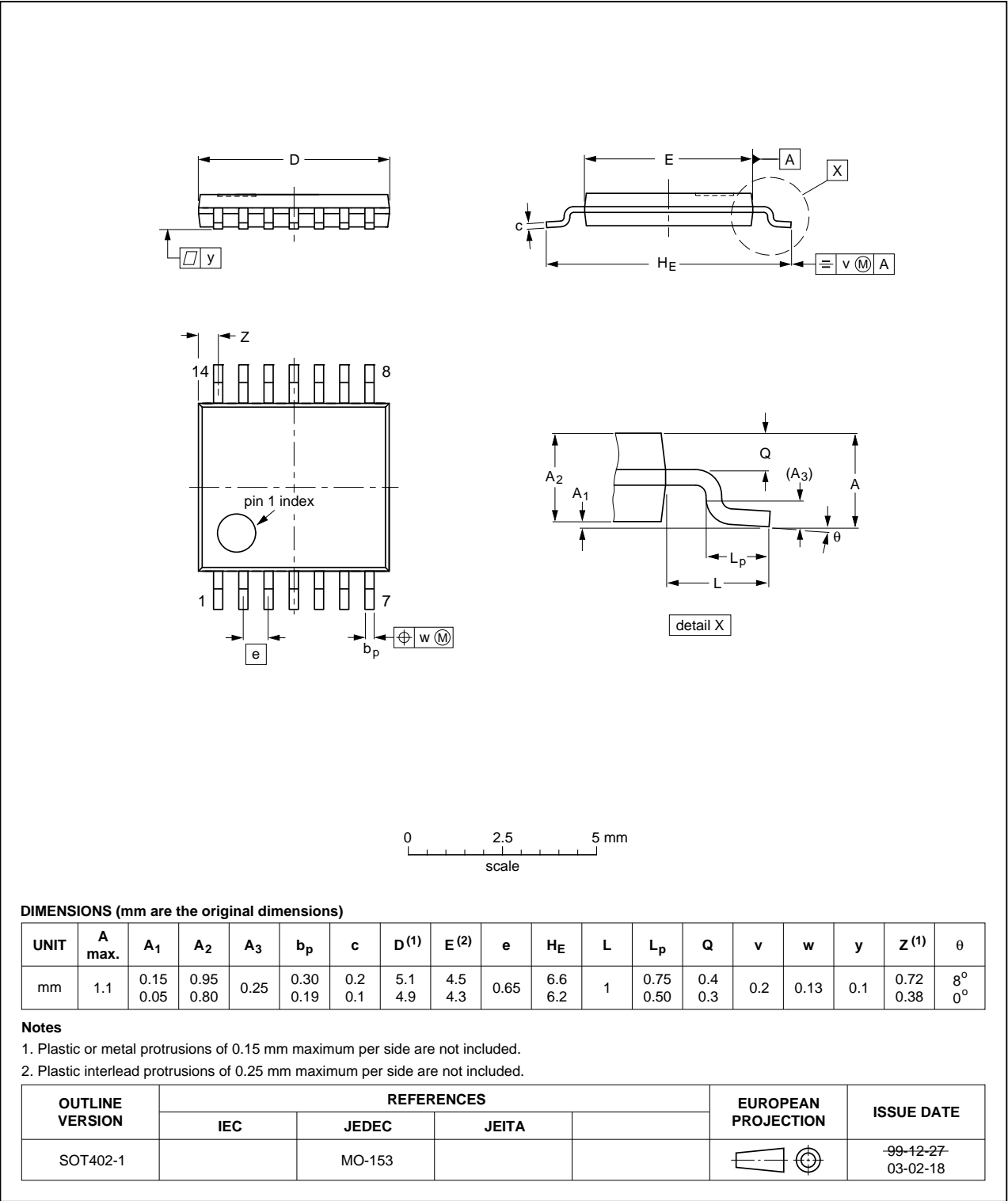


Fig 9. Package outline SOT402-1 (TSSOP14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT107_Q100 v.1	20131118	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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