# 74HC2G00-Q100; 74HCT2G00-Q100

# Dual 2-input NAND gate Rev. 1 — 7 November 2013

**Product data sheet** 

# 1. General description

The 74HC2G00-Q100; 74HCT2G00-Q100 is a dual 2-input NAND gate. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V<sub>CC</sub>.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

#### Features and benefits 2.

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - For 74HC2G00-Q100: CMOS level
  - ◆ For 74HCT2G00-Q100: TTL level
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

# **Ordering information**

Table 1. **Ordering information** 

Type number	Package								
	Temperature range	Name	Description	Version					
74HC2G00DP-Q100	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package;	SOT505-2					
74HCT2G00DP-Q100			8 leads; body width 3 mm; lead length 0.5 mm						
74HC2G00DC-Q100	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package;	SOT765-1					
74HCT2G00DC-Q100			8 leads; body width 2.3 mm						



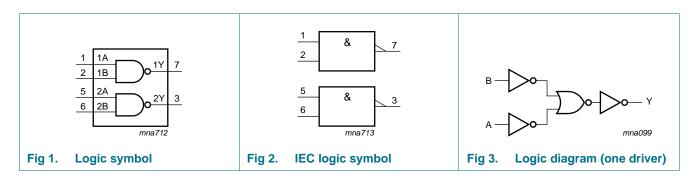
## 4. Marking

Table 2. Marking code

Type number	Marking code <sup>[1]</sup>
74HC2G00DP-Q100	H00
74HCT2G00DP-Q100	T00
74HC2G00DC-Q100	H00
74HCT2G00DC-Q100	T00

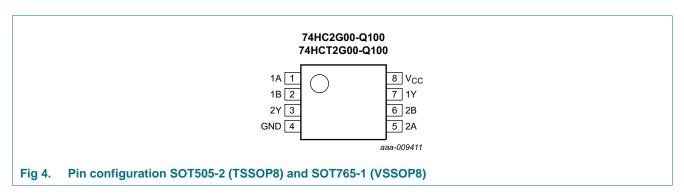
<sup>[1]</sup> The pin 1 indicator is located on the lower left corner of the device, below the marking code.

# 5. Functional diagram



# 6. Pinning information

#### 6.1 Pinning



#### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V <sub>CC</sub>	8	supply voltage

74HC HCT2G00 Q100

# 7. Functional description

Table 4. Function table [1]

Input		Output
nA	nB	nY
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level.

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	±20	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	±20	mA
I <sub>O</sub>	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	<u>[1]</u> _	25	mA
I <sub>CC</sub>	supply current		<u>[1]</u> _	50	mA
I <sub>GND</sub>	ground current		<u>[1]</u> –50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>D</sub>	dynamic power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2] _	300	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	bol Parameter Conditions		74H	74HC2G00-Q100		74HCT2G00-Q100			Unit
			Min	Тур	Max	Min	Тур	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
Vo	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise	$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
	and fall rate	V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

<sup>[2]</sup> For TSSOP8 package: above 55 °C the value of  $P_{tot}$  derates linearly with 2.5 mW/K. For VSSOP8 package: above 110 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

#### 10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T<sub>amb</sub> = 25 °C.

Symbol	Parameter	Conditions	-40	°C to +8	35 °C	-40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	
74HC2G0	00-Q100			'	'	'		'
$V_{IH}$	HIGH-level input	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	V
	voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	V
$V_{IL}$	LOW-level input	V <sub>CC</sub> = 2.0 V	-	8.0	0.5	-	0.5	V
voltage	voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	V
		$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	V
		$I_{O} = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.13	4.32	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.63	5.81	-	5.2	-	V
$V_{OL}$	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$						
	voltage	$I_{O} = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	V
		$I_{O} = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	V
		$I_{O} = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.33	-	0.4	V
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±1.0	-	±1.0	μΑ
I <sub>CC</sub>	supply current	per input pin; $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	10	-	20	μА
Cı	input capacitance		-	1.5	-	-	-	pF

Table 7. Static characteristics ... continued

Voltages are referenced to GND (ground = 0 V). All typical values are measured at  $T_{amb}$  = 25 °C.

Symbol	Parameter	Conditions	-40	–40 °C to +85 °C			-40 °C to +125 °C		
			Min	Тур	Max	Min	Max		
74HCT2G	00-Q100							'	
V <sub>IH</sub>	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	V	
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V	
$V_{OH}$	HIGH-level output	$V_I = V_{IH}$ or $V_{IL}$							
	voltage	$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	V	
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.13	4.32	-	3.7	-	V	
$V_{OL}$	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$							
	voltage	$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	V	
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.33	-	0.4	V	
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	-	±1.0	μΑ	
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	10	-	20	μА	
$\Delta I_{CC}$	additional supply current	per input; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V};$ $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A}$	-	-	375	-	410	μА	
Cı	input capacitance		-	1.5	-	-	-	pF	

# 11. Dynamic characteristics

#### Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); all typical values are measured at T<sub>amb</sub> = 25 °C; for test circuit, see Figure 6.

•		,, ,,			arrio			_	
Symbol	Parameter			-40 °C to +85 °C		–40 °C t	o +125 °C	Unit	
				Min	Тур	Max	Min	Max	
74HC2G	00-Q100		'		'		'	1	•
t <sub>pd</sub>	propagation delay	nA and nB to nY; see Figure 5	<u>[1]</u>						
		V <sub>CC</sub> = 2.0 V		-	25	95	-	110	ns
		V <sub>CC</sub> = 4.5 V		-	9	19	-	22	ns
		V <sub>CC</sub> = 6.0 V		-	7	16	-	20	ns
t <sub>t</sub>	transition time	see Figure 5	[2]						
		V <sub>CC</sub> = 2.0 V		-	18	95	-	125	ns
		V <sub>CC</sub> = 4.5 V		-	6	19	-	25	ns
		V <sub>CC</sub> = 6.0 V		-	5	16	-	20	ns
$C_{PD}$	power dissipation capacitance	$V_I = GND$ to $V_{CC}$	[3]	-	10	-	-	-	pF

Table 8. Dynamic characteristics ... continued

Voltages are referenced to GND (ground = 0 V); all typical values are measured at T<sub>amb</sub> = 25 °C; for test circuit, see Figure 6.

Symbol Parameter Conditions		Conditions		-40 °C to +85 °		5 °C		0 °C to +125 °C □	
		Min	Тур	Max	Min	Max			
74HCT20	G00-Q100							•	
t <sub>pd</sub>	propagation delay	nA and nB to nY; see Figure 5	<u>[1]</u>						
		V <sub>CC</sub> = 4.5 V		-	12	24	-	29	ns
t <sub>t</sub>	transition time	$V_{CC} = 4.5 \text{ V}$ ; see Figure 5	[2]	-	6	19	-	22	ns
$C_{PD}$	power dissipation capacitance	$V_I = GND$ to $V_{CC} - 1.5 V$	[3]	-	10	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [2]  $t_t$  is the same as  $t_{TLH}$  and  $t_{THL}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

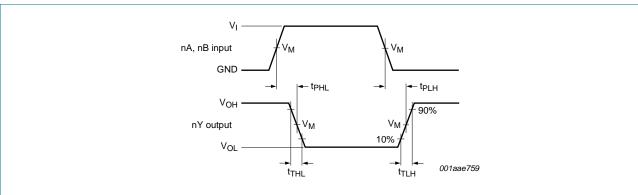
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of outputs.

#### 12. Waveforms



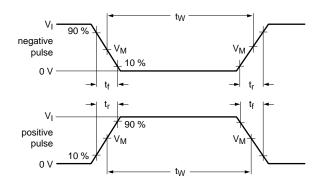
Measurement points are given in Table 9.

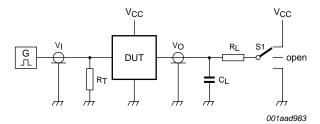
 $V_{\mbox{\scriptsize OL}}$  and  $V_{\mbox{\scriptsize OH}}$  are typical output voltage levels that occur with the output load.

Fig 5. Propagation delay data input (nA, nB) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74HC2G00-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT2G00-Q100	1.3 V	1.3 V





Test data is given in Table 10.

Definitions for test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_L$  = Load resistance.

S1 = Test selection switch.

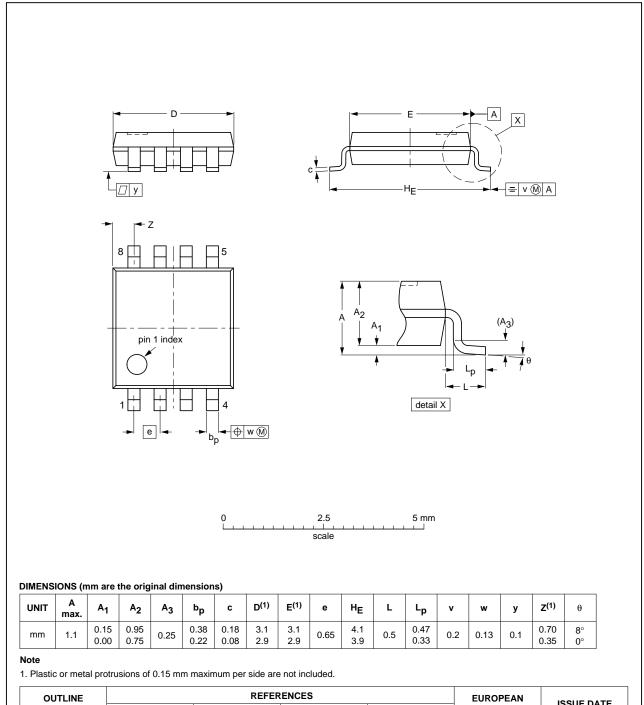
Fig 6. Test circuit for measuring switching times

Table 10. Test data

Туре	Input		Load	S1 position	
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>
74HC2G00-Q100	V <sub>CC</sub>	≤ 6 ns	50 pF	1 kΩ	open
74HCT2G00-Q100	3 V	≤ 6 ns	50 pF	1 kΩ	open

# 13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



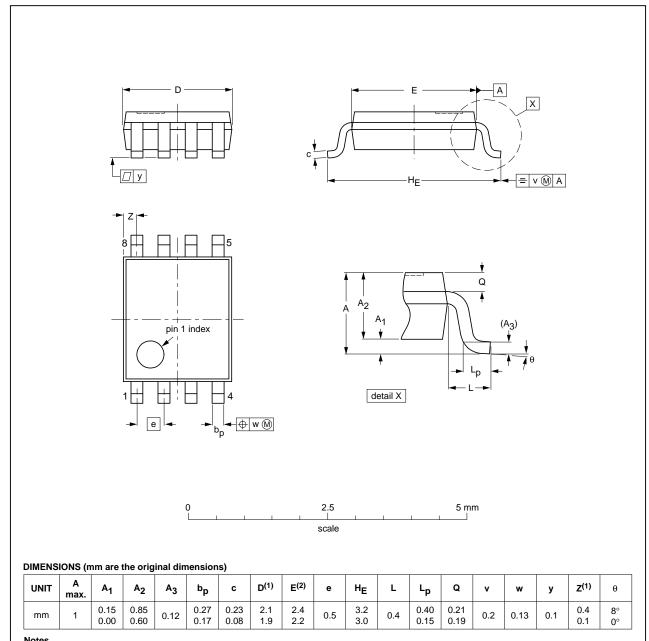
OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT505-2						02-01-16

Fig 7. Package outline SOT505-2 (TSSOP8)

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#### VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT765-1		MO-187				02-06-07

Fig 8. Package outline SOT765-1 (VSSOP8)

74HC\_HCT2G00\_Q100

## 14. Abbreviations

#### Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 15. Revision history

#### Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G00_Q100 v.1	20131107	Product data sheet	-	-

### 16. Legal information

#### 16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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# 74HC2G00-Q100; 74HCT2G00-Q100

**Dual 2-input NAND gate** 

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# 74HC2G00-Q100; 74HCT2G00-Q100

**Dual 2-input NAND gate** 

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