# 74HC4067; 74HCT4067

## 16-channel analog multiplexer/demultiplexer

Rev. 5 — 13 December 2011 Product data sheet

## 1. General description

The 74HC4067; 74HCT4067 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4067B. The device is specified in compliance with JEDEC standard no. 7A.

The 74HC4067; 74HCT4067 is a 16-channel analog multiplexer/demultiplexer with four address inputs (S0 to S3), an active-LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y0 to Y15) and a common input/output (Z).

The 74HC4067; 74HCT4067 contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y15) and the other side connected to a common input/output (Z).

With pin $\overline{E}$ = LOW, one of the sixteen switches is selected by pins S0 to S3 (low impedance ON-state). All unselected switches are in the high-impedance OFF-state. With pin $\overline{E}$ = HIGH, all switches are in the high-impedance OFF-state, independent of pins S0 to S3.

The analog inputs/outputs (Y0 to Y15, and Z) can swing between $V_{CC}$ as a positive limit and GND as a negative limit. $V_{CC}$ to GND may not exceed 10 V.

## 2. Features and benefits

- Low ON resistance:
  - 80 Ω (typical) at $V_{CC}$ = 4.5 V
  - 70 Ω (typical) at $V_{CC}$ = 6.0 V
  - 60 Ω (typical) at $V_{CC}$ = 9.0 V
- Typical ‘break before make’ built-in

## 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| **74HC4067** | | | | |
| 74HC4067N | −40 °C to +125 °C | DIP24 | plastic dual in-line package; 24 leads (600 mil); reverse bending | SOT101-1 |
| 74HC4067D | −40 °C to +125 °C | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| 74HC4067DB | −40 °C to +125 °C | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 |
| 74HC4067PW | −40 °C to +125 °C | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |
| 74HC4067BQ | −40 °C to +125 °C | DHVQFN24 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm | SOT815-1 |
| **74HCT4067** | | | | |
| 74HCT4067N | −40 °C to +125 °C | DIP24 | plastic dual in-line package; 24 leads (600 mil); reverse bending | SOT101-1 |
| 74HCT4067D | −40 °C to +125 °C | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| 74HCT4067DB | −40 °C to +125 °C | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 |
| 74HCT4067PW | −40 °C to +125 °C | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |
| 74HCT4067BQ | −40 °C to +125 °C | DHVQFN24 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm | SOT815-1 |

## 5. Functional diagram

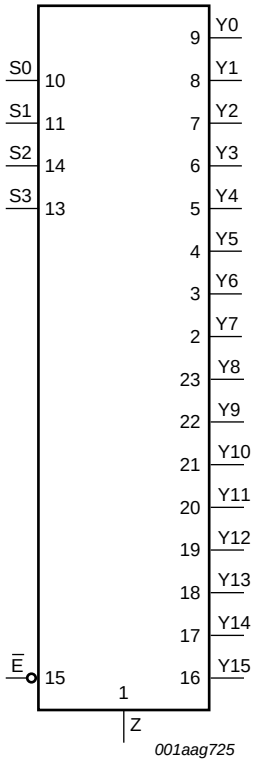



Fig 1. Logic symbol

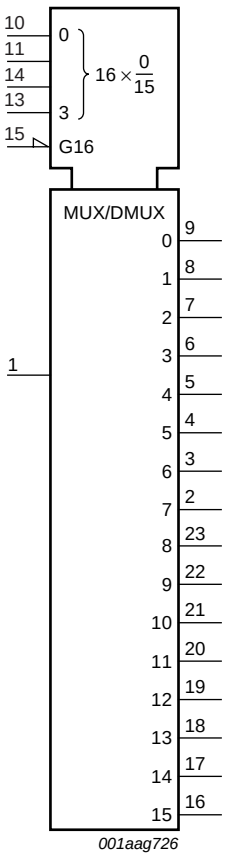



Fig 2. IEC logic symbol

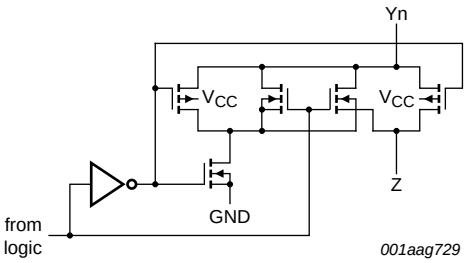



Fig 3. Schematic diagram (one switch)

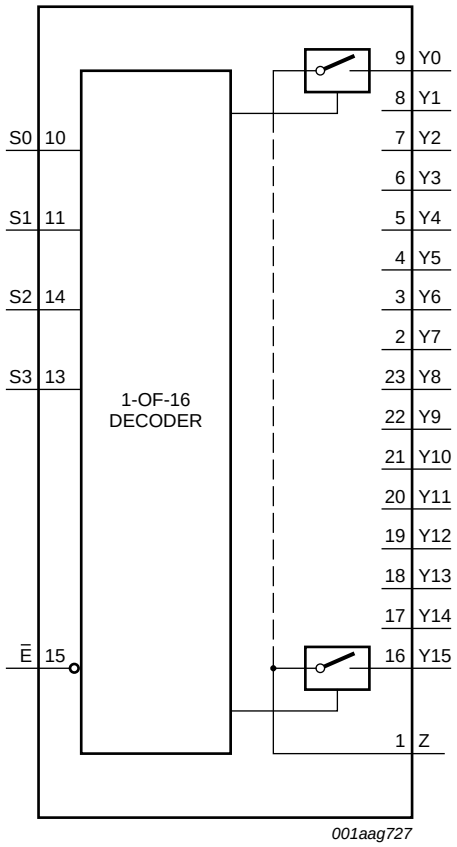



**Fig 4. Functional diagram**

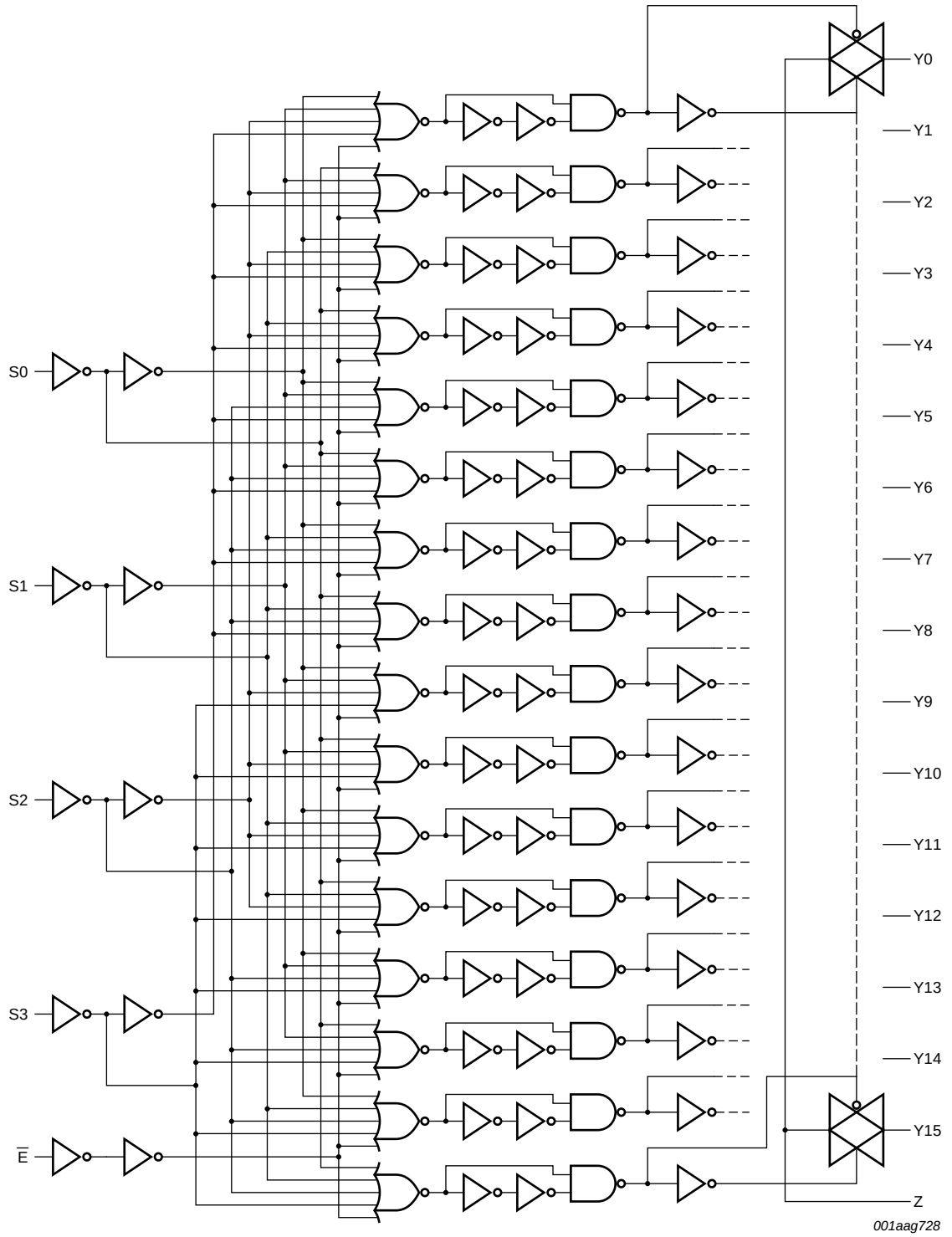



**Fig 5. Logic diagram**

# 6. Pinning information

## 6.1 Pinning

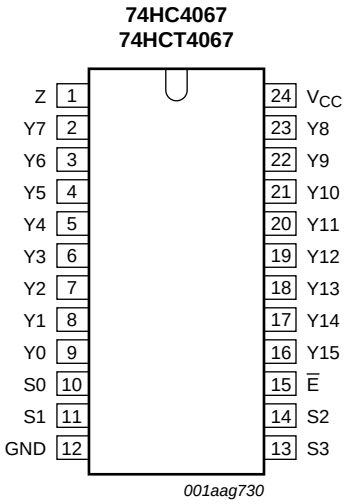
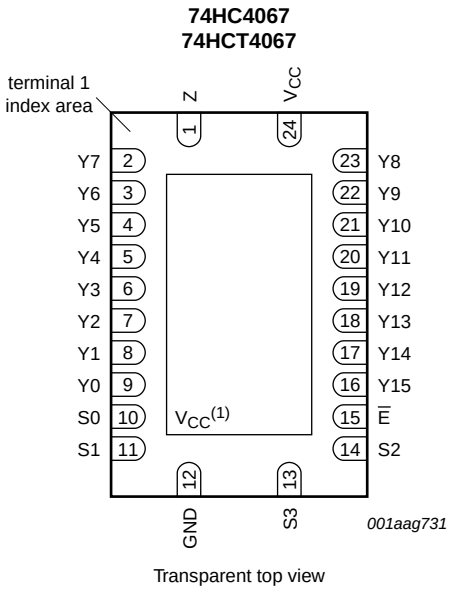



**Fig 6. Pin configuration for DIP24, SO24, SSOP24 and TSSOP24**




Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to $V_{CC}$.

**Fig 7. Pin configuration for DHVQFN24**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| Z | 1 | common input or output |
| Y7, Y6, Y5, Y4, Y3, Y2, Y1, Y0, Y15, Y14, Y13, Y12, Y11, Y10, Y9, Y8 | 2, 3, 4, 5, 6, 7, 8, 9, 16, 17, 18, 19, 20, 21, 22, 23 | independent input or output |
| S0, S1, S3, S2 | 10, 11, 13, 14 | address input 0 |
| GND | 12 | ground (0 V) |
| $\overline{E}$ | 15 | enable input (active LOW) |
| $V_{CC}$ | 24 | supply voltage |

## 7. Functional description

**Table 3. Function table[1]**

| Inputs | | | | | Channel ON |
|---|---|---|---|---|---|
| $\overline{E}$ | S3 | S2 | S1 | S0 | |
| L | L | L | L | L | Y0 to Z |
| L | L | L | L | H | Y1 to Z |
| L | L | L | H | L | Y2 to Z |
| L | L | L | H | H | Y3 to Z |
| L | L | H | L | L | Y4 to Z |
| L | L | H | L | H | Y5 to Z |
| L | L | H | H | L | Y6 to Z |
| L | L | H | H | H | Y7 to Z |
| L | H | L | L | L | Y8 to Z |
| L | H | L | L | H | Y9 to Z |
| L | H | L | H | L | Y10 to Z |
| L | H | L | H | H | Y11 to Z |
| L | H | H | L | L | Y12 to Z |
| L | H | H | L | H | Y13 to Z |
| L | H | H | H | L | Y14 to Z |
| L | H | H | H | H | Y15 to Z |
| H | X | X | X | X | - |

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | [1] | −0.5 | +11.0 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | | - | ±20 | mA |
| $I_{SK}$ | switch clamping current | $V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V | | - | ±20 | mA |
| $I_{SW}$ | switch current | $V_{SW} = -0.5$ V to $V_{CC} + 0.5$ V | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | 50 | mA |
| $I_{GND}$ | ground current | | | - | −50 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |

**Table 4. Limiting values** *...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C | | | | |
| | | DIP24 package | [2] | - | 750 | mW |
| | | SO24 package | [3] | - | 500 | mW |
| | | SSOP24 package | [4] | - | 500 | mW |
| | | TSSOP24 package | [4] | - | 500 | mW |
| | | DHVQFN24 package | [5] | - | 500 | mW |
| P | power dissipation | per switch | | - | 100 | mW |

[1] To avoid drawing $V_{CC}$ current out of terminal Z, when switch current flows in terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no $V_{CC}$ current will flow out of terminals Yn. In this case there is no limit for the voltage drop across the switch, but the voltages at Yn and Z may not exceed $V_{CC}$ or GND.

[2] For DIP24 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[3] For SO24 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

[4] For SSOP24 and TSSOP24 packages: $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

[5] For DHVQFN24 package: $P_{tot}$ derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **74HC4067** | | | | | | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 10.0 | V |
| $V_I$ | input voltage | | GND | - | $V_{CC}$ | V |
| $V_{SW}$ | switch voltage | | GND | - | $V_{CC}$ | V |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 2.0 V | - | - | 625 | ns |
| | | $V_{CC}$ = 4.5 V | - | 1.67 | 139 | ns |
| | | $V_{CC}$ = 6.0 V | - | - | 83 | ns |
| | | $V_{CC}$ = 10.0 V | - | - | 31 | ns |
| $T_{amb}$ | ambient temperature | | −40 | +25 | +125 | °C |
| **74HCT4067** | | | | | | |
| $V_{CC}$ | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | GND | - | $V_{CC}$ | V |
| $V_{SW}$ | switch voltage | | GND | - | $V_{CC}$ | V |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 4.5 V | - | 1.67 | 139 | ns |
| $T_{amb}$ | ambient temperature | | −40 | +25 | +125 | °C |

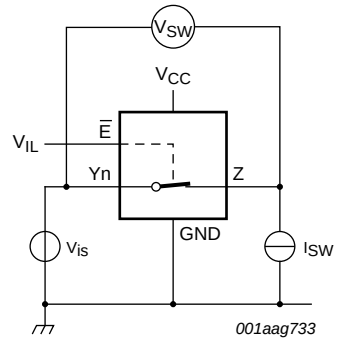
## 10. Static characteristics

**Table 6. $R_{ON}$ resistance per switch for types 74HC4067 and 74HCT4067**

*$V_I = V_{IH}$ or $V_{IL}$; for test circuit see Figure 8.*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*
*For 74HC4067: $V_{CC} - GND$ = 2.0 V, 4.5 V, 6.0 V and 9.0 V.*
*For 74HCT4067: $V_{CC} - GND$ = 4.5 V.*

| Symbol | Parameter | Conditions | | 25 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Max (85 °C) | Max (125 °C) | |
| $R_{ON(peak)}$ | ON resistance (peak) | $V_{is}$ = $V_{CC}$ to GND | | | | | | |
| | | $V_{CC}$ = 2.0 V; $I_{SW}$ = 100 μA | [1] | - | - | - | - | Ω |
| | | $V_{CC}$ = 4.5 V; $I_{SW}$ = 1000 μA | | 110 | 180 | 225 | 270 | Ω |
| | | $V_{CC}$ = 6.0 V; $I_{SW}$ = 1000 μA | | 95 | 160 | 200 | 240 | Ω |
| | | $V_{CC}$ = 9.0 V; $I_{SW}$ = 1000 μA | | 75 | 130 | 165 | 195 | Ω |
| $R_{ON(rail)}$ | ON resistance (rail) | $V_{is}$ = GND or $V_{CC}$ | | | | | | |
| | | $V_{CC}$ = 2.0 V; $I_{SW}$ = 100 μA | [1] | 150 | - | - | - | |
| | | $V_{CC}$ = 4.5 V; $I_{SW}$ = 1000 μA | | 90 | 160 | 200 | 240 | Ω |
| | | $V_{CC}$ = 6.0 V; $I_{SW}$ = 1000 μA | | 80 | 140 | 175 | 210 | Ω |
| | | $V_{CC}$ = 9.0 V; $I_{SW}$ = 1000 μA | | 70 | 120 | 150 | 180 | Ω |
| $\Delta R_{ON}$ | ON resistance mismatch between channels | $V_{is}$ = $V_{CC}$ to GND | | | | | | |
| | | $V_{CC}$ = 2.0 V | [1] | - | - | - | - | Ω |
| | | $V_{CC}$ = 4.5 V | | 9 | - | - | - | Ω |
| | | $V_{CC}$ = 6.0 V | | 8 | - | - | - | Ω |
| | | $V_{CC}$ = 9.0 V | | 6 | - | - | - | Ω |

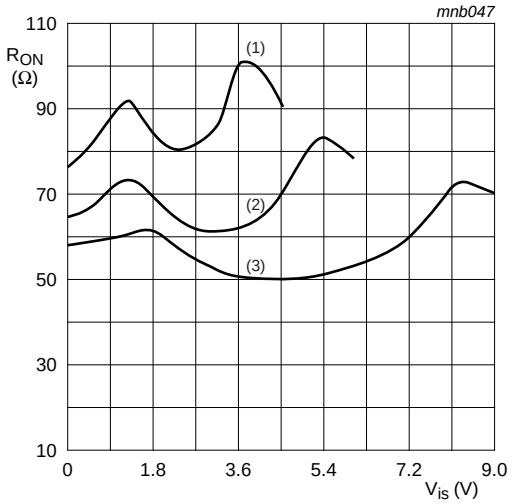
[1] At supply voltages ($V_{CC}$ − GND) approaching 2 V, the analog switch ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.




$V_{is}$ = 0 V to ($V_{CC}$ − GND)

$$R_{ON} = \frac{V_{SW}}{I_{SW}}$$

**Fig 8. Test circuit for measuring $R_{ON}$**




$V_{is}$ = 0 V to ($V_{CC}$ − GND)

(1) $V_{CC}$ = 4.5 V

(2) $V_{CC}$ = 6.0 V

(3) $V_{CC}$ = 9.0 V

**Fig 9. Typical $R_{ON}$ as a function of input voltage $V_{is}$**

**Table 7. Static characteristics 74HC4067**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = 25 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | 1.2 | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | 2.4 | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | 3.2 | - | V |
| | | $V_{CC}$ = 9.0 V | 6.3 | 4.7 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | 0.8 | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | - | 2.1 | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | 2.8 | 1.80 | V |
| | | $V_{CC}$ = 9.0 V | - | 4.3 | 2.70 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND | | | | |
| | | $V_{CC}$ = 6.0 V | - | - | ±0.1 | μA |
| | | $V_{CC}$ = 10.0 V | - | - | ±0.2 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 10.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\lvert V_{SW}\rvert$ = $V_{CC}$ − GND; see Figure 10 | | | | |
| | | per channel | - | - | ±0.1 | μA |
| | | all channels | - | - | ±0.8 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 10.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\lvert V_{SW}\rvert$ = $V_{CC}$ − GND; see Figure 11 | - | - | ±0.8 | μA |

**Table 7. Static characteristics 74HC4067** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $V_{is}$ = GND or $V_{CC}$; $V_{os} = V_{CC}$ or GND | | | | |
| | | $V_{CC}$ = 6.0 V | - | - | 8.0 | μA |
| | | $V_{CC}$ = 10.0 V | - | - | 16.0 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | pF |
| **$T_{amb}$ = –40 °C to +85 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | - | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | - | - | V |
| | | $V_{CC}$ = 9.0 V | 6.3 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.50 | V |
| | | $V_{CC}$ = 4.5 V | - | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | - | 1.80 | V |
| | | $V_{CC}$ = 9.0 V | - | - | 2.70 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND | | | | |
| | | $V_{CC}$ = 6.0 V | - | - | ±1.0 | μA |
| | | $V_{CC}$ = 10.0 V | - | - | ±2.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 10.0 V; $V_I = V_{IH}$ or $V_{IL}$; $\|V_{SW}\| = V_{CC} - GND$; see Figure 10 | | | | |
| | | per channel | - | - | ±1.0 | μA |
| | | all channels | - | - | ±8.0 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 10.0 V; $V_I = V_{IH}$ or $V_{IL}$; $\|V_{SW}\| = V_{CC} - GND$; see Figure 11 | - | - | ±8.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $V_{is}$ = GND or $V_{CC}$; $V_{os} = V_{CC}$ or GND | | | | |
| | | $V_{CC}$ = 6.0 V | - | - | 80.0 | μA |
| | | $V_{CC}$ = 10.0 V | - | - | 160 | μA |
| **$T_{amb}$ = –40 °C to +125 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | - | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | - | - | V |
| | | $V_{CC}$ = 9.0 V | 6.3 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.50 | V |
| | | $V_{CC}$ = 4.5 V | - | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | - | 1.80 | V |
| | | $V_{CC}$ = 9.0 V | - | - | 2.70 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND | | | | |
| | | $V_{CC}$ = 6.0 V | - | - | ±1.0 | μA |
| | | $V_{CC}$ = 10.0 V | - | - | ±2.0 | μA |

**Table 7. Static characteristics 74HC4067** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 10.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 10 | | | | |
| | | per channel | - | - | ±1.0 | μA |
| | | all channels | - | - | ±8.0 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 10.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 11 | - | - | ±8.0 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $V_{is}$ = GND or $V_{CC}$; $V_{os}$ = $V_{CC}$ or GND | | | | |
| | | $V_{CC}$ = 6.0 V | - | - | 160 | μA |
| | | $V_{CC}$ = 10.0 V | - | - | 320 | μA |

**Table 8. Static characteristics 74HCT4067**

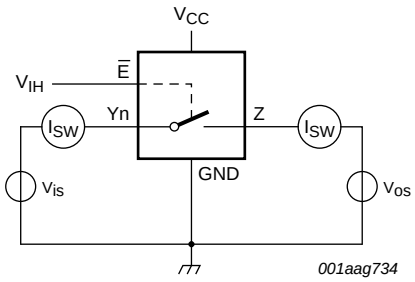
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = 25 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | 1.6 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | 1.2 | 0.8 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.1 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 10 | | | | |
| | | per channel | - | - | ±0.1 | μA |
| | | all channels | - | - | ±0.8 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 11 | - | - | ±0.8 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $V_{is}$ = GND or $V_{CC}$; $V_{os}$ = $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | - | - | 8.0 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = $V_{CC}$ − 2.1 V; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | | | | |
| | | pin $\overline{E}$ | - | 60 | 216 | μA |
| | | pin Sn | - | 50 | 180 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | pF |
| **$T_{amb}$ = −40 °C to +85 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±1.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 10 | | | | |
| | | per channel | - | - | ±1.0 | μA |
| | | all channels | - | - | ±8.0 | μA |

**Table 8. Static characteristics 74HCT4067** *...continued*

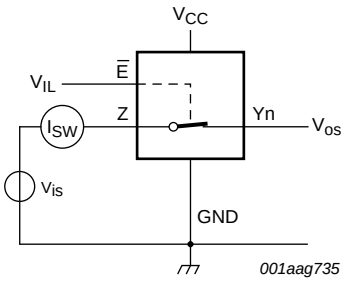
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 11 | - | - | ±8.0 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $V_{is}$ = GND or $V_{CC}$; $V_{os}$ = $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | - | - | 80.0 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = $V_{CC}$ − 2.1 V; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | | | | |
| | | pin $\overline{E}$ | - | - | 270 | μA |
| | | pin Sn | - | - | 225 | μA |
| **$T_{amb}$ = –40 °C to +125 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±1.0 | μA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 10 | | | | |
| | | per channel | - | - | ±1.0 | μA |
| | | all channels | - | - | ±8.0 | μA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $\|V_{SW}\|$ = $V_{CC}$ − GND; see Figure 11 | - | - | ±8.0 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $V_{is}$ = GND or $V_{CC}$; $V_{os}$ = $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | - | - | 160 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = $V_{CC}$ − 2.1 V; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | | | | |
| | | pin $\overline{E}$ | - | - | 294 | μA |
| | | pin Sn | - | - | 245 | μA |




$V_{is}$ = $V_{CC}$ and $V_{os}$ = GND
$V_{is}$ = GND and $V_{os}$ = $V_{CC}$

**Fig 10. Test circuit for measuring OFF-state leakage current**




$V_{is}$ = $V_{CC}$ and $V_{os}$ = open
$V_{is}$ = GND and $V_{os}$ = open

**Fig 11. Test circuit for measuring ON-state leakage current**

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics 74HC4067**

*GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF unless specified otherwise; for test circuit see Figure 14.*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | 25 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Typ | Max | Max (85 °C) | Max (125 °C) | |
| $t_{pd}$ | propagation delay | Yn to Z; see Figure 12 [1][2] | | | | | |
| | | $V_{CC}$ = 2.0 V | 25 | 75 | 95 | 110 | ns |
| | | $V_{CC}$ = 4.5 V | 9 | 15 | 19 | 22 | ns |
| | | $V_{CC}$ = 6.0 V | 7 | 13 | 16 | 19 | ns |
| | | $V_{CC}$ = 9.0 V | 5 | 9 | 11 | 14 | ns |
| | | Z to Yn | | | | | |
| | | $V_{CC}$ = 2.0 V | 18 | 60 | 75 | 90 | ns |
| | | $V_{CC}$ = 4.5 V | 6 | 12 | 15 | 18 | ns |
| | | $V_{CC}$ = 6.0 V | 5 | 10 | 13 | 15 | ns |
| | | $V_{CC}$ = 9.0 V | 4 | 8 | 10 | 12 | ns |
| $t_{off}$ | turn-off time | $\overline{E}$ to Yn; see Figure 13 [3] | | | | | |
| | | $V_{CC}$ = 2.0 V | 74 | 250 | 315 | 375 | ns |
| | | $V_{CC}$ = 4.5 V | 27 | 50 | 63 | 75 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | 27 | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | 22 | 43 | 54 | 64 | ns |
| | | $V_{CC}$ = 9.0 V | 20 | 38 | 48 | 57 | ns |
| | | Sn to Yn | | | | | |
| | | $V_{CC}$ = 2.0 V | 83 | 250 | 315 | 375 | ns |
| | | $V_{CC}$ = 4.5 V | 30 | 50 | 63 | 75 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | 29 | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | 24 | 43 | 54 | 64 | ns |
| | | $V_{CC}$ = 9.0 V | 21 | 38 | 48 | 57 | ns |
| | | $\overline{E}$ to Z | | | | | |
| | | $V_{CC}$ = 2.0 V | 85 | 275 | 345 | 415 | ns |
| | | $V_{CC}$ = 4.5 V | 31 | 55 | 69 | 83 | ns |
| | | $V_{CC}$ = 6.0 V | 25 | 47 | 59 | 71 | ns |
| | | $V_{CC}$ = 9.0 V | 24 | 42 | 53 | 63 | ns |
| | | Sn to Z | | | | | |
| | | $V_{CC}$ = 2.0 V | 94 | 290 | 365 | 435 | ns |
| | | $V_{CC}$ = 4.5 V | 34 | 58 | 73 | 87 | ns |
| | | $V_{CC}$ = 6.0 V | 27 | 47 | 62 | 74 | ns |
| | | $V_{CC}$ = 9.0 V | 25 | 45 | 56 | 68 | ns |

**Table 9. Dynamic characteristics 74HC4067** *…continued*

*GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF unless specified otherwise; for test circuit see Figure 14.*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | | 25 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Max (85 °C) | Max (125 °C) | |
| $t_{on}$ | turn-on time | $\overline{E}$ to Yn; see Figure 13 | [4] | | | | | |
| | | $V_{CC}$ = 2.0 V | | 80 | 275 | 345 | 415 | ns |
| | | $V_{CC}$ = 4.5 V | | 29 | 55 | 69 | 83 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | 26 | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | | 23 | 47 | 59 | 71 | ns |
| | | $V_{CC}$ = 9.0 V | | 17 | 42 | 53 | 63 | ns |
| | | Sn to Yn | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 88 | 300 | 375 | 450 | ns |
| | | $V_{CC}$ = 4.5 V | | 32 | 60 | 75 | 90 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | 29 | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | | 26 | 51 | 64 | 77 | ns |
| | | $V_{CC}$ = 9.0 V | | 18 | 45 | 56 | 68 | ns |
| | | $\overline{E}$ to Z | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 85 | 275 | 345 | 415 | ns |
| | | $V_{CC}$ = 4.5 V | | 31 | 55 | 69 | 83 | ns |
| | | $V_{CC}$ = 6.0 V | | 25 | 47 | 59 | 71 | ns |
| | | $V_{CC}$ = 9.0 V | | 18 | 42 | 53 | 63 | ns |
| | | Sn to Z | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 94 | 300 | 375 | 450 | ns |
| | | $V_{CC}$ = 4.5 V | | 34 | 60 | 75 | 90 | ns |
| | | $V_{CC}$ = 6.0 V | | 27 | 51 | 64 | 77 | ns |
| | | $V_{CC}$ = 9.0 V | | 19 | 45 | 56 | 68 | ns |
| $C_{PD}$ | power dissipation capacitance | per switch; $V_I$ = GND to $V_{CC}$ | [5] | 29 | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3] $t_{on}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.

[4] $t_{off}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$\Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
$C_L$ = output load capacitance in pF;
$C_{sw}$ = switch capacitance in pF;
$V_{CC}$ = supply voltage in V.

**Table 10. Dynamic characteristics 74HCT4067**

*GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF unless specified otherwise; for test circuit see Figure 14.*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | | 25 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Max (85 °C) | Max (125 °C) | |
| $t_{pd}$ | propagation delay | Yn to Z; see Figure 12 | [1][2] | | | | | |
| | | $V_{CC}$ = 4.5 V | | 9 | 15 | 19 | 22 | ns |
| | | Z to Yn | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 6 | 12 | 15 | 18 | ns |
| $t_{off}$ | turn-off time | $\overline{E}$ to Yn; see Figure 13 | [3] | | | | | |
| | | $V_{CC}$ = 4.5 V | | 26 | 55 | 69 | 83 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | 26 | - | - | - | ns |
| | | Sn to Yn | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 31 | 55 | 69 | 83 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | 30 | - | - | - | ns |
| | | $\overline{E}$ to Z | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 30 | 60 | 75 | 90 | ns |
| | | Sn to Z | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 35 | 60 | 75 | 90 | ns |
| $t_{on}$ | turn-on time | $\overline{E}$ to Yn; see Figure 13 | [4] | | | | | |
| | | $V_{CC}$ = 4.5 V | | 32 | 60 | 75 | 90 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | 32 | - | - | - | ns |
| | | Sn to Yn | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 35 | 60 | 75 | 90 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | 33 | - | - | - | ns |
| | | $\overline{E}$ to Z | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 38 | 65 | 81 | 98 | ns |
| | | Sn to Z | | | | | | |
| | | $V_{CC}$ = 4.5 V | | 38 | 65 | 81 | 98 | ns |
| $C_{PD}$ | power dissipation capacitance | per switch; $V_I$ = GND to ($V_{CC}$ – 1.5 V) | [5] | 29 | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3] $t_{on}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.

[4] $t_{off}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
$C_L$ = output load capacitance in pF;
$C_{sw}$ = switch capacitance in pF;
$V_{CC}$ = supply voltage in V.

## 12. Waveforms

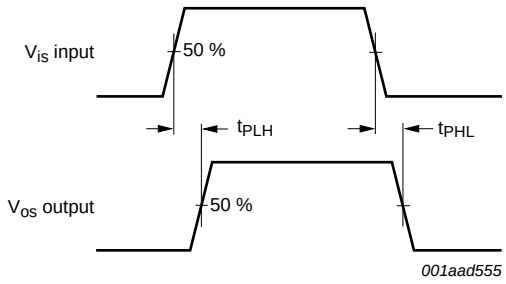
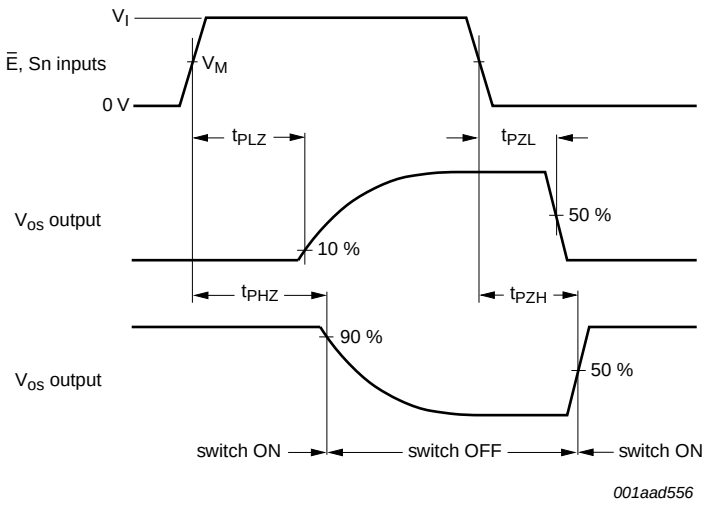



**Fig 12. Input ($V_{is}$) to output ($V_{os}$) propagation delays**

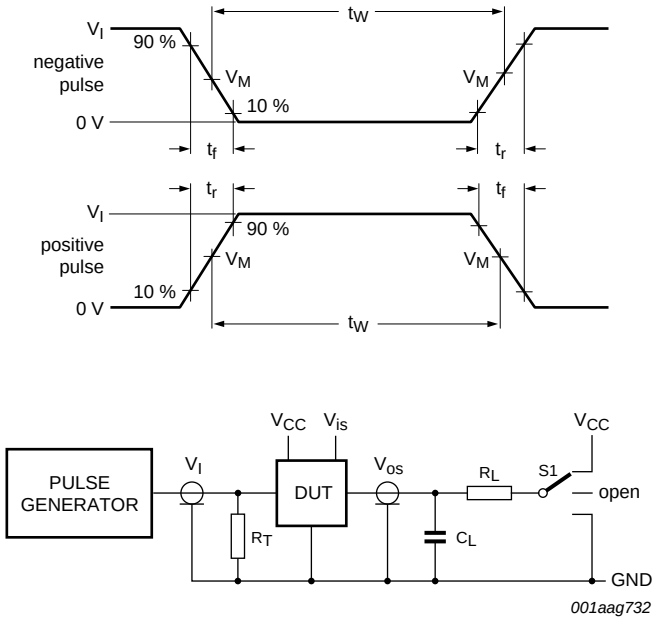



Measurement points are shown in Table 11.

**Fig 13. Turn-on and turn-off times**

**Table 11. Measurement points**

| Type | $V_I$ | $V_M$ |
|---|---|---|
| 74HC4067 | $V_{CC}$ | $0.5V_{CC}$ |
| 74HCT4067 | 3.0 V | 1.3 V |




Test data is given in Table 12.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistor.

S1 = Test selection switch.

**Fig 14. Load circuitry for measuring switching times**

**Table 12. Test data**

| Test | Input | | | | Output | | S1 position |
|---|---|---|---|---|---|---|---|
| | Control $\overline{E}$ | Address Sn | Switch Yn (Z) | $t_r$, $t_f$ | Switch Z (Yn) | | |
| | $V_I$[1] | $V_I$[1] | $V_{is}$ | | $C_L$ | $R_L$ | |
| $t_{PHL}$, $t_{PLH}$ | GND | GND or $V_{CC}$ | GND to $V_{CC}$ | 6 ns | 50 pF | - | open |
| $t_{PHZ}$, $t_{PZH}$ | GND to $V_{CC}$ | GND to $V_{CC}$ | $V_{CC}$ | 6 ns | 50 pF, 15 pF | 1 kΩ | GND |
| $t_{PLZ}$, $t_{PZL}$ | GND to $V_{CC}$ | GND to $V_{CC}$ | GND | 6 ns | 50 pF, 15 pF | 1 kΩ | $V_{CC}$ |

[1] For 74HCT4067: maximum input voltage $V_I$ = 3.0 V.

## 13. Additional dynamic characteristics

**Table 13. Additional dynamic characteristics**

*Recommended conditions and typical values; GND = 0 V; $T_{amb}$ = 25 °C.*
*$V_{is}$ is the input voltage at a Yn or Z terminal, whichever is assigned as an input.*
*$V_{os}$ is the output voltage at a Yn or Z terminal, whichever is assigned as an output.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| THD | total harmonic distortion | $R_L$ = 10 kΩ; $C_L$ = 50 pF; see Figure 15 | | | | | |
| | | $f_i$ = 1 kHz | | | | | |
| | | $V_{CC}$ = 4.5 V; $V_{is(p-p)}$ = 4.0 V | | - | 0.04 | - | % |
| | | $V_{CC}$ = 9.0 V; $V_{is(p-p)}$ = 8.0 V | | - | 0.02 | - | % |
| | | $f_i$ = 10 kHz | | | | | |
| | | $V_{CC}$ = 4.5 V; $V_{is(p-p)}$ = 4.0 V | | - | 0.12 | - | % |
| | | $V_{CC}$ = 9.0 V; $V_{is(p-p)}$ = 8.0 V | | - | 0.06 | - | % |
| $\alpha_{iso}$ | isolation (OFF-state) | $R_L$ = 600 Ω; $C_L$ = 50 pF; see Figure 16 | [1] | | | | |
| | | $V_{CC}$ = 4.5 V | | - | −50 | - | dB |
| | | $V_{CC}$ = 9.0 V | | - | −50 | - | dB |
| $f_{(-3dB)}$ | −3 dB frequency response | $R_L$ = 50 Ω; $C_L$ = 10 pF; see Figure 17 | [2] | | | | |
| | | $V_{CC}$ = 4.5 V | | - | 90 | - | MHz |
| | | $V_{CC}$ = 9.0 V | | - | 100 | - | MHz |
| $C_{sw}$ | switch capacitance | independent pins Y | | - | 5 | - | pF |
| | | common pin Z | | - | 45 | - | pF |

[1] Adjust input voltage $V_{is}$ to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Adjust input voltage $V_{is}$ to 0 dBm level at $V_{os}$ for $f_i$ = 1 MHz (0 dBm = 1 mW into 50 Ω). After set-up, $f_i$ is increased to obtain a reading of −3 dB at $V_{os}$.

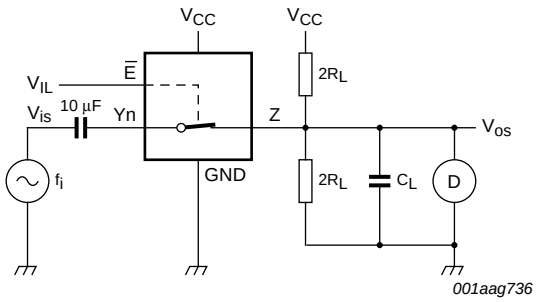
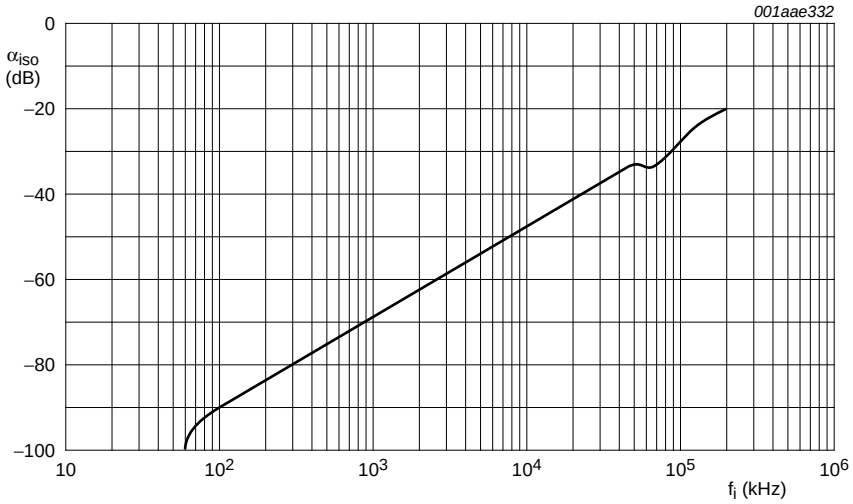
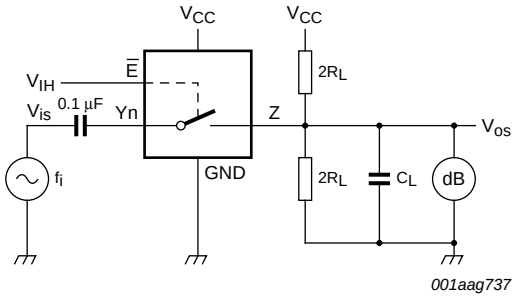



**Fig 15. Test circuit for measuring total harmonic distortion**



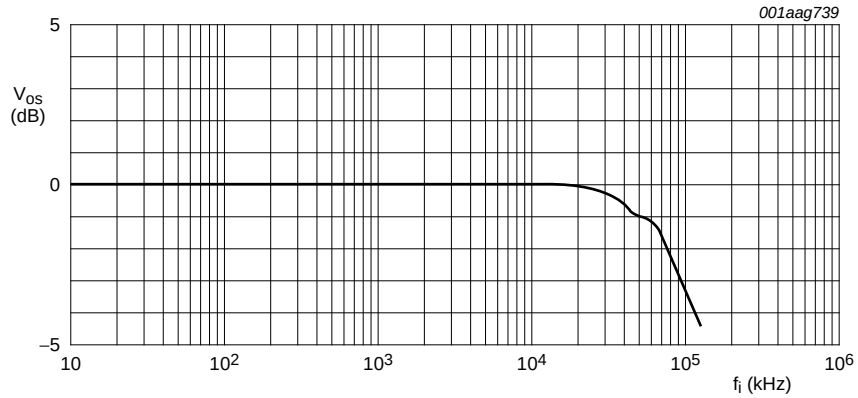

a. Isolation (OFF-state)



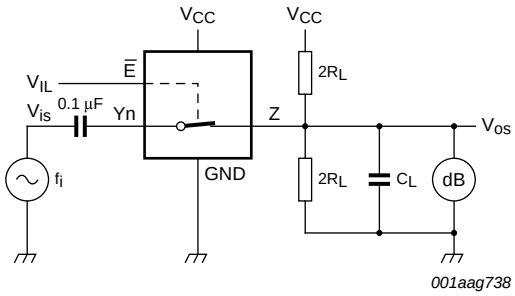

b. Test circuit

$V_{CC}$ = 4.5 V; GND = 0 V; $R_L$ = 600 Ω; $R_{source}$ = 1 kΩ.

**Fig 16. Isolation (OFF-state) as a function of frequency**




a. Typical −3 dB frequency response



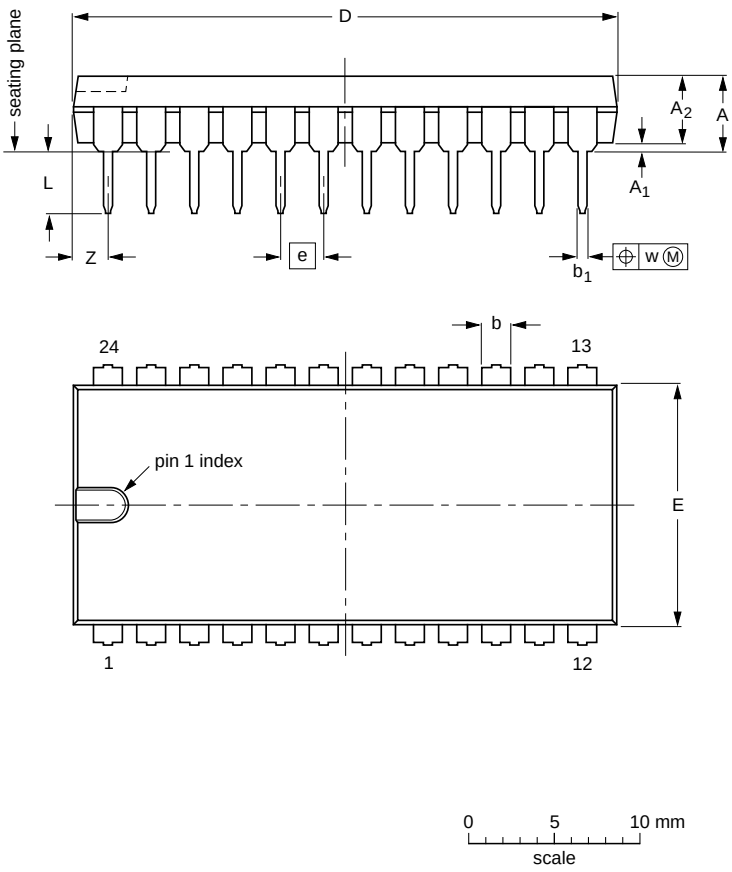

b. Test circuit

$V_{CC}$ = 4.5 V; GND = 0 V; $R_L$ = 50 Ω; $R_{source}$ = 1 kΩ.

**Fig 17. –3 dB frequency response**

## 14. Package outline

**DIP24: plastic dual in-line package; 24 leads (600 mil)** **SOT101-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.1 | 0.51 | 4 | 1.7<br>1.3 | 0.53<br>0.38 | 0.32<br>0.23 | 32.0<br>31.4 | 14.1<br>13.7 | 2.54 | 15.24 | 3.9<br>3.4 | 15.80<br>15.24 | 17.15<br>15.90 | 0.25 | 2.2 |
| inches | 0.2 | 0.02 | 0.16 | 0.066<br>0.051 | 0.021<br>0.015 | 0.013<br>0.009 | 1.26<br>1.24 | 0.56<br>0.54 | 0.1 | 0.6 | 0.15<br>0.13 | 0.62<br>0.60 | 0.68<br>0.63 | 0.01 | 0.087 |

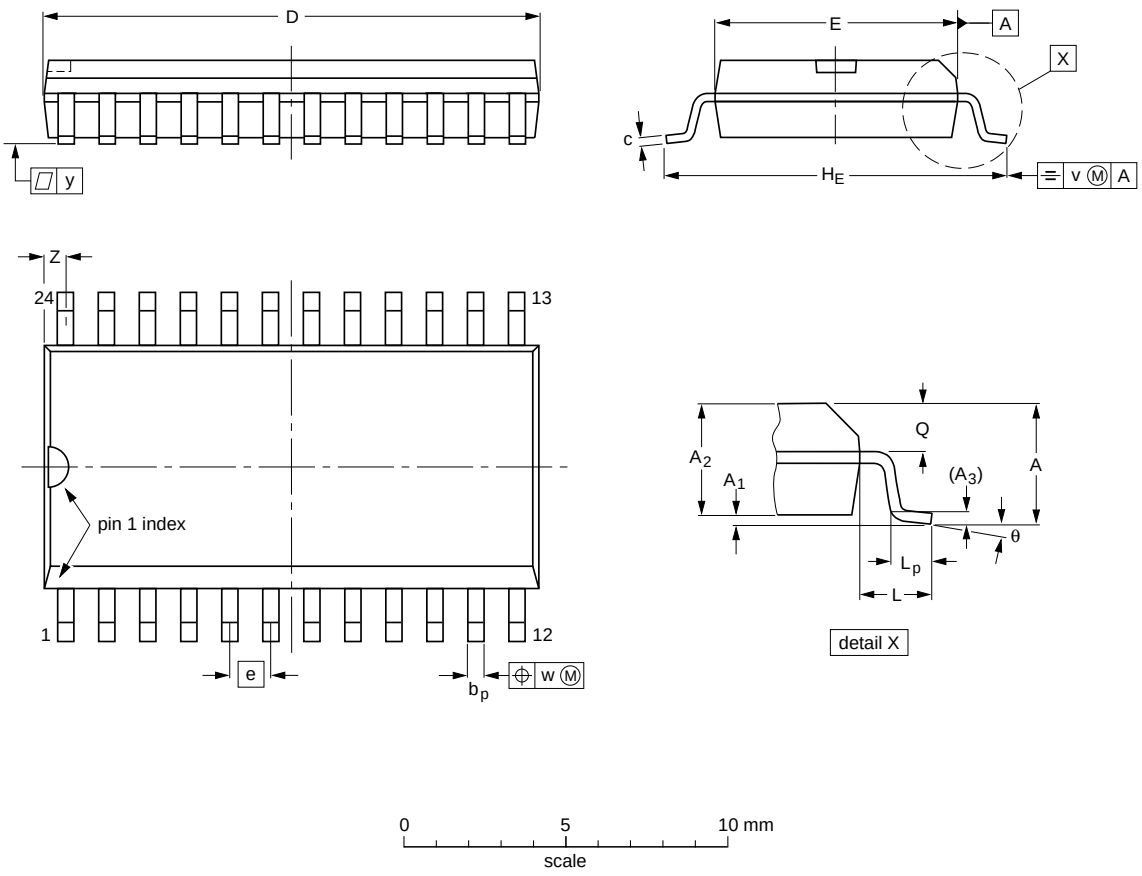
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT101-1 | 051G02 | MO-015 | SC-509-24 | | | ~~99-12-27~~<br>03-02-13 |

**Fig 18. Package outline SOT101-1 (DIP24)**

**SO24: plastic small outline package; 24 leads; body width 7.5 mm** **SOT137-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 15.6<br>15.2 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

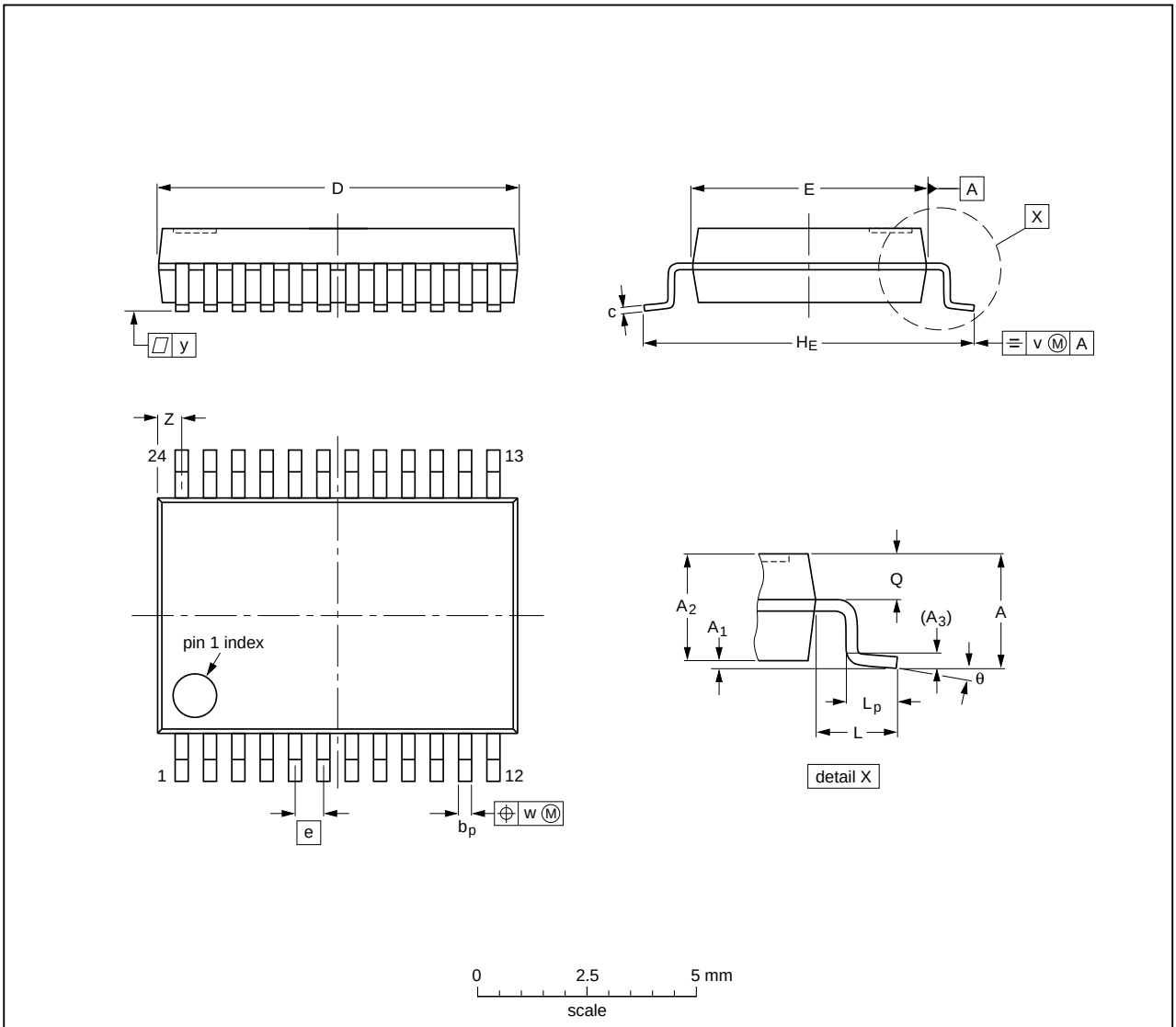
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT137-1 | 075E05 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 19. Package outline SOT137-1 (SO24)**

**SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm** **SOT340-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 8.4<br>8.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.8<br>0.4 | $8^o$<br>$0^o$ |

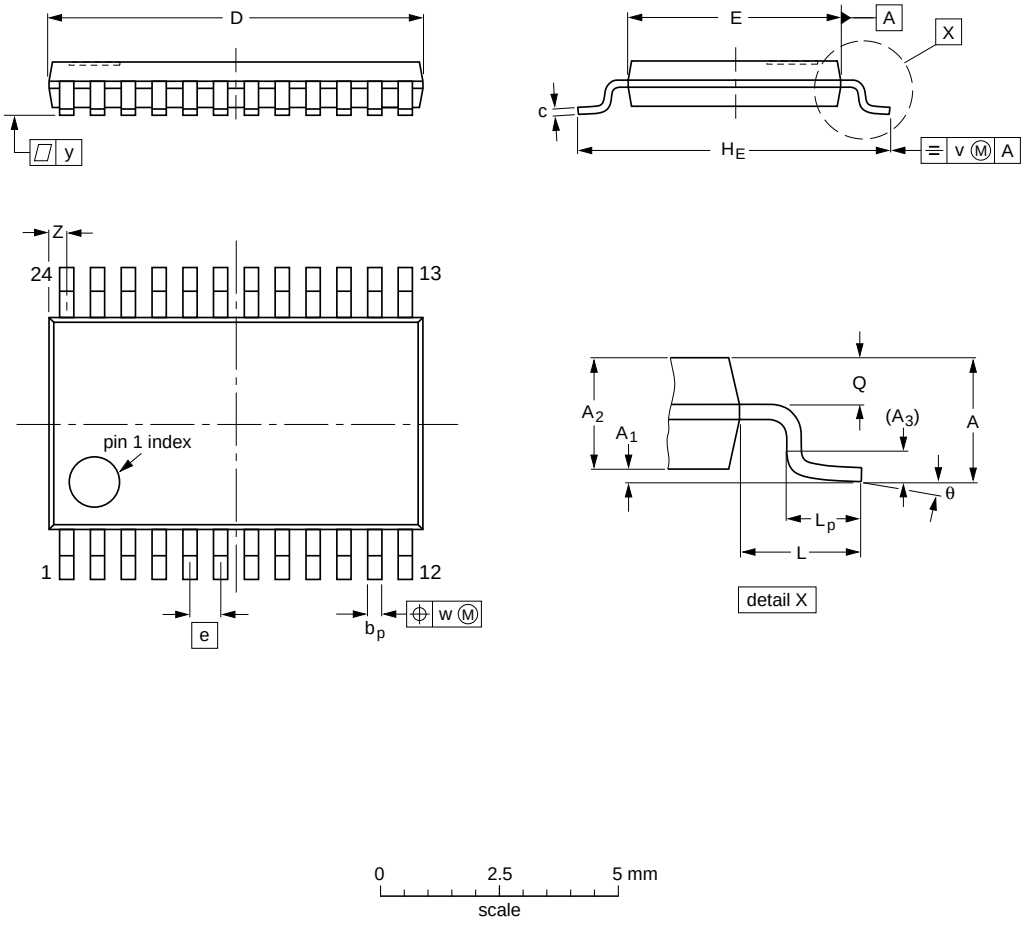
**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT340-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 20. Package outline SOT340-1 (SSOP24)**

**TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm** **SOT355-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 7.9<br>7.7 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | $8^o$<br>$0^o$ |

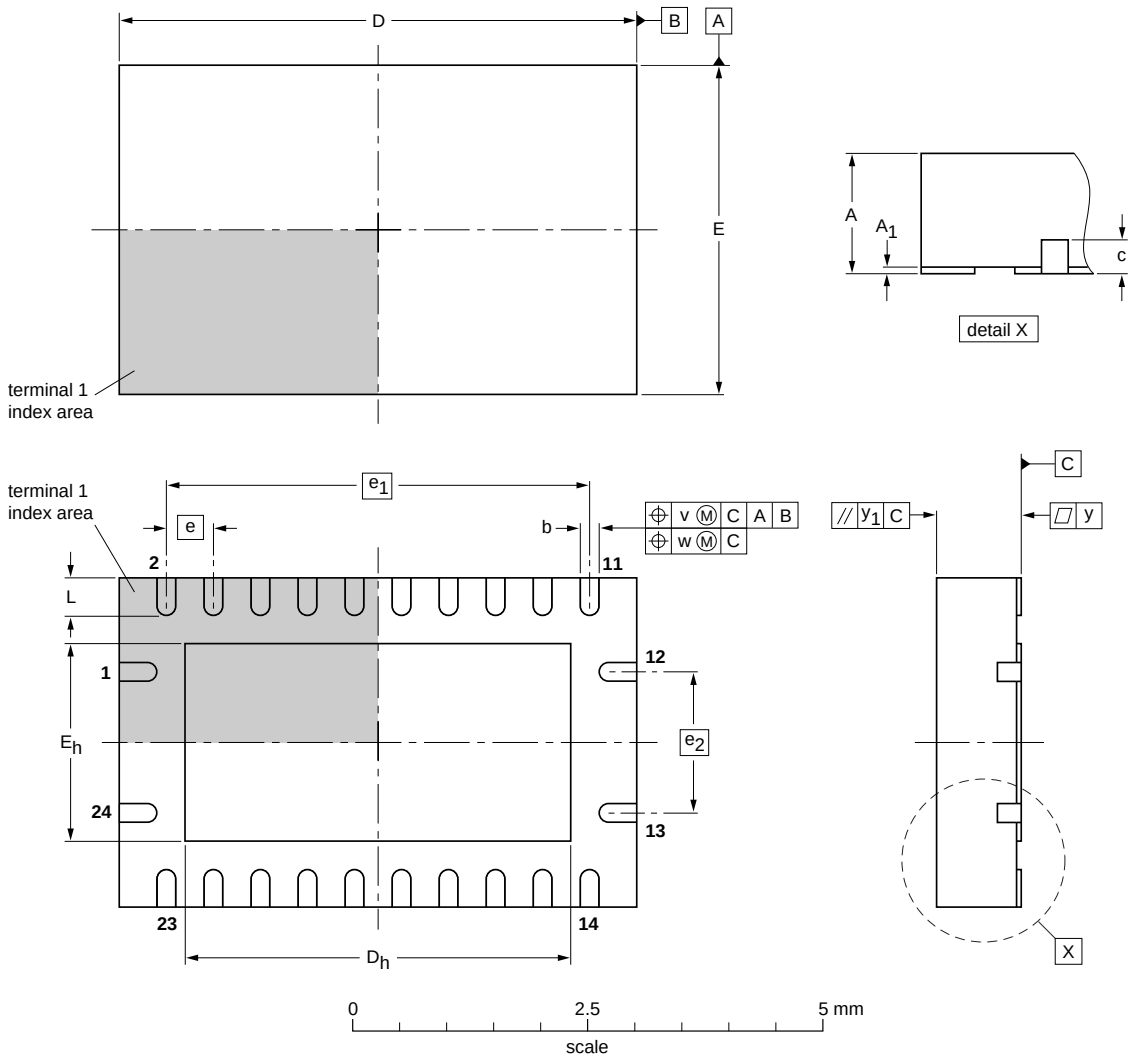
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT355-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 21. Package outline SOT355-1 (TSSOP24)**

**DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm** **SOT815-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 5.6<br>5.4 | 4.25<br>3.95 | 3.6<br>3.4 | 2.25<br>1.95 | 0.5 | 4.5 | 1.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT815-1 | - - - | - - - | - - - | | | 03-04-29 |

**Fig 22. Package outline SOT815-1 (DHVQFN24)**

## 15. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC_HCT4067 v.5 | 20111213 | Product data sheet | - | 74HC_HCT4067 v.4 |
| Modifications: | • Legal pages updated. | | | |
| 74HC_HCT4067 v.4 | 20110518 | Product data sheet | - | 74HC_HCT4067 v.3 |
| 74HC_HCT4067 v.3 | 20071015 | Product data sheet | - | 74HC_HCT4067_CNV v.2 |
| 74HC_HCT4067_CNV v.2 | 19970901 | Product specification | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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