74LV164-Q100

8-bit serial-in/parallel-out shift register

Rev. 1 — 26 June 2013 Product data sheet

1. General description

The 74LV164-Q100 is a low-voltage, Si-gate CMOS device and is pin and function compatible with the 74HC164-Q100 and 74HCT164-Q100.

The 74LV164-Q100 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB). Either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP). It enters Q0, which is the logical AND-function of the two data inputs (DSA and DSB). Data inputs DSA and DSB, existed one set-up time prior to the rising clock edge.

A LOW on the master reset input (MR) overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Gated serial data inputs
- Asynchronous master reset
- ESD protection:
  - MIL-STD-833, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV164D-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV164PW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV164BQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

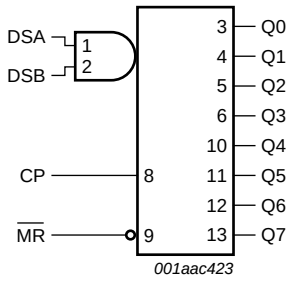


Fig 1. Logic symbol

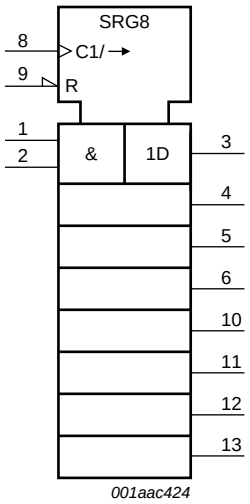


Fig 2. IEC logic symbol

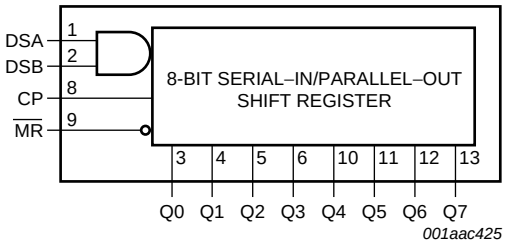


Fig 3. Functional diagram

5. Pinning information

5.1 Pinning

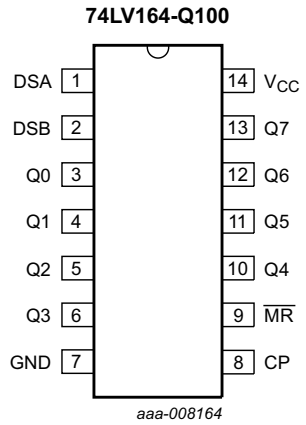
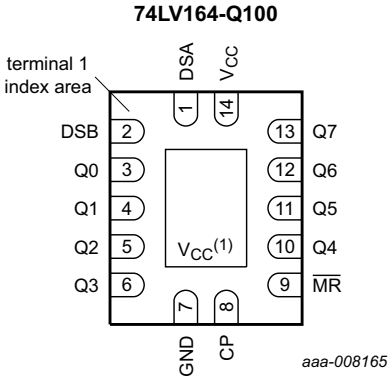


Fig 4. Pin configuration SO14 and TSSOP14



Transparent top view

(1) The die substrate is attached to the exposed die pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input SA
DSB	2	data input SB
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (edge triggered LOW-to-HIGH)
$\overline{MR}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH clock transition;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q = lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±50	mA
I_O	output current	output source or sink current, $V_O = 0.5$ V to $(V_{CC} + 0.5$ V)	[1]	-	±25	mA
I_{CC}	supply current			-	±50	mA
I_{GND}	ground current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = –40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
TSSOP14 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
DHVQFN14 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	5.5	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air		−40	-	+125	°C
t_r	rise time	input					
		V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V		-	-	50	ns/V
t_f	fall time	input					
		V_{CC} = 1.0 V to 2.0 V		-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V		-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V. LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.2 V	-	1.2	-	V
		I_O = −100 µA; V_{CC} = 2.0 V	1.8	2.0	-	V
		I_O = −100 µA; V_{CC} = 2.7 V	2.5	2.7	-	V
		I_O = −100 µA; V_{CC} = 3.0 V	2.8	3.0	-	V
		I_O = −6 mA; V_{CC} = 3.0 V	2.4	2.82	-	V
		I_O = −100 µA; V_{CC} = 4.5 V	4.3	4.5	-	V
		I_O = −12 mA; V_{CC} = 4.5 V	3.6	4.2	-	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	0	0.2	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	μA
I_{CC}	supply current	quiescent: $V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	μA
ΔI_{CC}	additional supply current	quiescent, per input: $V_I = V_{CC} - 0.6$ V; V_{CC} = 2.7 V to 3.6 V	-	-	500	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 μA; V_{CC} = 1.2 V	-	-	-	V
		I_O = –100 μA; V_{CC} = 2.0 V	1.8	-	-	V
		I_O = –100 μA; V_{CC} = 2.7 V	2.5	-	-	V
		I_O = –100 μA; V_{CC} = 3.0 V	2.8	-	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.2	-	-	V
		I_O = –100 μA; V_{CC} = 4.5 V	4.3	-	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.5	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.2 V	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	-	0.5	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	-	0.2	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	-	0.65	V

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	μA
I_{CC}	supply current	quiescent: $V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	μA
ΔI_{CC}	additional supply current	quiescent, per input: $V_I = V_{CC} - 0.6$ V; V_{CC} = 2.7 V to 3.6 V	-	-	850	μA

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; R_L = 1 kΩ; for test circuit, see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{pd}	propagation delay	CP - see Figure 6; $\overline{MR}$ - see Figure 7	[2]				
		V_{CC} = 1.2 V		-	75	-	ns
		V_{CC} = 2.0 V		-	26	39	ns
		V_{CC} = 2.7 V		-	19	29	ns
		V_{CC} = 3.0 V to 3.6 V		-	14	23	ns
		V_{CC} = 4.5 V to 5.5 V		-	12	19	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[3]	-	12	-	ns
t_W	pulse width	CP - see Figure 6					
		V_{CC} = 2.0 V		34	9	-	ns
		V_{CC} = 2.7 V		25	6	-	ns
		V_{CC} = 3.0 V to 3.6 V		20	5	-	ns
		V_{CC} = 4.5 V to 5.5 V		13	4	-	ns
		$\overline{MR}$ - see Figure 7					
		V_{CC} = 2.0 V		34	10	-	ns
		V_{CC} = 2.7 V		25	8	-	ns
		V_{CC} = 3.0 V to 3.6 V		20	6	-	ns
		V_{CC} = 4.5 V to 5.5 V		13	5	-	ns
t_{rem}	removal time	$\overline{MR}$ to CP - see Figure 7					
		V_{CC} = 1.2 V		-	30	-	ns
		V_{CC} = 2.0 V		19	10	-	ns
		V_{CC} = 2.7 V		14	8	-	ns
		V_{CC} = 3.0 V to 3.6 V		11	6	-	ns
		V_{CC} = 4.5 V to 5.5 V		8	5	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; R_L = 1 kΩ; for test circuit, see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{su}	set-up time	Dn to CP - see Figure 8					
		V_{CC} = 1.2 V		-	15	-	ns
		V_{CC} = 2.0 V		22	5	-	ns
		V_{CC} = 2.7 V		16	4	-	ns
		V_{CC} = 3.0 V to 3.6 V		13	3	-	ns
		V_{CC} = 4.5 V to 5.5 V		9	2	-	ns
t_h	hold time	Dn to CP - see Figure 8					
		V_{CC} = 1.2 V		-	–10	-	ns
		V_{CC} = 2.0 V		5	–3	-	ns
		V_{CC} = 2.7 V		5	–2	-	ns
		V_{CC} = 3.0 V to 3.6 V		5	–2	-	ns
		V_{CC} = 4.5 V to 5.5 V		5	–1	-	ns
f_{max}	maximum frequency	see Figure 6					
		V_{CC} = 2.0 V		14	40	-	MHz
		V_{CC} = 2.7 V		19	58	-	MHz
		V_{CC} = 3.0 V to 3.6 V		24	70	-	MHz
		V_{CC} = 4.5 V to 5.5 V		36	100	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF		-	78	-	MHz
C_{PD}	power dissipation capacitance	per gate: V_{CC} = 3.3 V	[4][5]	-	40	-	pF
T_{amb} = –40 °C to +125 °C							
t_{pd}	propagation delay	CP - see Figure 6: $\overline{MR}$ - see Figure 7	[2]				
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	49	ns
		V_{CC} = 2.7 V		-	-	36	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	29	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	24	ns
t_W	pulse width	CP - see Figure 6: $\overline{MR}$ - see Figure 7					
		V_{CC} = 2.0 V		41	-	-	ns
		V_{CC} = 2.7 V		30	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		24	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		16	-	-	ns
t_{rem}	removal time	$\overline{MR}$ to CP - see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		24	-	-	ns
		V_{CC} = 2.7 V		18	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		14	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		10	-	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; R_L = 1 kΩ; for test circuit, see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time	Dn to CP - see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	26	-	-	ns
		V_{CC} = 2.7 V	19	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	15	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	10	-	-	ns
t_h	hold time	Dn to CP - see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 2.7 V	5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5	-	-	ns
f_{max}	maximum frequency	see Figure 6				
		V_{CC} = 2.0 V	12	-	-	MHz
		V_{CC} = 2.7 V	16	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	20	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	30	-	-	MHz

[1] Typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

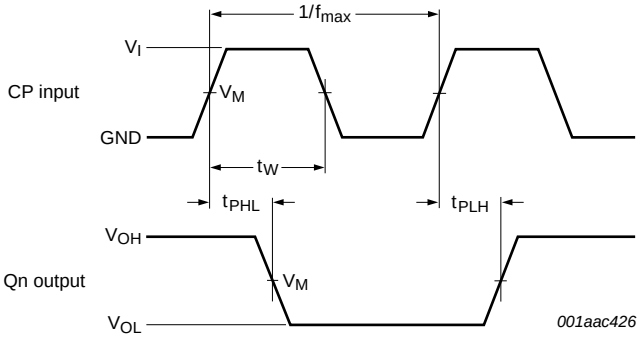
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

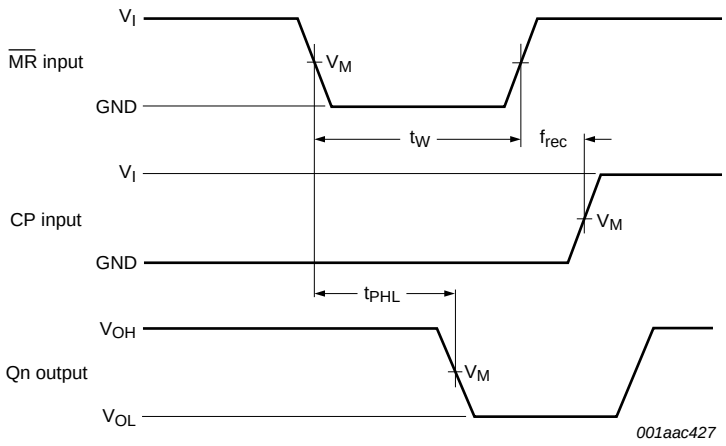
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

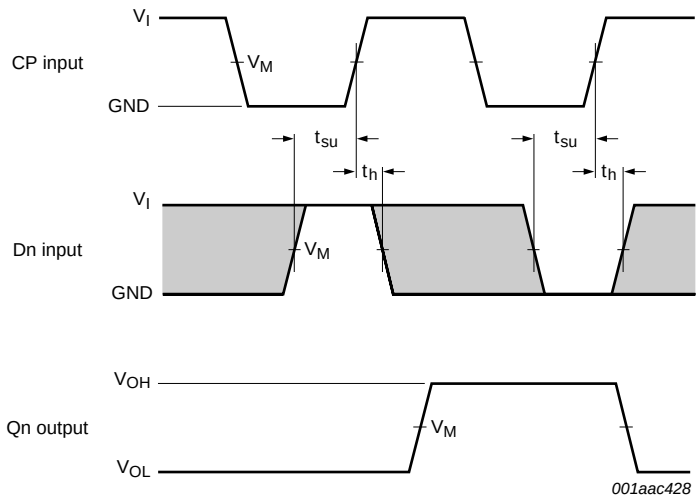
Fig 6. Propagation delay clock (CP) to output (Qn), clock pulse width and maximum clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Pulse width master reset ($\overline{MR}$), propagation delay master reset ($\overline{MR}$) to output (Qn) and removal time master reset ($\overline{MR}$) to clock (CP)



Measurement points are given in Table 8.

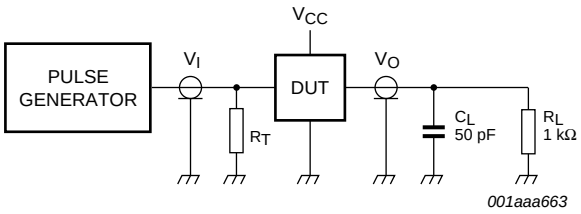
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 8. Data set-up and hold times inputs (Dn) to clock (CP)

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.0 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

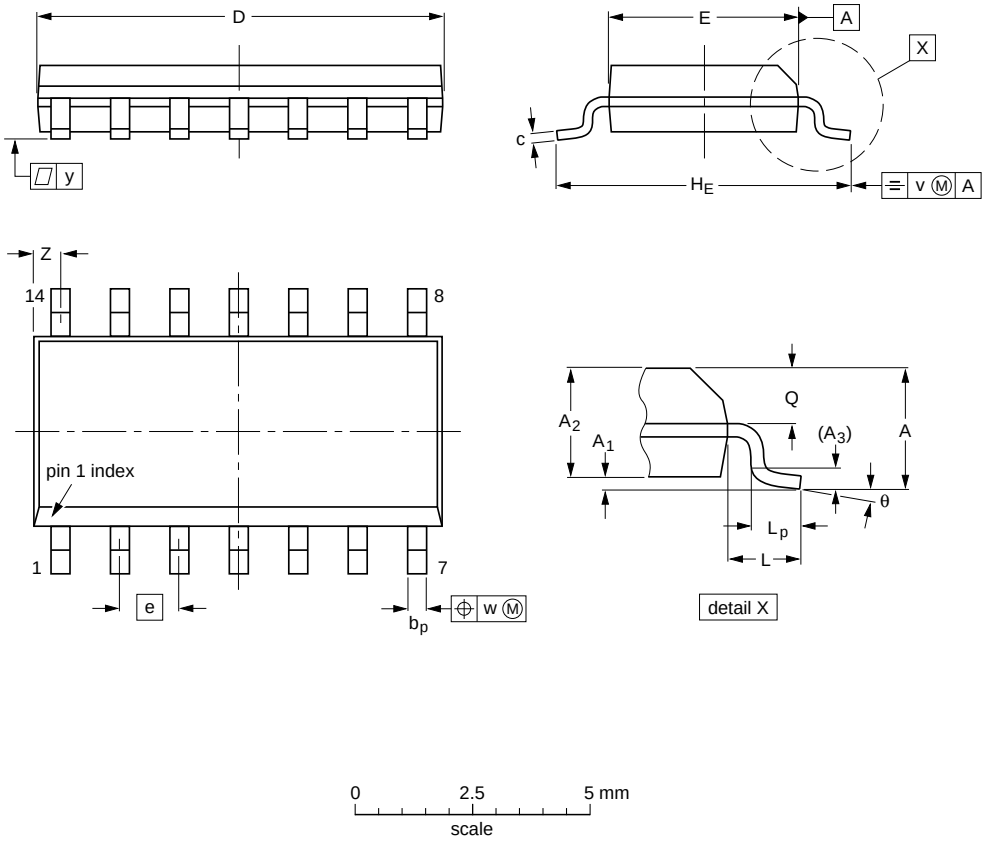
Fig 9. Load circuitry for switching times

Table 9. Test data

Supply voltage	Input		Load		Test
V_{CC}	V_I	t_r, t_f	C_L	R_L	
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.0 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF, 15 pF	1 kΩ	t_{PHL}, t_{PLH}
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

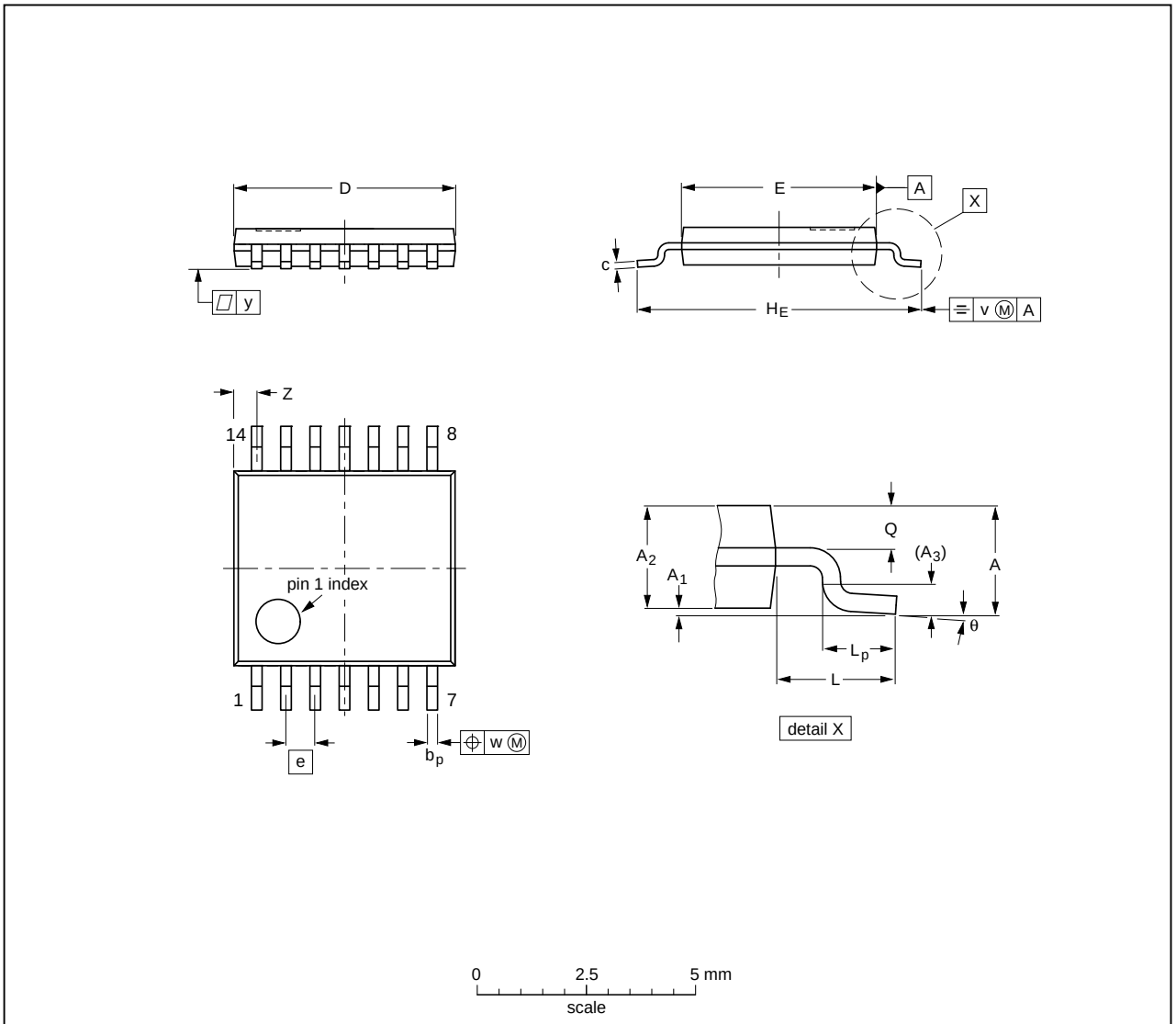
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

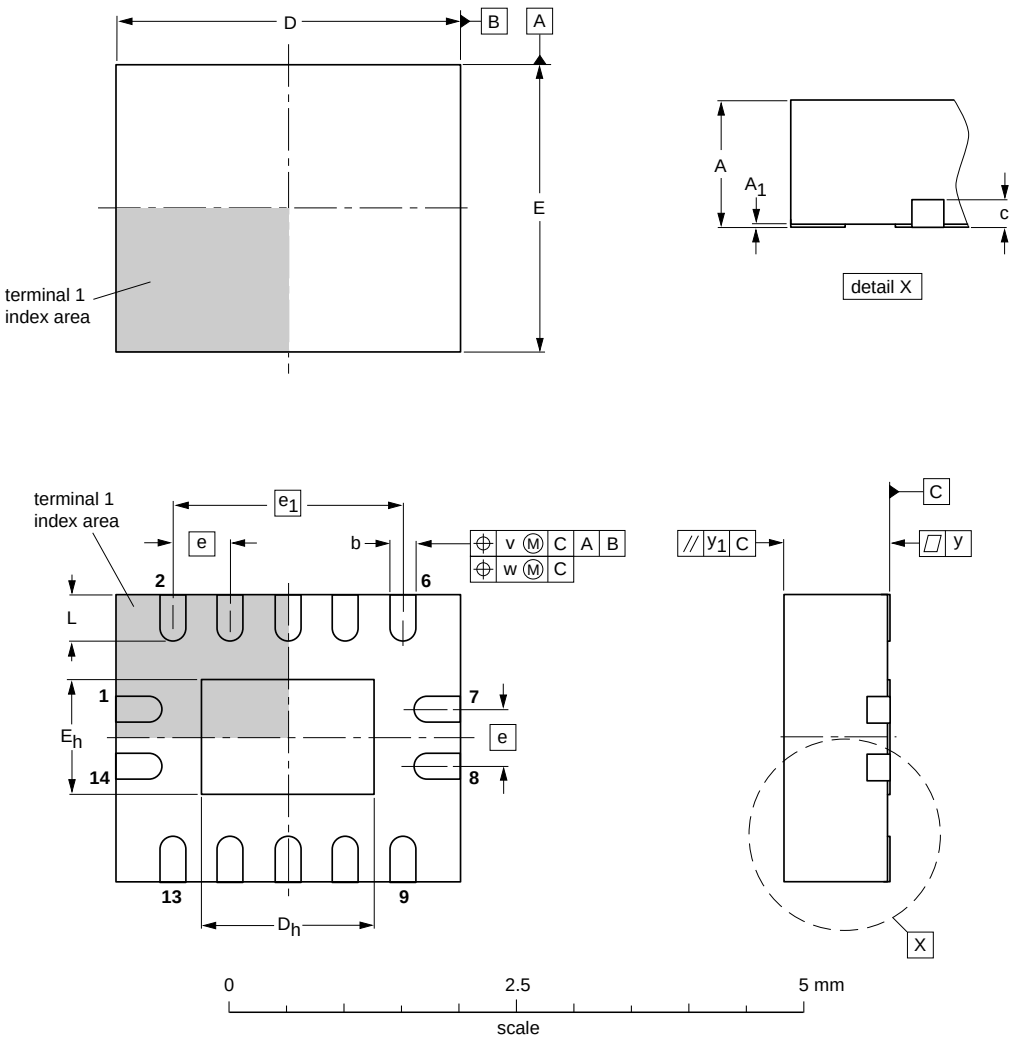
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 12. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
MIL	Military

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV164_Q100 v.1	20130626	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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