

74LVC16245A; 74LVCH16245A

16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Rev. 12 — 13 February 2012

Product data sheet

1. General description

The 74LVC16245A; 74LVCH16245A are 16-bit transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features two output enable ($\overline{\text{nOE}}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $\overline{\text{nOE}}$ controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH16245A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when $V_{CC} = 0$ V
- All data inputs have bus hold (74LVCH16245A only)
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C



3. Ordering information

Table 1. Ordering information

| Type number | Temperature range | Package | | |
|-----------------------------------|-------------------|---------|---|-----------|
| | | Name | Description | Version |
| 74LVC16245ADL 74LVCH16245ADL | -40 °C to +125 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |
| 74LVC16245ADGG 74LVCH16245ADGG | -40 °C to +125 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74LVC16245AEV 74LVCH16245AEV | -40 °C to +125 °C | VFBGA56 | plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm | SOT702-1 |
| 74LVC16245ABX 74LVCH16245ABX | -40 °C to +125 °C | HXQFN60 | plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body 4 × 6 × 0.5 mm | SOT1134-2 |

4. Functional diagram

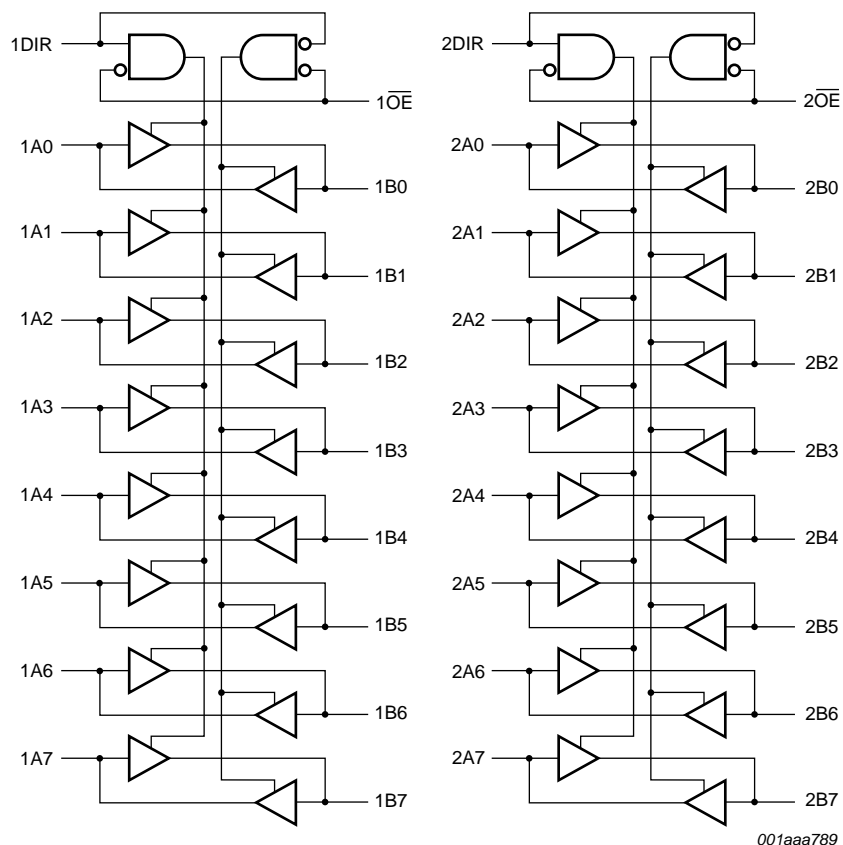


Fig 1. Logic symbol

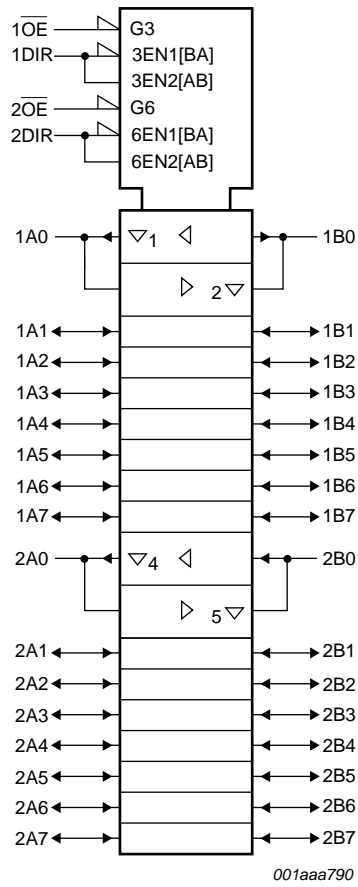


Fig 2. IEC logic symbol

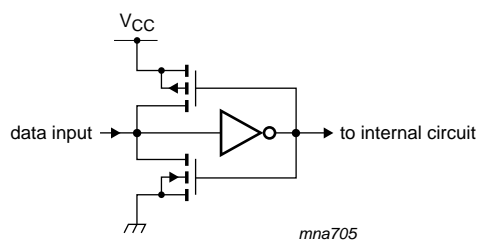
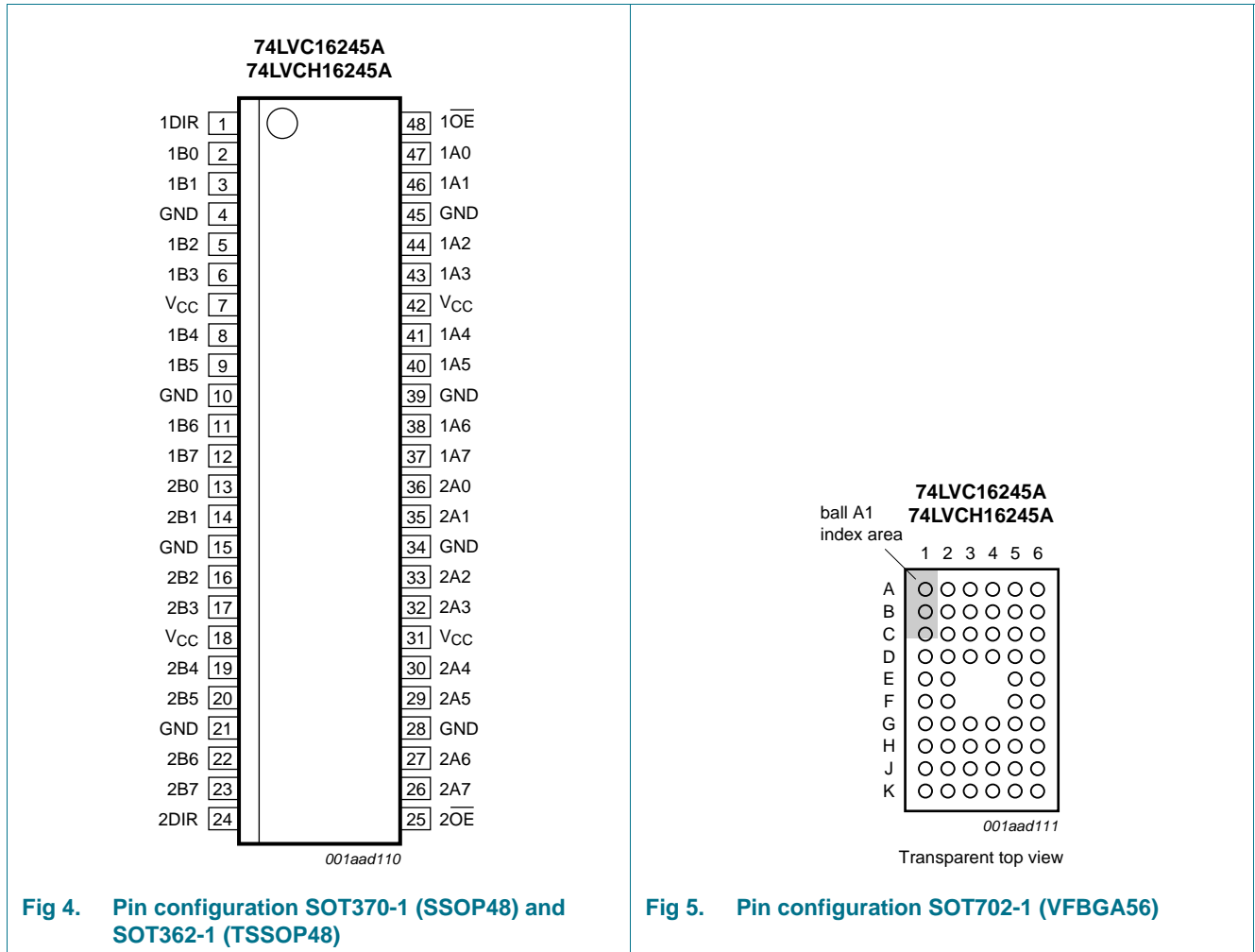
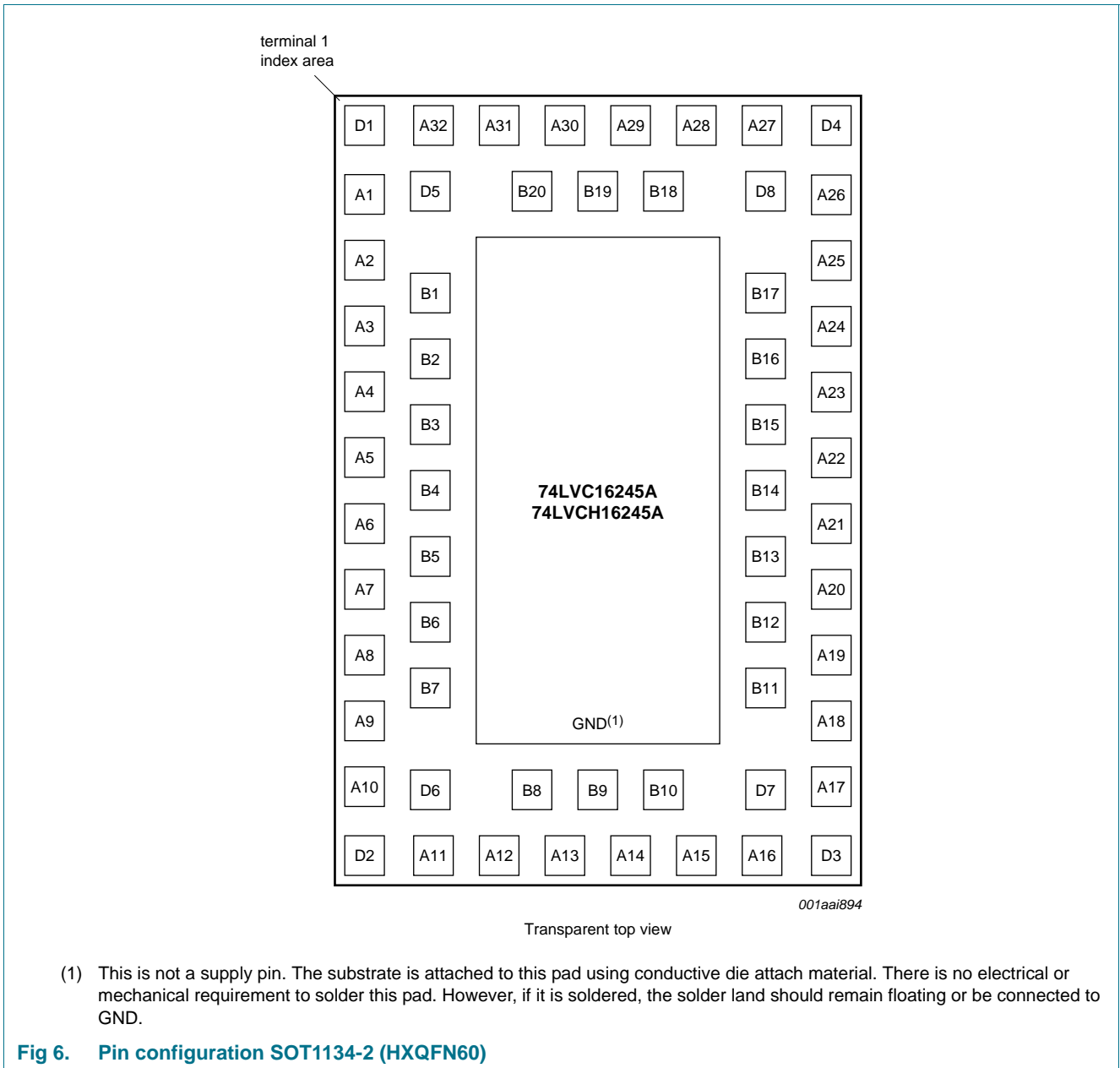


Fig 3. Bus hold circuit

5. Pinning information

5.1 Pinning





5.2 Pin description

Table 2. Pin description

| Symbol | Pin | | | Description |
|-------------------------------------|--------------------------------|--------------------------------|--|----------------------------------|
| | SOT370-1 and SOT362-1 | SOT702-1 | SOT1134-2 | |
| 1DIR, 2DIR | 1, 24 | A1, K1 | A30, A13 | direction control input |
| 1B0 to 1B7 | 2, 3, 5, 6, 8, 9, 11, 12 | B2, B1, C2, C1, D2, D1, E2, E1 | B20, A31, D5, D1, A2, B2, B3, A5 | data input/output |
| 2B0 to 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | F1, F2, G1, G2, H1, H2, J1, J2 | A6, B5, B6, A9, D2, D6, A12, B8 | data input/output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | B3, B4, D3, D4, G3, G4, J3, J4 | A32, A3, A8, A11, A16, A19, A24, A27 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | C3, C4, H3, H4 | A1, A10, A17, A26 | supply voltage |
| $\overline{1OE}$, $\overline{2OE}$ | 48, 25 | A6, K6 | A29, A14 | output enable input (active LOW) |
| 1A0 to 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | B5, B6, C5, C6, D5, D6, E5, E6 | B18, A28, D8, D4, A25, B16, B15, A22 | data input/output |
| 2A0 to 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | F6, F5, G6, G5, H6, H5, J6, J5 | A21, B13, B12, A18, D3, D7, A15, B10 | data input/output |
| n.c. | - | A2, A3, A4, A5, K2, K3, K4, K5 | A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19 | not connected |

6. Functional description

Table 3. Function table^[1]

| Inputs | | Outputs | |
|--------|------|-----------|-----------|
| nOE | nDIR | nAn | nBn |
| L | L | nAn = nBn | inputs |
| L | H | inputs | nBn = nAn |
| H | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--------------------------------|----------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ±50 | mA |
| V_O | output voltage | output HIGH or LOW | [2] -0.5 | $V_{CC} + 0.5$ | V |
| | | output 3-state | [2] -0.5 | +6.5 | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ±50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C; | | | |
| | | (T)SSOP48 package | [3] - | 500 | mW |
| | | VFBGA56 package | [4] - | 1000 | mW |
| | | HXQFN60 package | [4] - | 1000 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

[4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---------------------------|------|-----|----------|------|
| V_{CC} | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | 3.6 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | output HIGH or LOW | 0 | - | V_{CC} | V |
| | | output 3-state | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.2$ V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 0 | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|--|---|------------------------|--------------------|------------------------|------------------------|------------------------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | 0.65 × V _{CC} | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V | V _{CC} - 0.2 | - | - | V _{CC} - 0.3 | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | I _O = -18 mA; V _{CC} = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| | | I _O = -24 mA; V _{CC} = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| I _I | input leakage current ^[2] | V _I = 5.5 V or GND; V _{CC} = 3.6 V | - | ±0.1 | ±5 | - | ±20 | μA |
| I _{OZ} | OFF-state output current ^{[2][3]} | V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V | - | ±0.1 | ±5 | - | ±20 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 5.5 V; V _{CC} = 0.0 V | - | ±0.1 | ±10 | - | ±20 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V | - | 0.1 | 20 | - | 80 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.7 V to 3.6 V | - | 5 | 500 | - | 5000 | μA |
| C _I | input capacitance | V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC} | - | 5.0 | - | - | - | pF |
| C _{I/O} | input/output capacitance | V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC} | - | 10 | - | - | - | pF |

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-------------------|---|---|------------------|--------------------|-----|-------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| I _{BHL} | bus hold LOW current ^{[4][5]} | V _{CC} = 1.65; V _I = 0.58 V | 10 | - | - | 10 | - | μA |
| | | V _{CC} = 2.3; V _I = 0.7 V | 30 | - | - | 25 | - | μA |
| | | V _{CC} = 3.0; V _I = 0.8 V | 75 | - | - | 60 | - | μA |
| I _{BHH} | bus hold HIGH current ^{[4][5]} | V _{CC} = 1.65; V _I = 1.07 V | -10 | - | - | -10 | - | μA |
| | | V _{CC} = 2.3; V _I = 1.7 V | -30 | - | - | -25 | - | μA |
| | | V _{CC} = 3.0; V _I = 2.0 V | -75 | - | - | -60 | - | μA |
| I _{BHLO} | bus hold LOW overdrive current ^{[4][6]} | V _{CC} = 1.95 V | 200 | - | - | 200 | - | μA |
| | | V _{CC} = 2.7 V | 300 | - | - | 300 | - | μA |
| | | V _{CC} = 3.6 V | 500 | - | - | 500 | - | μA |
| I _{BHHO} | bus hold HIGH overdrive current ^{[4][6]} | V _{CC} = 1.95 V | -200 | - | - | -200 | - | μA |
| | | V _{CC} = 2.7 V | -300 | - | - | -300 | - | μA |
| | | V _{CC} = 3.6 V | -500 | - | - | -500 | - | μA |

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input terminal.

[3] For I/O ports the parameter I_{OZ} includes the input leakage current.

[4] Valid for data inputs of bus hold parts only (74LVCH16245A). Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V_I level.

[6] The specified overdrive current at the data input forces the data input to the opposite input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------|---|------------------|--------------------|------|-------------------|------|------|
| | | | Min | Typ ^[2] | Max | Min | Max | |
| t _{pd} | propagation delay | nAn to nBn; nBn to nAn; see Figure 7 ^[1] | | | | | | |
| | | V _{CC} = 1.2 V | - | 13.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 5.2 | 12.2 | 1.5 | 13.8 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.8 | 6.0 | 1.0 | 6.7 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 2.7 | 4.7 | 1.0 | 6.0 | ns |
| t _{en} | enable time | nOE to nAn, nBn; see Figure 8 ^[1] | | | | | | |
| | | V _{CC} = 1.2 V | - | 15.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 5.9 | 15.0 | 1.5 | 16.9 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.3 | 7.9 | 1.0 | 8.8 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 3.5 | 6.7 | 1.5 | 8.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.7 | 5.5 | 1.0 | 7.0 | ns |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|------------------|--------------------|------|-------------------|------|------|
| | | | Min | Typ ^[2] | Max | Min | Max | |
| t _{dis} | disable time | nOE to nAn, nBn; see Figure 8 ^[1] | | | | | | |
| | | V _{CC} = 1.2 V | - | 11.0 | - | - | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 4.9 | 13.1 | 1.0 | 14.7 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 2.7 | 7.1 | 0.5 | 7.9 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 3.4 | 6.6 | 1.5 | 8.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.3 | 5.6 | 1.5 | 7.0 | ns |
| C _{PD} | power dissipation capacitance | per input; V _I = GND to V _{CC} ^[3] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | - | 11.5 | - | - | - | pF |
| | | V _{CC} = 2.3 V to 2.7 V | - | 15.2 | - | - | - | pF |
| | | V _{CC} = 3.0 V to 3.6 V | - | 18.5 | - | - | - | pF |

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

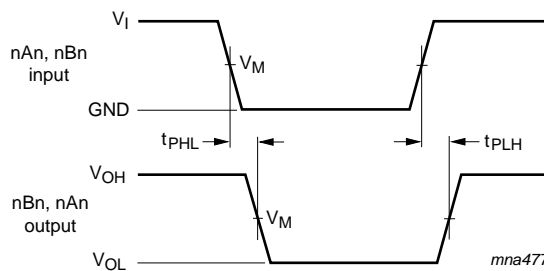
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

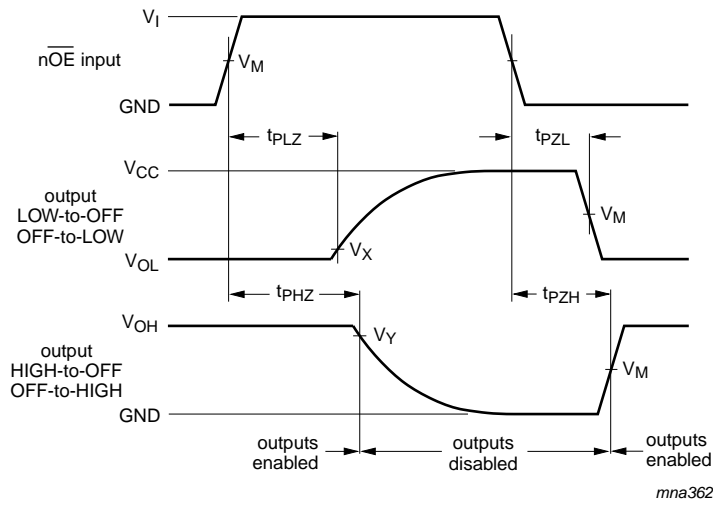
11. Waveforms



Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The input (nAn, nBn) to output (nBn, nAn) propagation delays



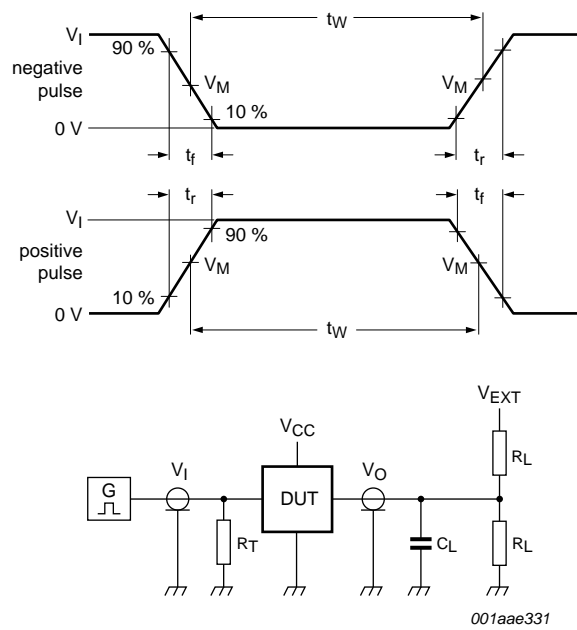
Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. 3-state enable and disable times

Table 8. Measurement points

| Supply voltage | V_M | Input | | | |
|------------------|---------------------|----------|---------------|-------------------|-------------------|
| | | V_I | $t_r = t_f$ | V_X | V_Y |
| 1.2 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 2.7 V | 1.5 V | 2.7 V | ≤ 2.5 ns | $V_{OL} + 0.3$ V | $V_{OH} - 0.3$ V |
| 3.0 V to 3.6 V | 1.5 V | 2.7 V | ≤ 2.5 ns | $V_{OL} + 0.3$ V | $V_{OH} - 0.3$ V |



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|------------------|----------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PLZ}, t_{PZL} | t_{PHZ}, t_{PZH} |
| 1.2 V | V_{CC} | ≤ 2 ns | 30 pF | 1 k Ω | open | $2 \times V_{CC}$ | GND |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2 ns | 30 pF | 1 k Ω | open | $2 \times V_{CC}$ | GND |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

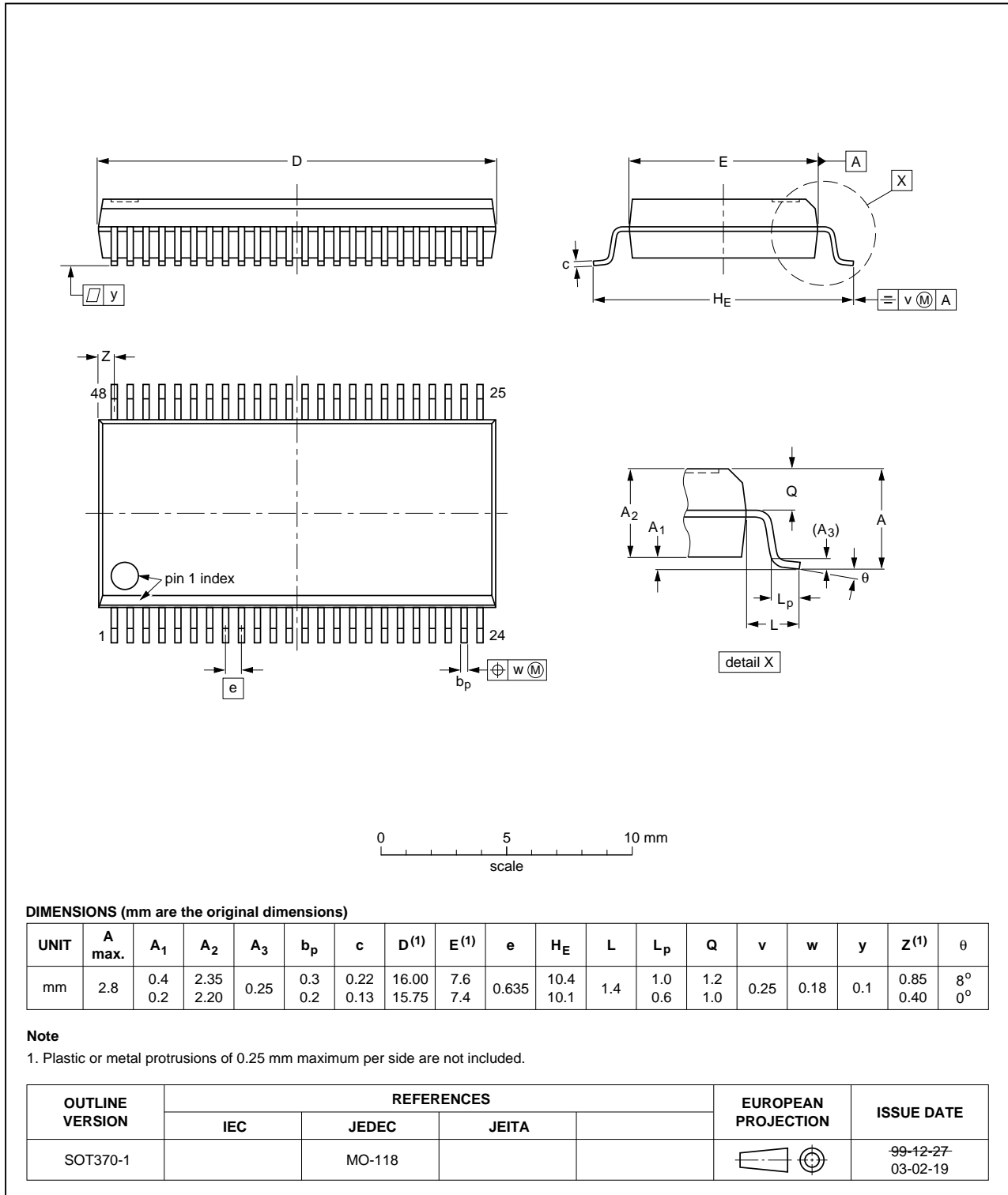


Fig 10. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

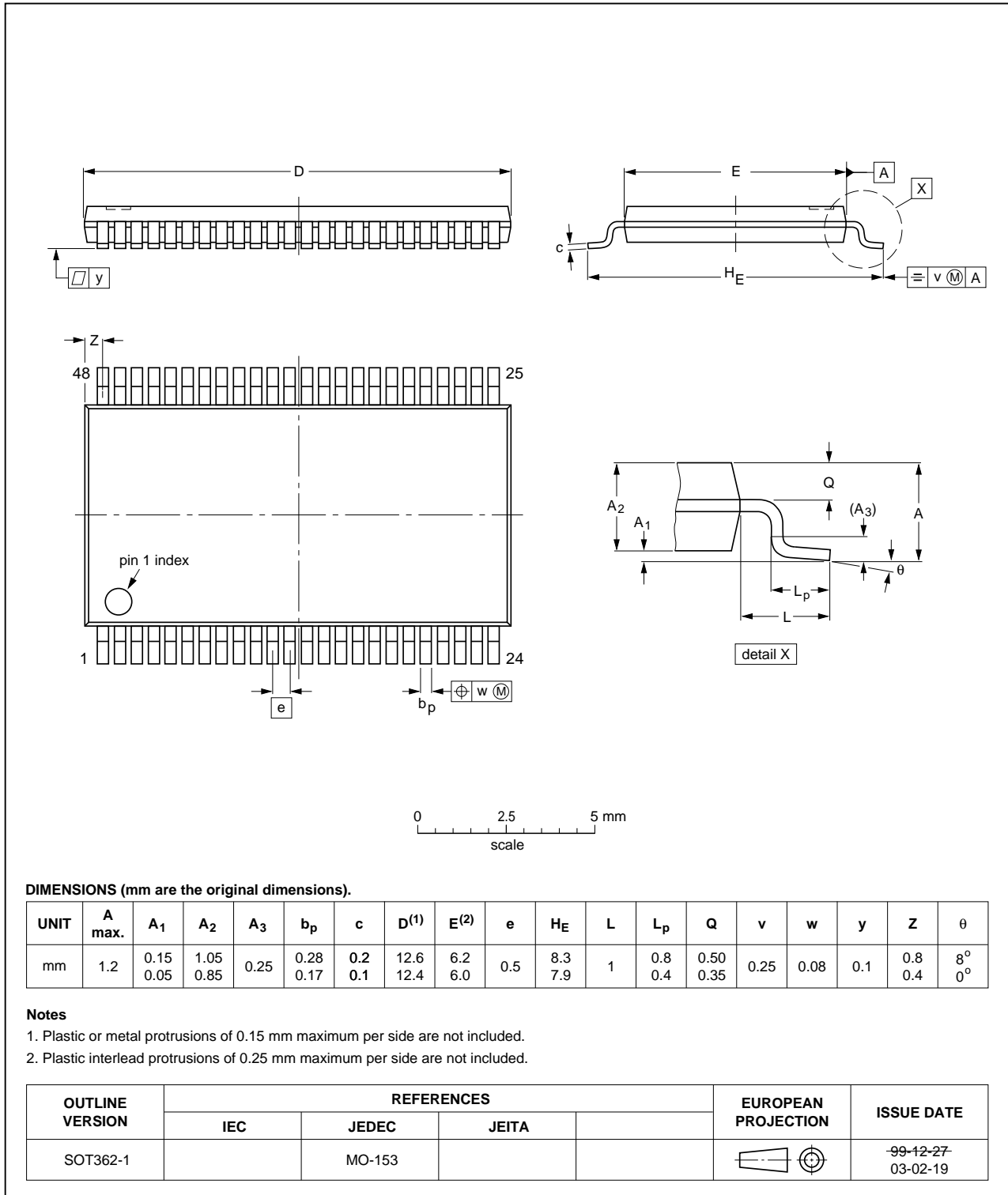


Fig 11. Package outline SOT362-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1

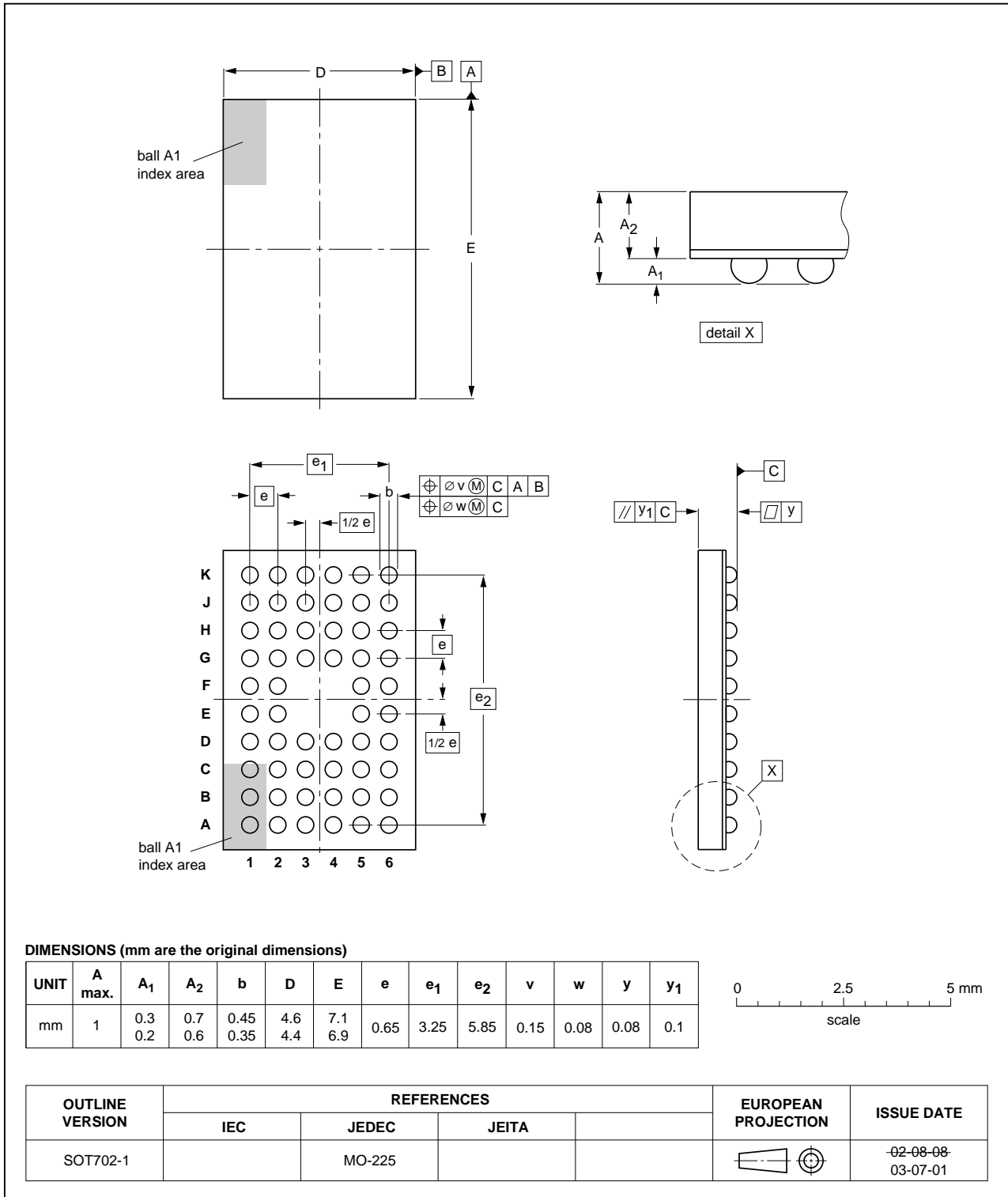


Fig 12. Package outline SOT702-1 (VFBGA56)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|-----------------------------|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------------------|---|-----------------------|---------------|----------------------------------|
| 74LVC_LVCH16245A v.12 | 20120213 | Product data sheet | - | 74LVC_LVCH16245A v.11 |
| Modifications: | <ul style="list-style-type: none"> For type number 74LVC16245ABX and 74LVCH16245ABX the sot code has changed to SOT1134-2. | | | |
| 74LVC_LVCH16245A v.11 | 20111208 | Product data sheet | - | 74LVC_LVCH16245A v.10 |
| Modifications: | <ul style="list-style-type: none"> Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges. | | | |
| 74LVC_LVCH16245A v.10 | 20110623 | Product data sheet | - | 74LVC_LVCH16245A v.9 |
| Modifications: | <ul style="list-style-type: none"> type numbers 74LVC16245ABQ and 74LVCH16245ABQ changed to 74LVC16245ABX and 74LVCH16245ABX. Figure 6: figure note 1 changed. | | | |
| 74LVC_LVCH16245A v.9 | 20100329 | Product data sheet | - | 74LVC_LVCH16245A v.8 |
| 74LVC_LVCH16245A v.8 | 20081106 | Product data sheet | - | 74LVC_LVCH16245A v.7 |
| 74LVC_LVCH16245A v.7 | 20031125 | Product specification | - | 74LVC_LVCH16245A v.6 |
| 74LVC_LVCH16245A v.6 | 20030130 | Product specification | - | 74LVC_LVCH16245A v.5 |
| 74LVC_LVCH16245A v.5 | 20021030 | Product specification | - | 74LVC_H16245A v.4 |
| 74LVC_H16245A v.4 | 19970925 | Product specification | - | 74LVC16245A_ 74LVCH16245A v.3 |
| 74LVC16245A_ 74LVCH16245A v.3 | 19970925 | Product specification | - | 74LVC16245A v.2 |
| 74LVC16245A v.2 | 19970801 | Product specification | - | 74LVC16245A v.1 |
| 74LVC16245A v.1 | - | - | - | - |

15. Legal information

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|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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