

# 74LVC04A

## Hex inverter

Rev. 9 — 17 November 2011

Product data sheet

## 1. General description

The 74LVC04A provides six inverting buffers. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

## 2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

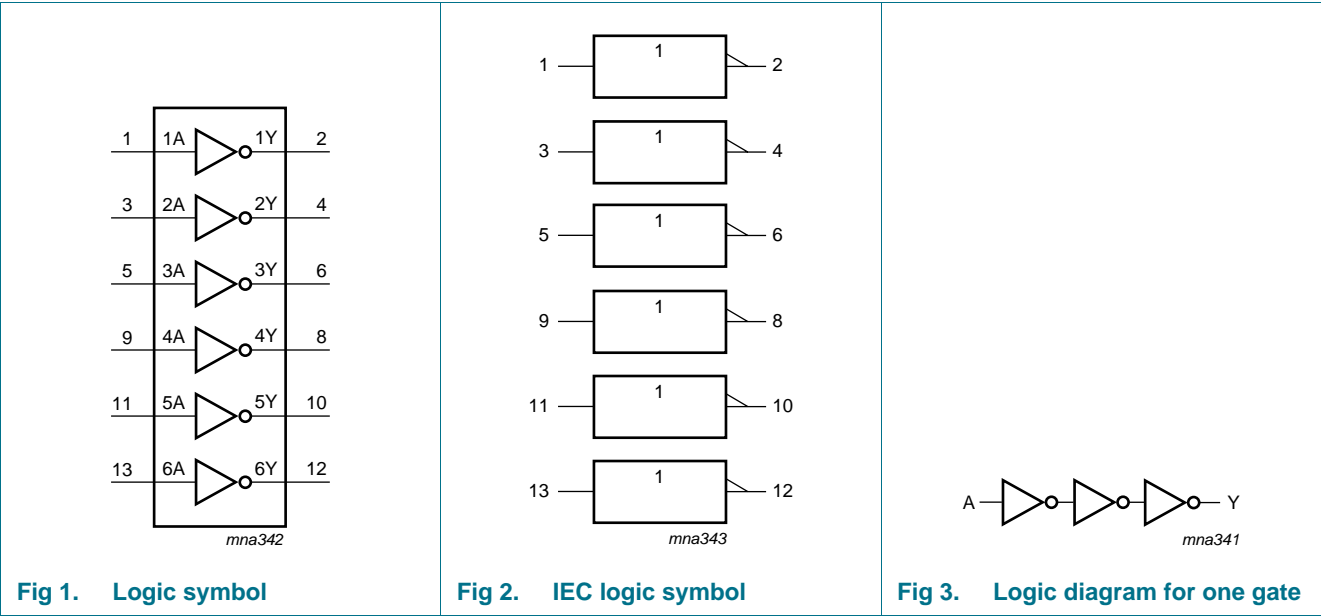
## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC04AD	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC04ADB	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC04APW	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	TSSOP14	plastic thin shrink outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC04ABQ	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

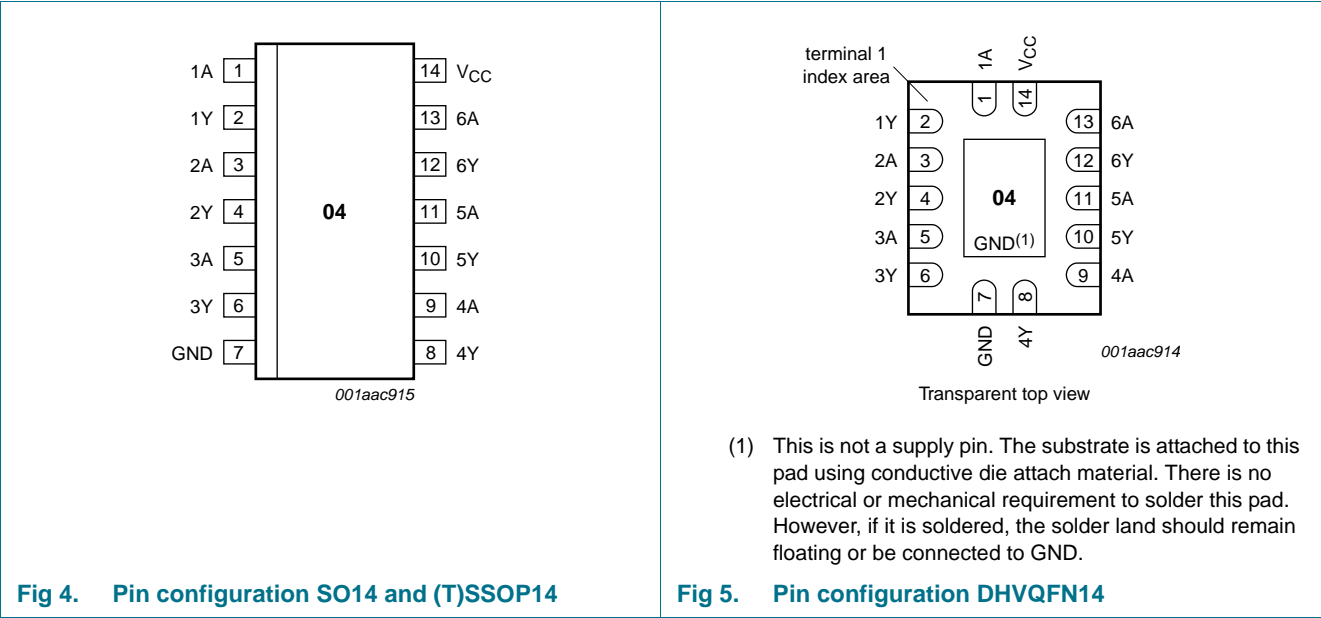


4. Functional diagram



5. Pinning information

5.1 Pinning



## 5.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level

## 7. Limiting values

**Table 4.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0	-50	-	mA
V <sub>I</sub>	input voltage		<sup>[1]</sup> -0.5	+6.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage		<sup>[2]</sup> -0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	<sup>[3]</sup> -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±20	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	4.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	14	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.3	3.7	8.8	0.3	10.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.2	5.0	0.5	5.8	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.1	5.5	1.0	7.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.0	4.5	1.0	6.0	ns
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	3.9	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	7.1	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	9.9	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

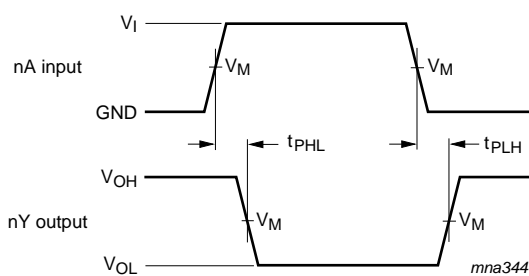
[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHzC<sub>L</sub> = output load capacitance in pFV<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

## 11. Waveforms

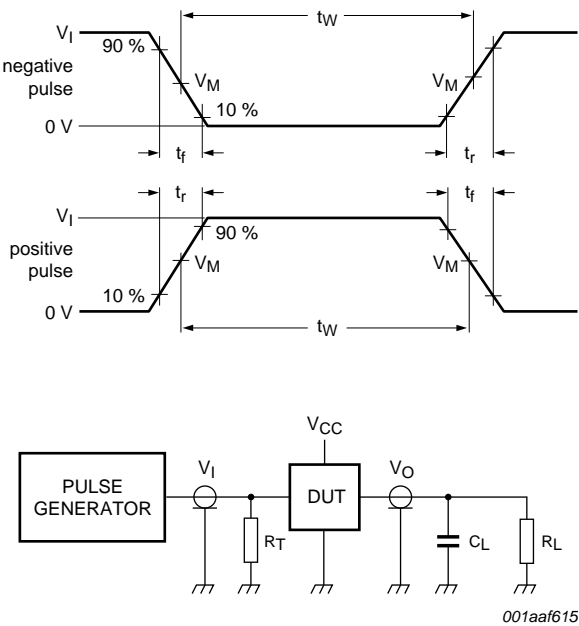


$V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. The input (nA) to output (nY) propagation delays**



Test data is given in [Table 8](#).  
Definitions for test circuit:  
 $R_L$  = Load resistance  
 $C_L$  = Load capacitance including jig and probe capacitance  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 7. Load circuitry for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
	$V_I$	$t_r, t_f$	$C_L$	$R_L$
1.2 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	1 k $\Omega$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2 \text{ ns}$	30 pF	500 $\Omega$
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

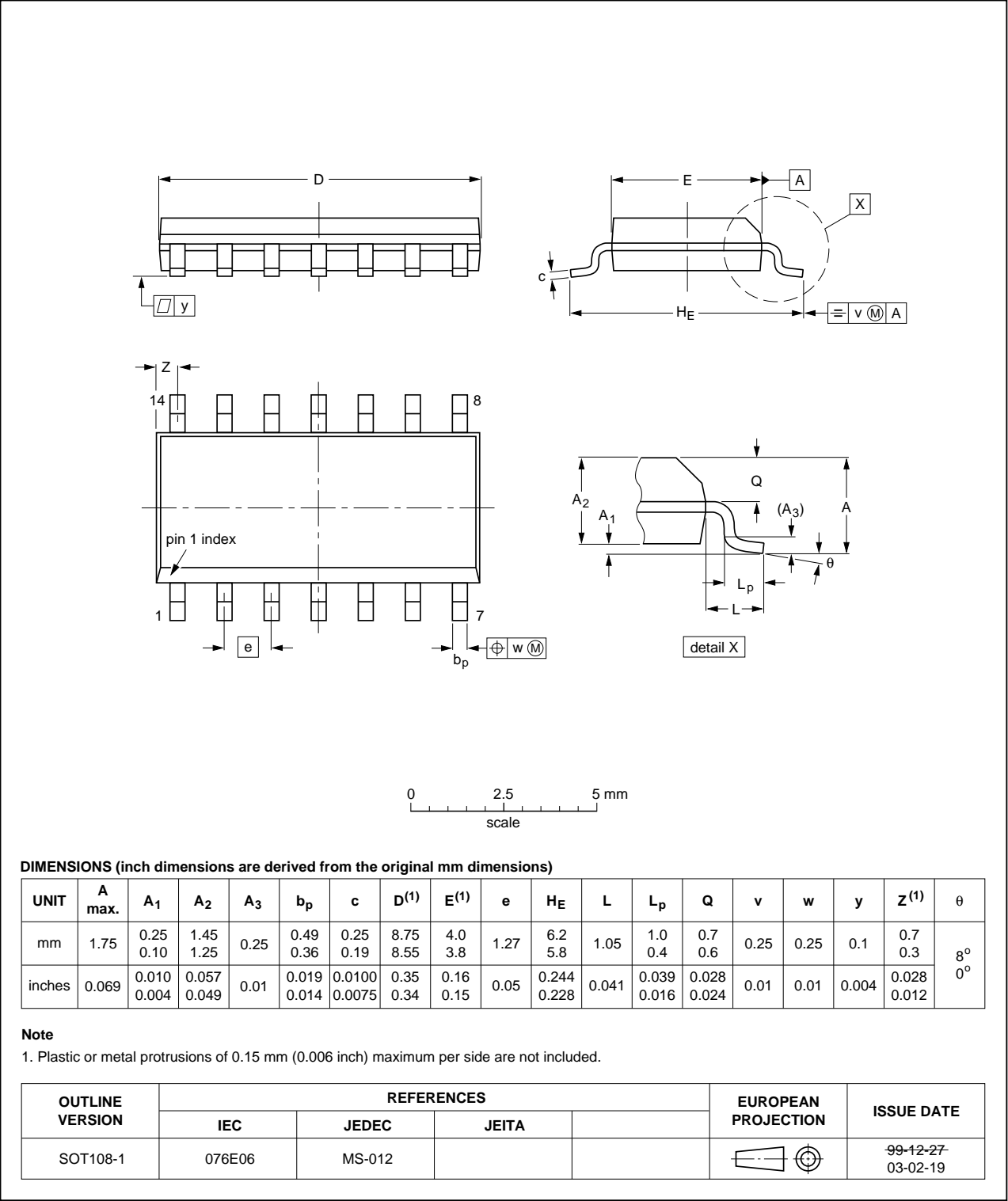


Fig 8. Package outline SOT108-1 (SO14)



SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm
SOT337-1

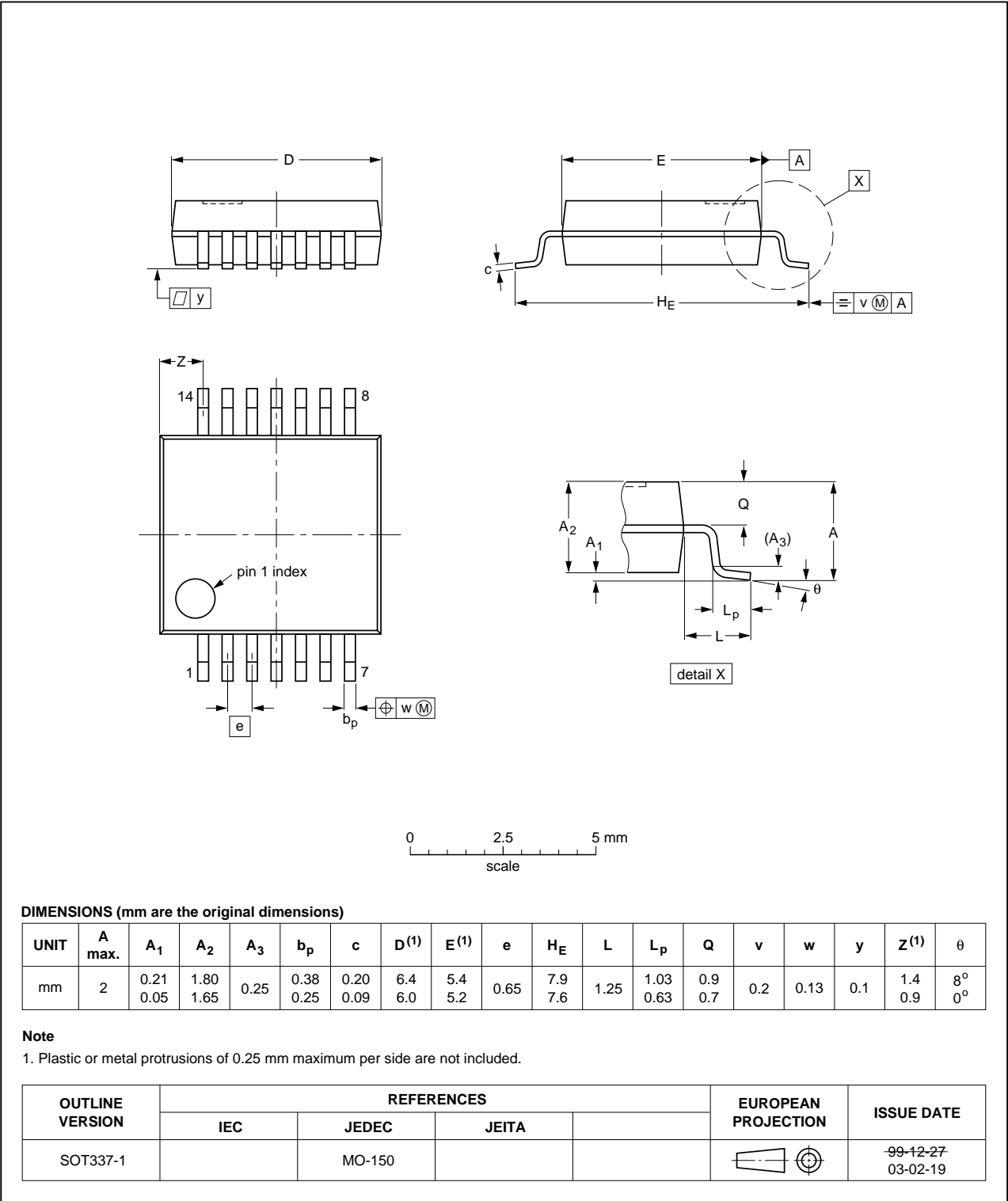


Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

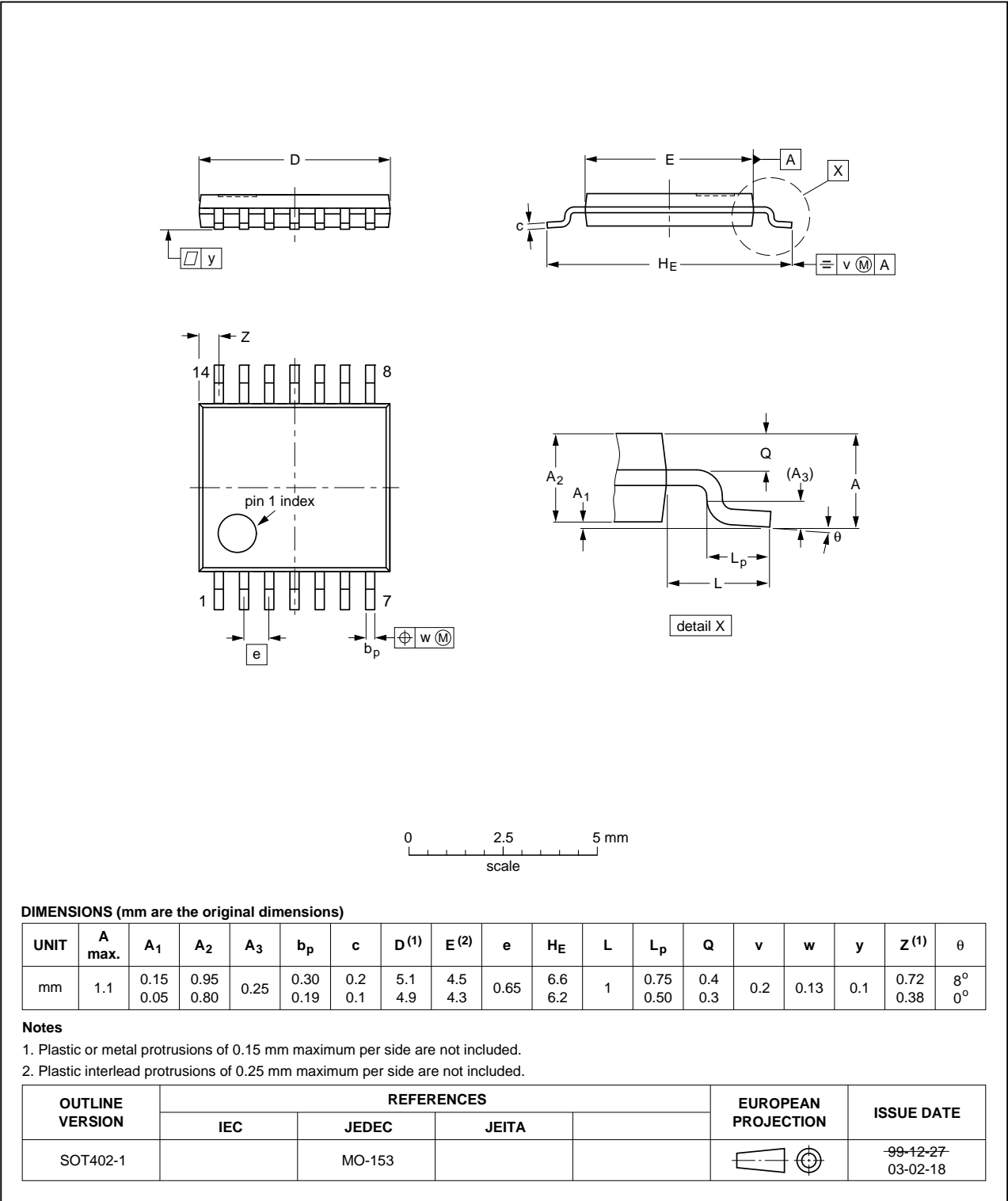


Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

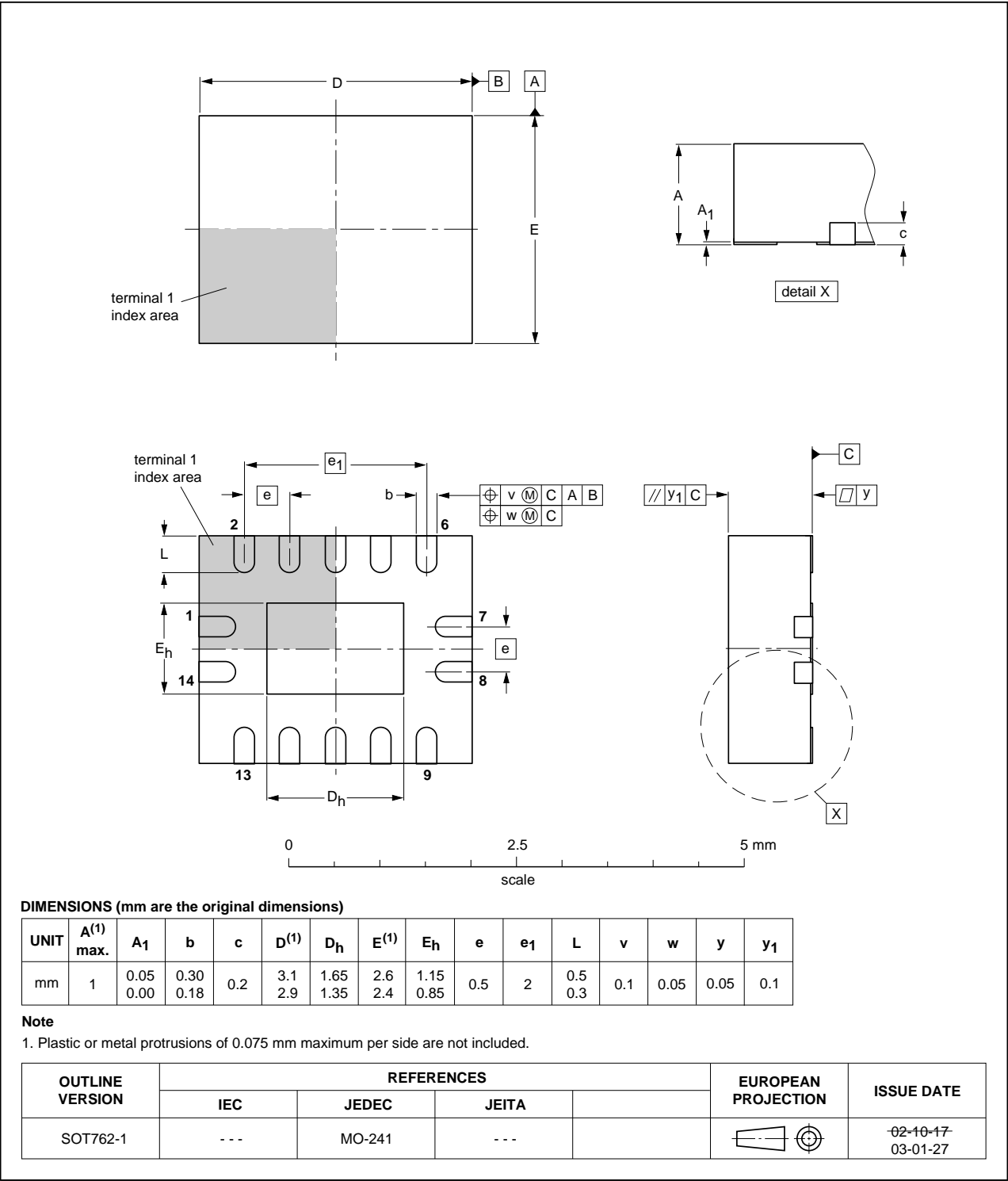


Fig 11. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC04A v.9	20111117	Product data sheet	-	74LVC04A v.8
Modifications:	<ul style="list-style-type: none"><li>Legal pages updated.</li><li><a href="#">Table 6</a>, bodyrow <math>\Delta I_{CC}</math>: condition <math>V_{CC}</math> changed.</li></ul>			
74LVC04A v.8	20110926	Product data sheet	-	74LVC04A v.7
74LVC04A v.7	20110201	Product data sheet	-	74LVC04A v.6
74LVC04A v.6	20030904	Product specification	-	74LVC04A v.5
74LVC04A v.5	20030224	Product specification	-	74LVC04A v.4
74LVC04A v.4	20020308	Product specification	-	74LVC04A v.3
74LVC04A v.3	19970630	Product specification	-	74LVC04A v.2
74LVC04A v.2	19970630	Product specification	-	74LVC04A v.1
74LVC04A v.1	19970203	Product specification	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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