

74LVC1G74-Q100

Single D-type flip-flop with set and reset; positive edge trigger

Rev. 2 — 14 May 2013

Product data sheet

1. General description

The 74LVC1G74-Q100 is a single positive edge triggered D-type flip-flop. It has individual data (D) inputs, clock (CP) inputs, set (\overline{SD}) and reset (\overline{RD}) inputs, and complementary Q and \overline{Q} outputs.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing damaging backflow current through the device when it is powered down.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- $\pm 24\text{ mA}$ output drive ($V_{CC} = 3.0\text{ V}$)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options



3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G74DP-Q100	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC1G74DC-Q100	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC1G74GD-Q100	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2

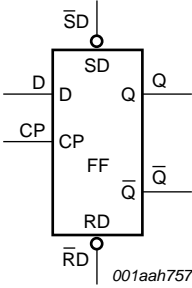
4. Marking

Table 2. Marking codes

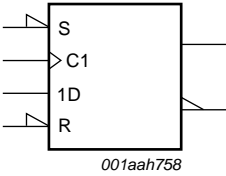
Type number	Marking code ^[1]
74LVC1G74DP-Q100	V74
74LVC1G74DC-Q100	V74
74LVC1G74GD-Q100	V74

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



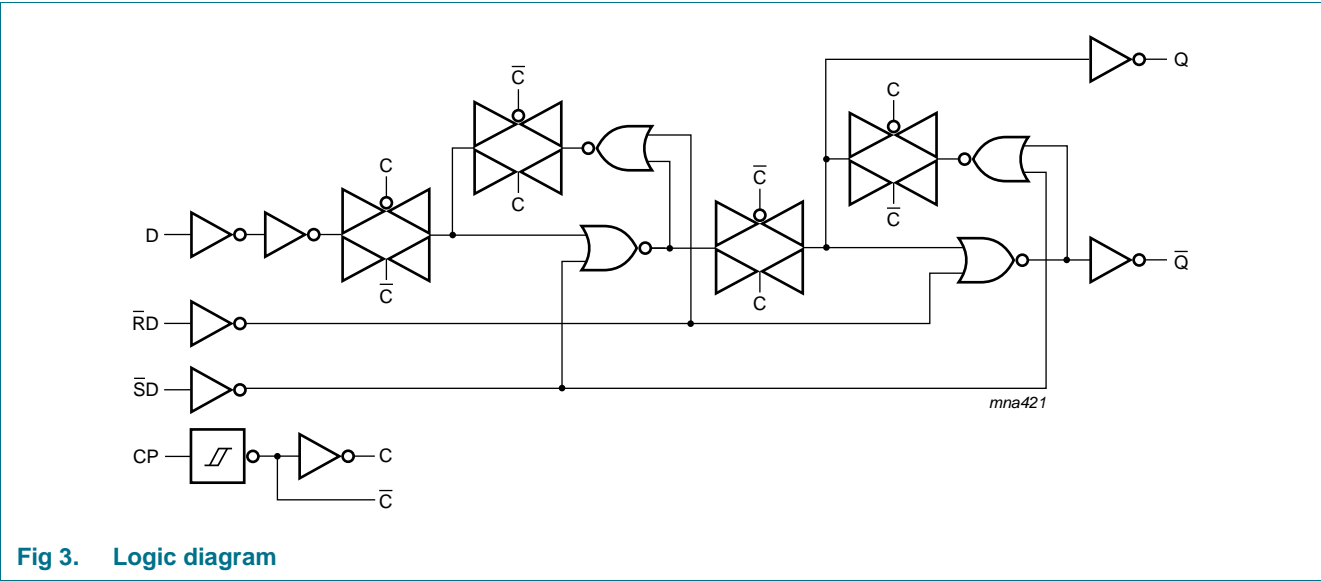
The logic symbol for the 74LVC1G74-Q100 is a rectangular block. It has two inputs on the left: 'D' (top) and 'CP' (bottom). It has two outputs on the right: 'Q' (top) and 'Q̄' (bottom). There are two additional inputs at the top: 'SD' (top) and 'RD' (bottom), both with a bubble indicating active-low. The symbol is labeled '001aah757' at the bottom right.



The IEC logic symbol for the 74LVC1G74-Q100 is a rectangular block. It has three inputs on the left: 'S' (top), 'C1' (middle), and '1D' (bottom). It has two outputs on the right: 'Q' (top) and 'Q̄' (bottom). There is an additional input at the bottom left labeled 'R'. The symbol is labeled '001aah758' at the bottom right.

Fig 1. Logic symbol

Fig 2. IEC logic symbol



6. Pinning information

6.1 Pinning

Fig 4. Pin configuration SOT505-2 and SOT765-1

Fig 5. Pin configuration SOT996-2

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
D	2	data input
\overline{Q}	3	complement output
GND	4	ground (0 V)
Q	5	true output
\overline{RD}	6	asynchronous reset-direct input (active LOW)
\overline{SD}	7	asynchronous set-direct input (active LOW)
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table for asynchronous operation^[1]

Input				Output	
$\overline{\text{SD}}$	$\overline{\text{RD}}$	CP	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

- [1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Table 5. Function table for synchronous operation^[1]

Input				Output	
$\overline{\text{SD}}$	$\overline{\text{RD}}$	CP	D	Q_{n+1}	$\overline{\text{Q}}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

- [1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
 Q_{n+1} = state after the next LOW-to-HIGH CP transition.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_{\text{I}} < 0 \text{ V}$	-50	-	mA
V_{I}	input voltage		^[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_{\text{O}} > V_{\text{CC}}$ or $V_{\text{O}} < 0 \text{ V}$	-	±50	mA
V_{O}	output voltage	Active mode	^[1] -0.5	$V_{\text{CC}} + 0.5$	V
		Power-down mode	^{[1][2]} -0.5	+6.5	V
I_{O}	output current	$V_{\text{O}} = 0 \text{ V to } V_{\text{CC}}$	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	$T_{\text{amb}} = -40 \text{ °C to } +125 \text{ °C}$	^[3] -	300	mW
T_{stg}	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] When $V_{\text{CC}} = 0 \text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.
 [3] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
 For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
 For XSON8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40$ °C to $+85$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	1.54	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	2.15	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.50	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	2.62	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.8	4.11	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ μ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.10	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	0.07	0.45	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	0.12	0.30	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.17	0.40	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.33	0.55	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	0.39	0.55	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V	-	± 0.1	± 5	μ A
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	± 0.1	± 10	μ A

Table 8. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_{CC}	supply current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 1.65\text{ V}$ to 5.5 V ; $I_O = 0\text{ A}$	-	0.1	10	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 2.3\text{ V}$ to 5.5 V	-	5	500	μA
C_I	input capacitance		-	4.0	-	pF
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V}$ to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V}$ to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}$; $V_{CC} = 1.65\text{ V}$	0.95	-	-	V
		$I_O = -8\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.7	-	-	V
		$I_O = -12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	1.9	-	-	V
		$I_O = -24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.0	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V}$ to 5.5 V	-	-	0.10	V
		$I_O = 4\text{ mA}$; $V_{CC} = 1.65\text{ V}$	-	-	0.70	V
		$I_O = 8\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	-	0.45	V
		$I_O = 12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	-	-	0.60	V
		$I_O = 24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	-	0.80	V
I_I	input leakage current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 0\text{ V}$ to 5.5 V	-	-	± 20	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5\text{ V}$; $V_{CC} = 0\text{ V}$	-	-	± 20	μA
I_{CC}	supply current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 1.65\text{ V}$ to 5.5 V ; $I_O = 0\text{ A}$	-	-	40	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 2.3\text{ V}$ to 5.5 V	-	-	5000	μA

[1] All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Q, \bar{Q} ; see Figure 6 ^[2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	6.0	13.4	1.5	13.4	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.5	5.9	1.0	5.9	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
		\bar{SD} to Q, \bar{Q} ; see Figure 7 ^[2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	6.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	5.9	1.0	5.9	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
		\bar{RD} to Q, \bar{Q} ; see Figure 7 ^[2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	5.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	5.9	1.0	5.9	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
t_w	pulse width	CP HIGH or LOW; see Figure 6						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.2	-	-	6.2	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.7	1.3	-	2.7	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	2.0	-	ns
		\bar{SD} and \bar{RD} LOW; see Figure 7						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.2	-	-	6.2	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 2.7\text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.7	1.6	-	2.7	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	2.0	-	ns

Table 9. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

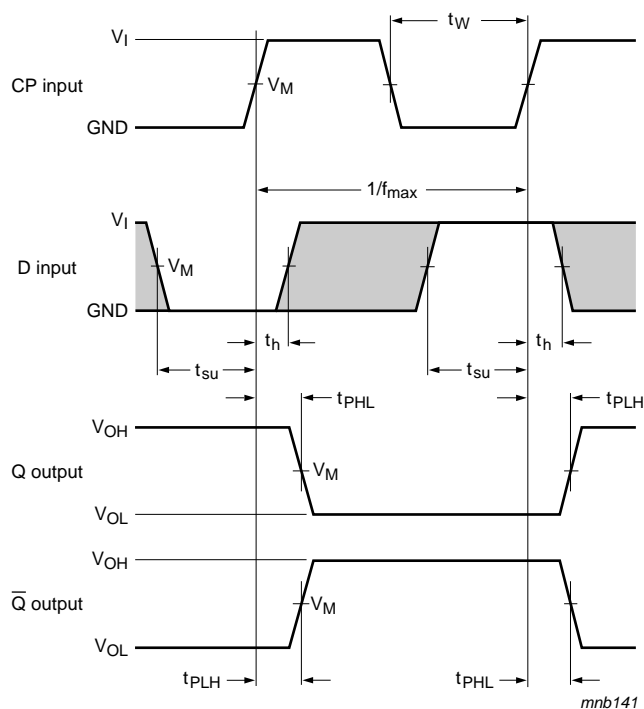
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{rec}	recovery time	\overline{SD} or \overline{RD} ; see Figure 7						
		V _{CC} = 1.65 V to 1.95 V	1.9	-	-	1.9	-	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	ns
		V _{CC} = 2.7 V	1.3	-	-	1.3	-	ns
		V _{CC} = 3.0 V to 3.6 V	+1.2	–3.0	-	+1.2	-	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
t _{su}	set-up time	D to CP; see Figure 6						
		V _{CC} = 1.65 V to 1.95 V	2.9	-	-	2.9	-	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	ns
		V _{CC} = 2.7 V	1.7	-	-	1.7	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	0.5	-	1.3	-	ns
		V _{CC} = 4.5 V to 5.5 V	1.1	-	-	1.1	-	ns
t _h	hold time	D to CP; see Figure 6						
		V _{CC} = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	-	-	1.0	-	ns
		V _{CC} = 2.7 V	1.0	-	-	1.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	0.6	-	1.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
f _{max}	maximum frequency	CP; see Figure 6						
		V _{CC} = 1.65 V to 1.95 V	80	-	-	80	-	MHz
		V _{CC} = 2.3 V to 2.7 V	175	-	-	175	-	MHz
		V _{CC} = 2.7 V	175	-	-	175	-	MHz
		V _{CC} = 3.0 V to 3.6 V	175	280	-	175	-	MHz
		V _{CC} = 4.5 V to 5.5 V	200	-	-	200	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V	[3]	-	15	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.[2] t_{pd} is the same as t_{PLH} and t_{PHL}.[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:f_i = input frequency in MHz;f_o = output frequency in MHz;C_L = output load capacitance in pF;V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



Measurement points are given in [Table 10](#).

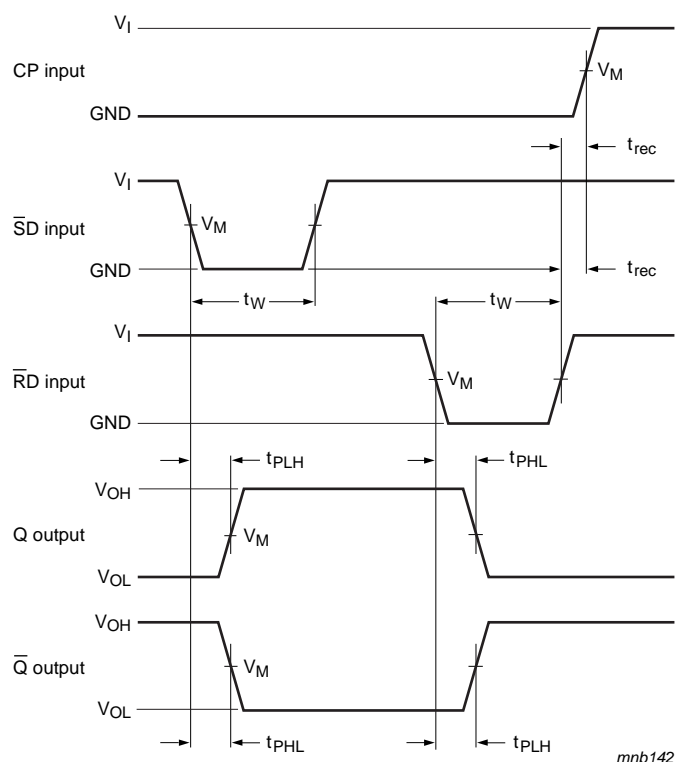
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The clock input (CP) to output (Q, \bar{Q}) propagation delays and pulse width, D to CP set-up, CP to D hold times and the maximum frequency

Table 10. Measurement points

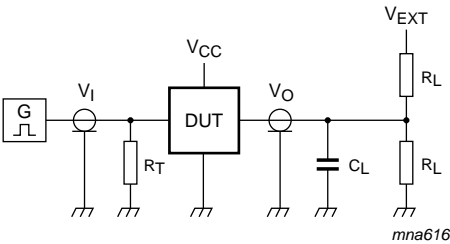
Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The set (\overline{SD}) and reset (\overline{RD}) input to output (Q, \overline{Q}) propagation delays, pulse widths and the \overline{RD} to CP recovery time



Test data is given in [Table 11](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2 × V _{CC}
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2 × V _{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V _{CC}

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

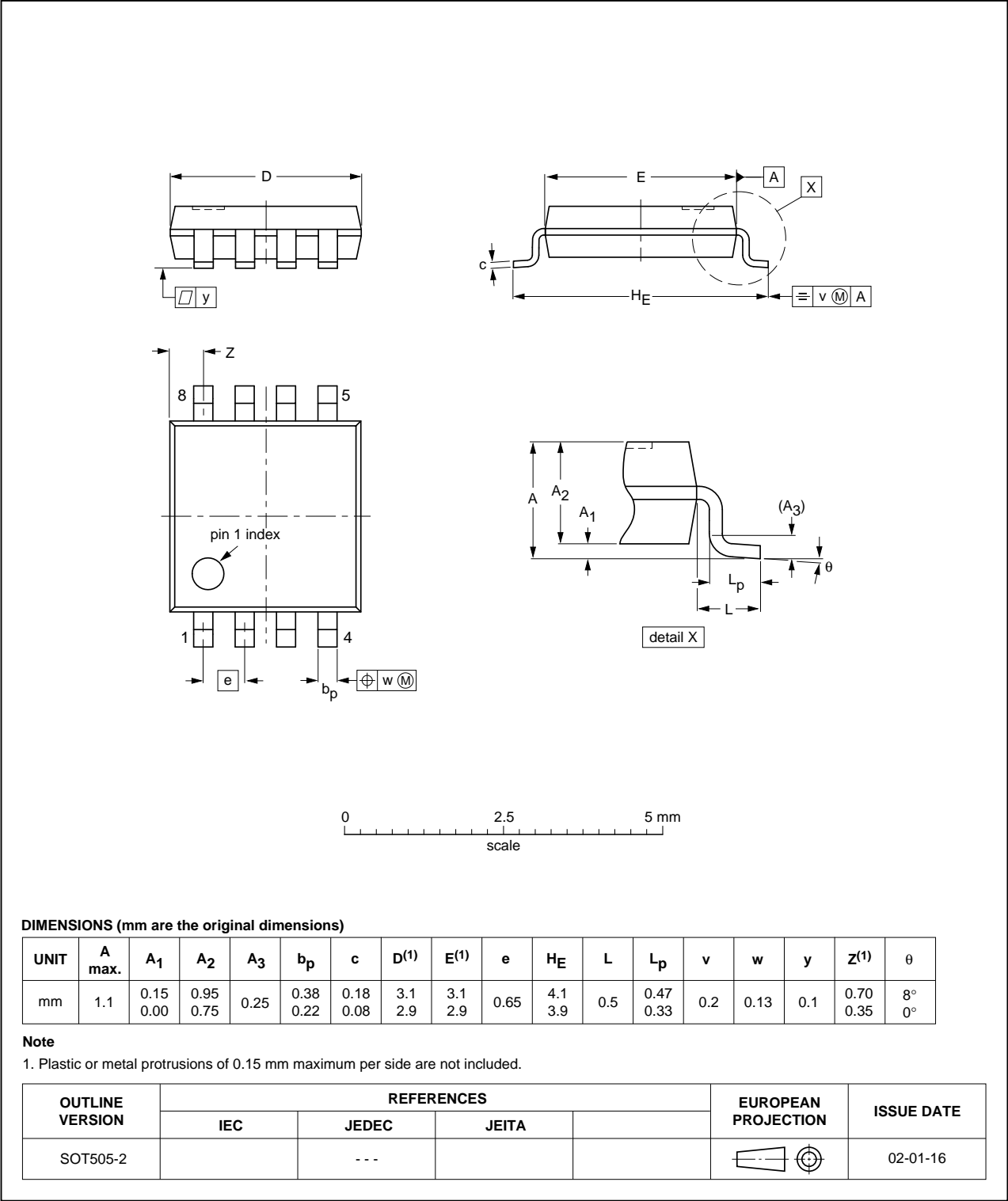


Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

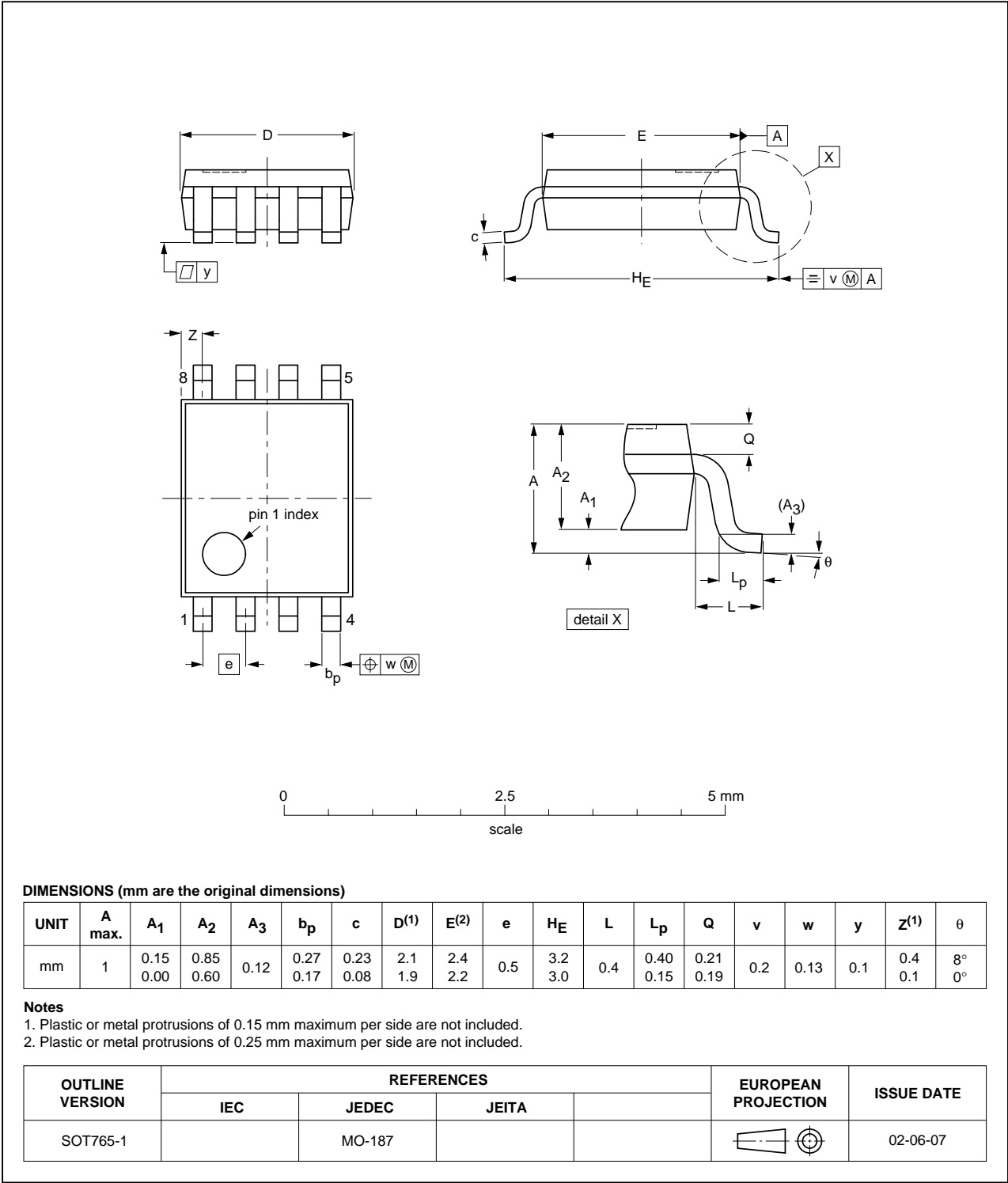


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

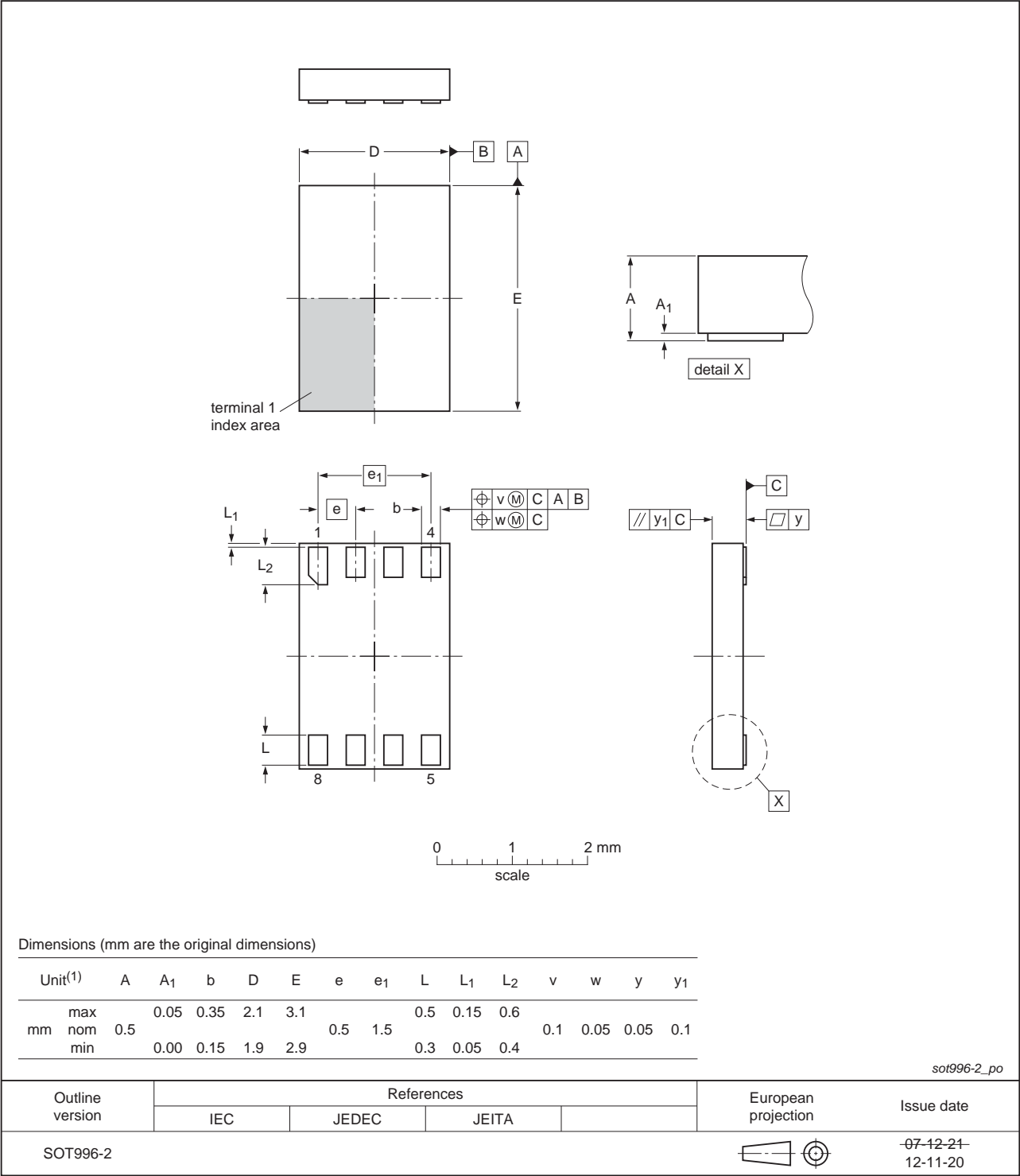


Fig 11. Package outline SOT996-2 (XSON8)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test
TTL	Transistor-Transistor Logic
MIL	Military

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G74_Q100 v.2	20130514	Product data sheet	-	74LVC1G74_Q100 v.1
Modifications:	• 74LVC1G74GD-Q100 (XSON8) added.			
74LVC1G74_Q100 v.1	20120807	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
8	Limiting values	4
9	Recommended operating conditions	5
10	Static characteristics	5
11	Dynamic characteristics	7
12	Waveforms	9
13	Package outline	12
14	Abbreviations	15
15	Revision history	15
16	Legal information	16
16.1	Data sheet status	16
16.2	Definitions	16
16.3	Disclaimers	16
16.4	Trademarks	17
17	Contact information	17
18	Contents	18

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 May 2013

Document identifier: 74LVC1G74_Q100