74LVC32A-Q100

Quad 2-input OR gate
Rev. 2 — 28 February 2013

Product data sheet

1. **General description**

The 74LVC32A-Q100 provides four 2-input OR gates.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 5 V tolerant inputs for interlacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

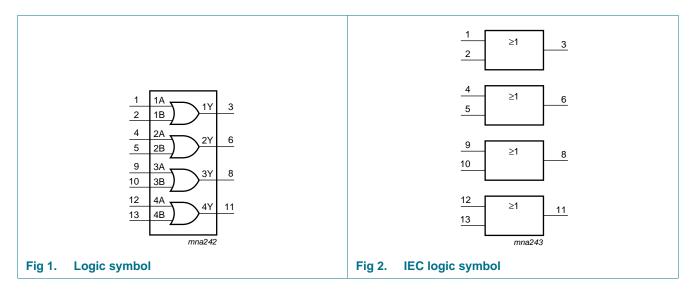


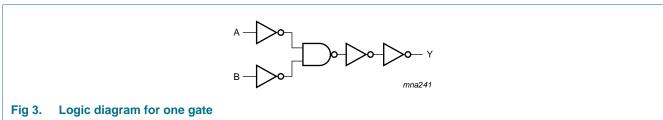
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC32AD-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC32ADB-Q100	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC32APW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC32ABQ-Q100	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5\times3\times0.85$ mm	SOT762-1

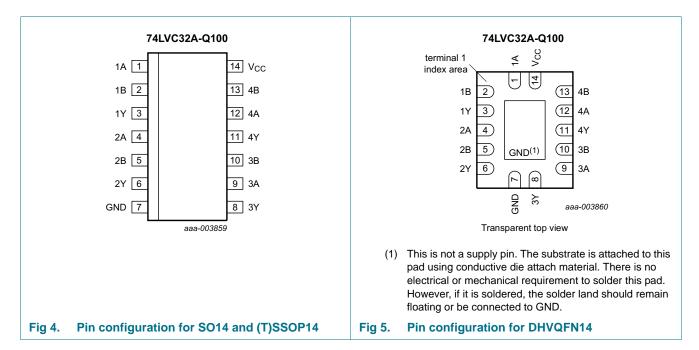
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection[1]

Input		Output
nA	nB	nY
L	L	L
X	Н	Н
Н	X	Н

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
VI	input voltage		[<u>1</u>] -0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
Vo	output voltage		[<u>2</u>] -0.5	$V_{CC} + 0.5$	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[3] _	500	mW

^[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_{I}	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
	rate	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

^[2] The output voltage ratings may be exceeded if the output current ratings are observed.

^[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For (T)SSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	35 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	V _{CC} - 0.2	-	-	$V_{CC}-0.3$	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
II	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μА
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND};$ $I_O = 0 \text{ A}$	-	0.1	10	-	40	μА
Δl _{CC}	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$	-	5	500	-	5000	μА
C _I	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_{I} = \text{GND to } V_{CC}$	-	4.0	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions		-40	°C to +8	5 °C	−40 °C to	+125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB to nY; see Figure 6	[2]						
		V _{CC} = 1.2 V		-	10	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.5	4.2	9.0	0.5	10.4	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.5	2.4	4.9	1.05	5.7	ns
		$V_{CC} = 2.7 \text{ V}$		1.5	2.5	4.4	1.5	5.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	2.2	3.8	1.0	5.0	ns
t _{sk(o)}	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation	per gate; $V_I = GND$ to V_{CC}	[4]						
	capacitance	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		-	4.7	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-	8.0	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	11.0	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

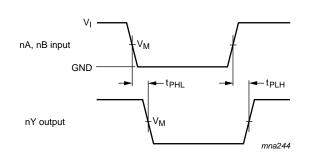
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

^[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

^[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

^[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

11. AC waveforms

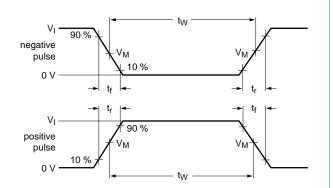


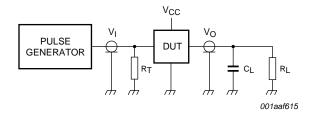
 V_M = 1.5 V at $V_{CC} \ge 2.7$ V

 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \ V.$

 $\mbox{V}_{\mbox{\scriptsize OL}}$ and $\mbox{V}_{\mbox{\scriptsize OH}}$ are typical output voltage levels that occur with the output load.

Fig 6. The input nA, nB to output nY propagation delays





Test data is given in Table 8. Definitions for test circuit:

 R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 $R_{T} = \mbox{Termination}$ resistance should be equal to output impedance Z_{o} of the pulse generator.

Fig 7. Test circuit for measuring switching times

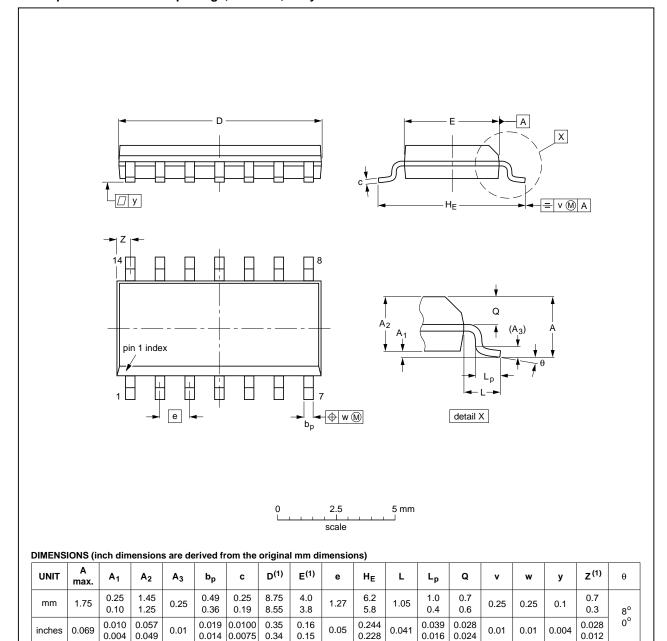
Table 8. Test data

Supply voltage	Input		Load					
	VI	t _r , t _f	CL	R _L				
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ				
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ				
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω				
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω				
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	$500~\Omega$				

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

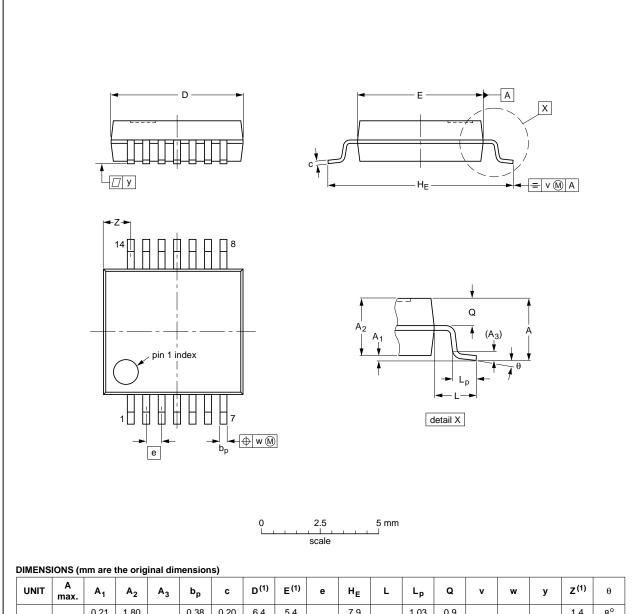
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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E ⁽¹⁾	e	HE	٦	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT337-1		MO-150				-99-12-27 03-02-19
					·	

Fig 9. Package outline SOT337-1 (SSOP14)

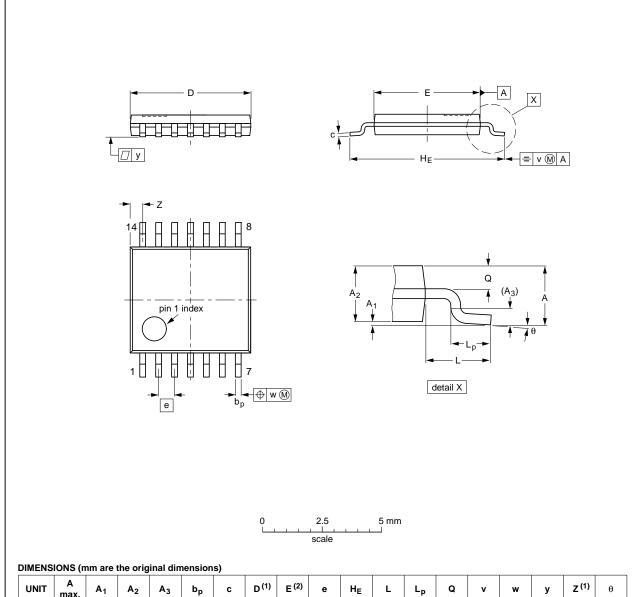
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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Ξ							-,												
	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				99-12-27 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

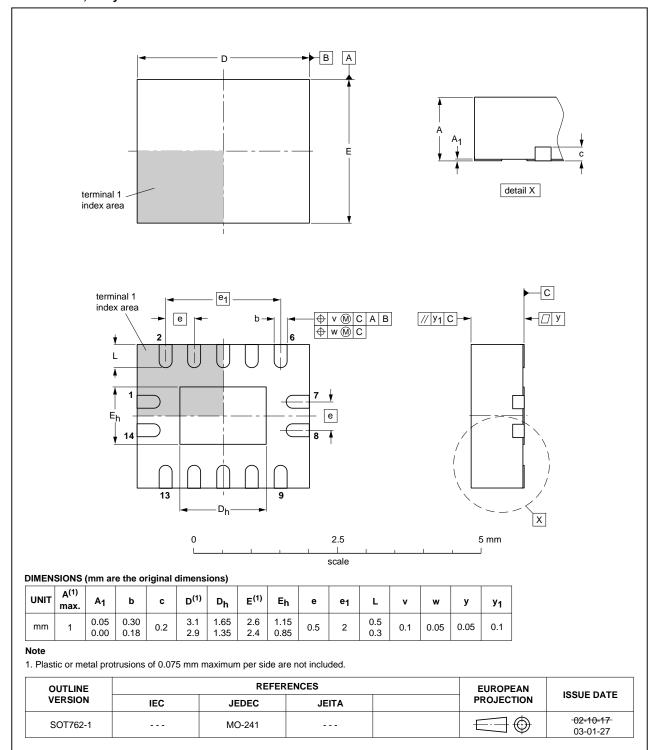


Fig 11. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description	
CDM	Charged Device Model	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
MM	Machine Model	
НВМ	Human Body Model	
TTL	Transistor-Transistor Logic	
MIL	Military	

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC32A_Q100 v.2	20130228	Product data sheet	-	74LVC32A_Q100 v.1
Modifications:	 74LVC32ADB- 	Q100 (SSOP14) added.		
74LVC32A_Q100 v.1	20120807	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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