BLS7G3135LS-200

LDMOS S-band radar power transistor

Rev. 2 — 23 September 2013 Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for S-band radar applications in the frequency range from 3100 MHz to 3500 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 300 µs; δ = 10 %; I_{Dq} = 100 mA; in a class-AB production test circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D	t_r	t_f
	(GHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	3.1	32	200	12	48	8	6
	3.3	32	200	12	46	8	6
	3.5	32	200	12	43	8	6

1.2 Features and benefits

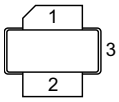
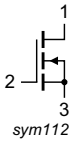
- High efficiency
- Excellent ruggedness
- Designed for broadband operation
- Excellent thermal stability
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Internally matched for ease of use (input and output)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-band radar applications in the frequency range 3100 MHz to 3500 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS7G3135LS-200	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter		Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	T_{case} = 85 °C; P_L = 200 W		
		t_p = 100 μs; δ = 20 %	0.147	K/W
		t_p = 200 μs; δ = 20 %	0.162	K/W
		t_p = 500 μs; δ = 20 %	0.186	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	51	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.7 A	-	2.34	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	0.06	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 200 W	8.8	12	-	dB
RL_{in}	input return loss	P_L = 200 W	-	–8	–4	dB
η_D	drain efficiency	P_L = 200 W	38	43	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 200 W		0.1	0.25	dB
t_r	rise time	P_L = 200 W	-	8	50	ns
t_f	fall time	P_L = 200 W	-	6	50	ns

7. Test information

7.1 Ruggedness in class-AB operation

The BLS7G3135LS-200 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 100 mA; P_L = 200 W; f = 3100 MHz; t_p = 300 μs; δ = 10 %.

7.2 Impedance information

Table 8. Typical impedance

Measured load pull data; V_{DS} = 32 V; I_{Dq} = 100 mA; typical values unless otherwise specified.

f (MHz)	Z_S (Ω)	Z_L (Ω)
3100	0.9 – j4.3	5.3 – j1.6
3200	1.3 – j4.9	4.8 – j1.5
3300	1.7 – j5.5	4.6 – j1.9
3400	2.4 – j6.4	4.0 – j2.1
3500	4.1 – j6.9	4.0 – j2.1

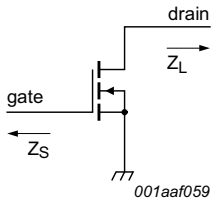
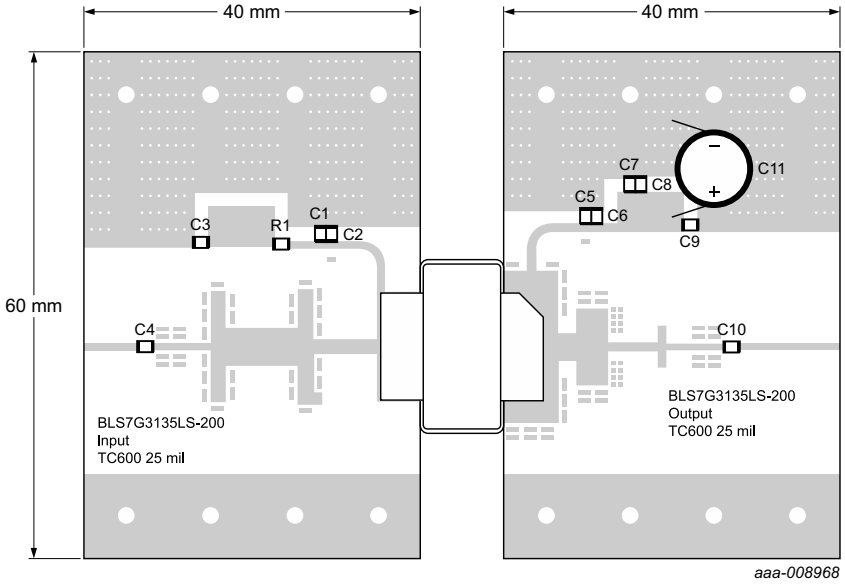


Fig 1. Definition of transistor impedance

7.3 Test circuit information



Printed-Circuit Board (PCB): Arlon TC600 with a thickness of 0.64 mm. See Table 9 for list of components.

Fig 2. Component layout

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value		Remarks
C1, C4, C4, C10	multilayer ceramic chip capacitor	15 pF	[1]	ATC600F
C2, C5	multilayer ceramic chip capacitor	10 pF	[1]	ATC600F
C3, C9	multilayer ceramic chip capacitor	0.1 μF	[2]	TDK
C7	multilayer ceramic chip capacitor	1 μF	[3]	Murata
C8	multilayer ceramic chip capacitor	10 μF	[3]	Murata
C11	electrolytic capacitor	2200 μF, 63 V		
R1	chip resistor	9.1 Ω	[4]	SMD 0805

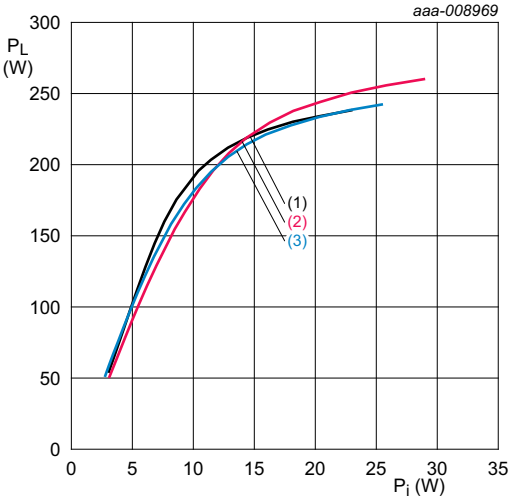
[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] TDK or capacitor of same quality.

[3] Murata or capacitor of same quality.

[4] Vishay Dale or resistor of same quality.

7.4 Graphical data



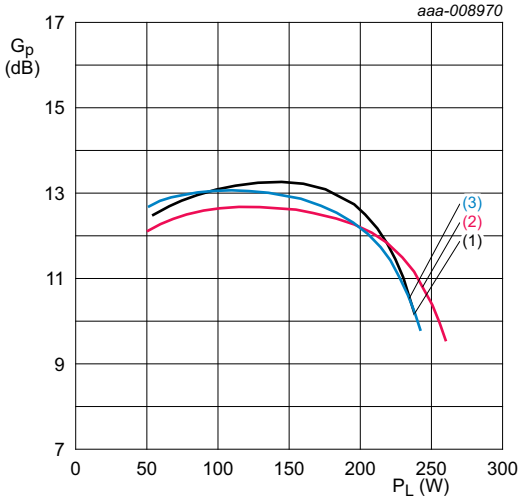
V_{DS} = 32 V; I_{Dq} = 100 mA; δ = 10 %; t_p = 300 µs.

(1) f = 3100 MHz

(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 3. Output power as a function of input power; typical values



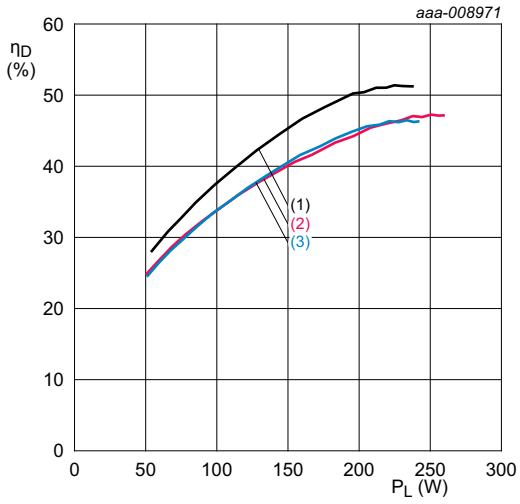
V_{DS} = 32 V; I_{Dq} = 100 mA; δ = 10 %; t_p = 300 µs.

(1) f = 3100 MHz

(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 4. Power gain as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 100 mA; δ = 10 %; t_p = 300 µs.

(1) f = 3100 MHz

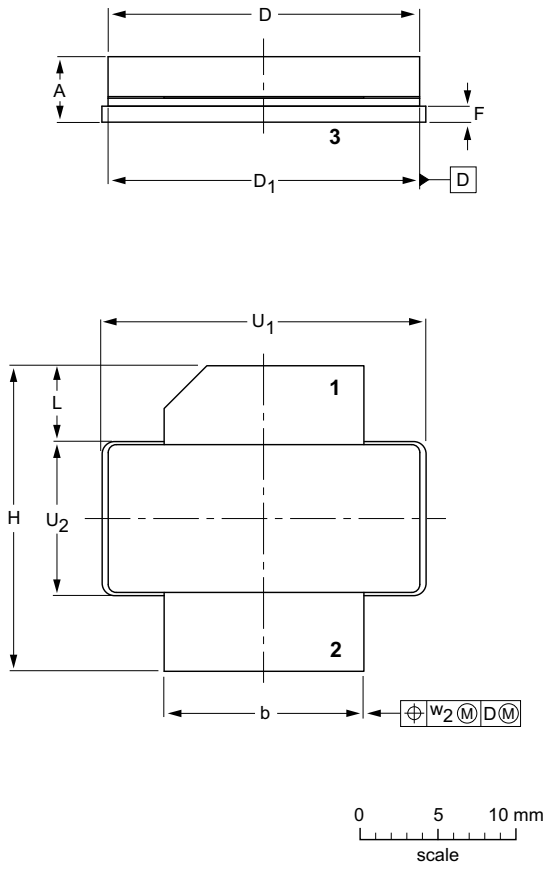
(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 5. Drain efficiency as a function of output power; typical values

8. Package outline

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 6. Package outline SOT502B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
S-band	Short wave band
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS7G3135LS-200 v.2	20130923	Product data sheet	-	BLS7G3135LS-200 v.1
Modifications:	• Table 1 on page 1: table updated. • Section 1.2 on page 1: section updated. • Table 4 on page 2: table note added. • Table 5 on page 2: table updated. • Table 6 on page 3: table updated. • Table 7 on page 3: table updated. • Section 7 on page 3: section added.			
BLS7G3135LS-200 v.1	20121009	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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Date of release: 23 September 2013
Document identifier: BLS7G3135LS-200