BTA2008-800E

3Q Hi-Com Triac

8 November 2012 Product data sheet

1. Product profile

1.1 General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

1.2 Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High commutation capability with sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

1.3 Applications

- Low power motor controls
- Small inductive loads e.g. solenoids, door locks, water valves
- Small loads in large white goods

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	-	9	A
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 70$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	0.8	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		0.5	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA

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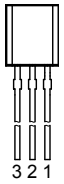
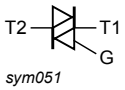
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 TO-92 (SOT54)	 sym051
2	G	gate		
3	T1	main terminal 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA2008-800E	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

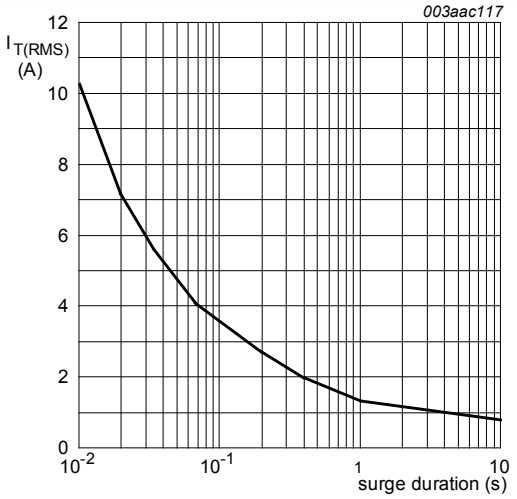
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; T_{lead} ≤ 70 °C; Fig. 1; Fig. 2; Fig. 3		-	0.8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	9	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		-	9.9	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	0.41	A^2s
dI_T/dt	rate of rise of on-state current	I_T = 1.5 A; I_G = 20 mA; dI_G/dt = 0.2 A/µs		-	100	A/µs
I_{GM}	peak gate current			-	1	A
P_{GM}	peak gate power			-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-	125	°C



f = 50 Hz; T_{lead} = 70 °C

Fig. 1. RMS on-state current as a function of surge duration; maximum values

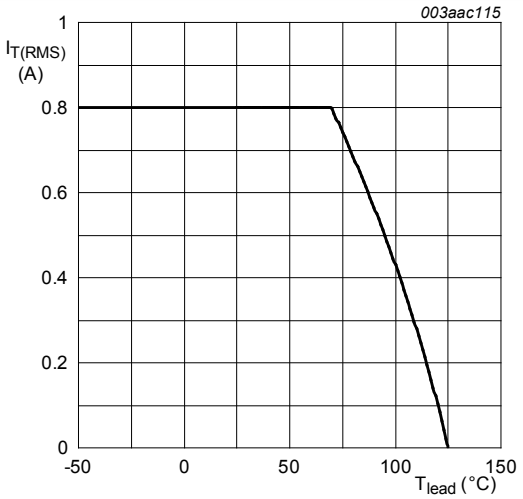
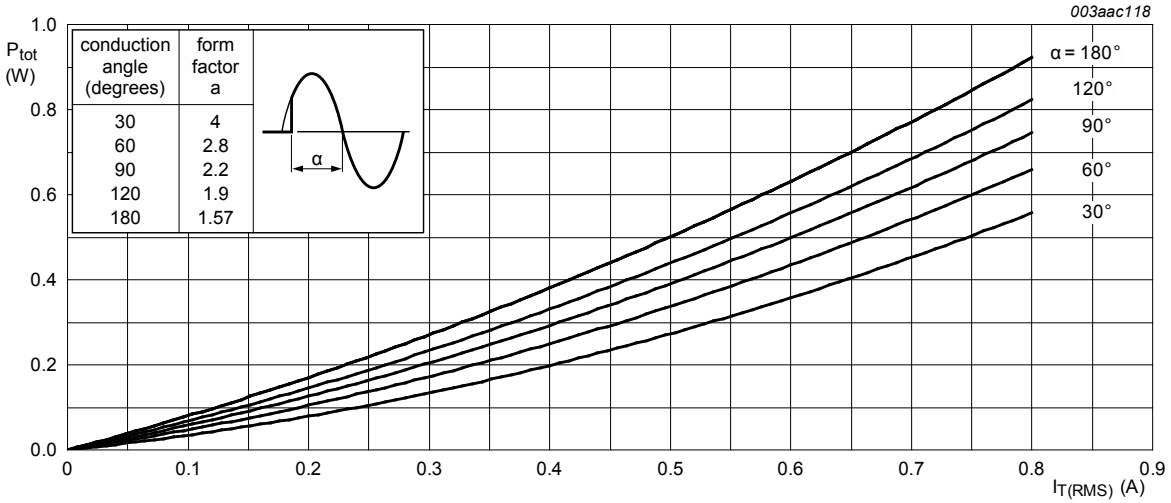


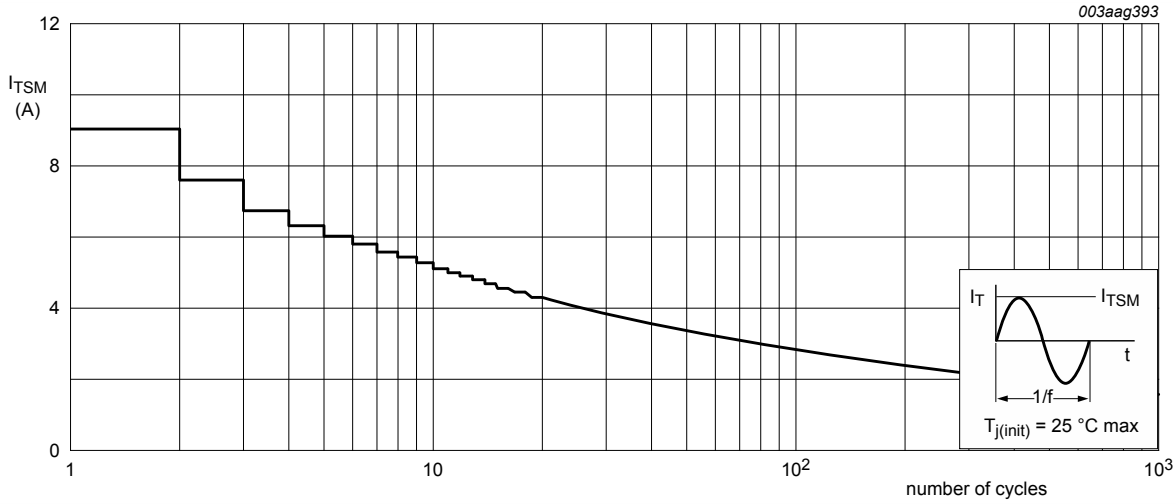
Fig. 2. RMS on-state current as a function of lead temperature; maximum values



α = conduction angle

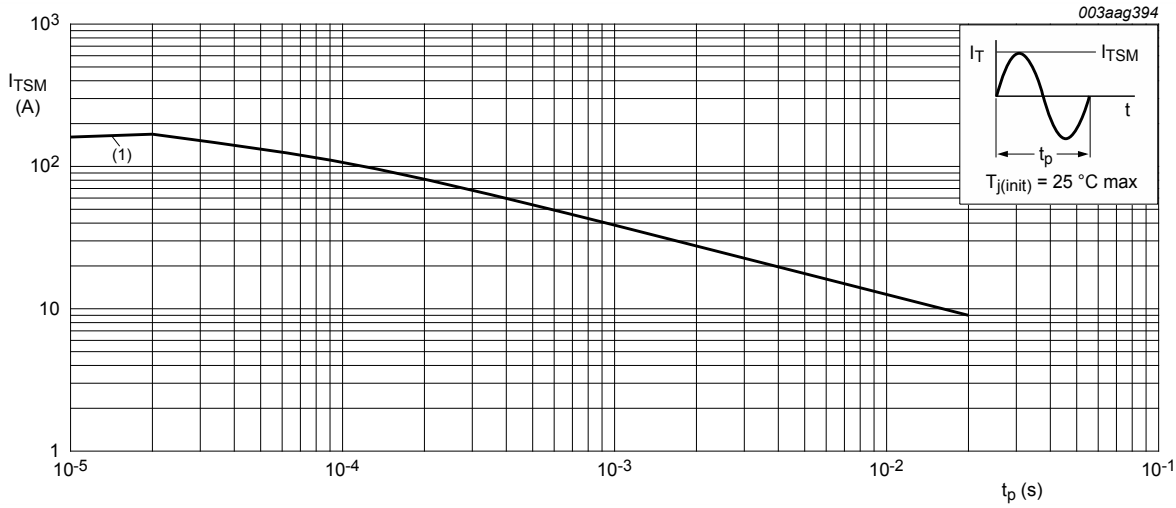
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms; (1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	full cycle; Fig. 6		-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm		-	150	-	K/W

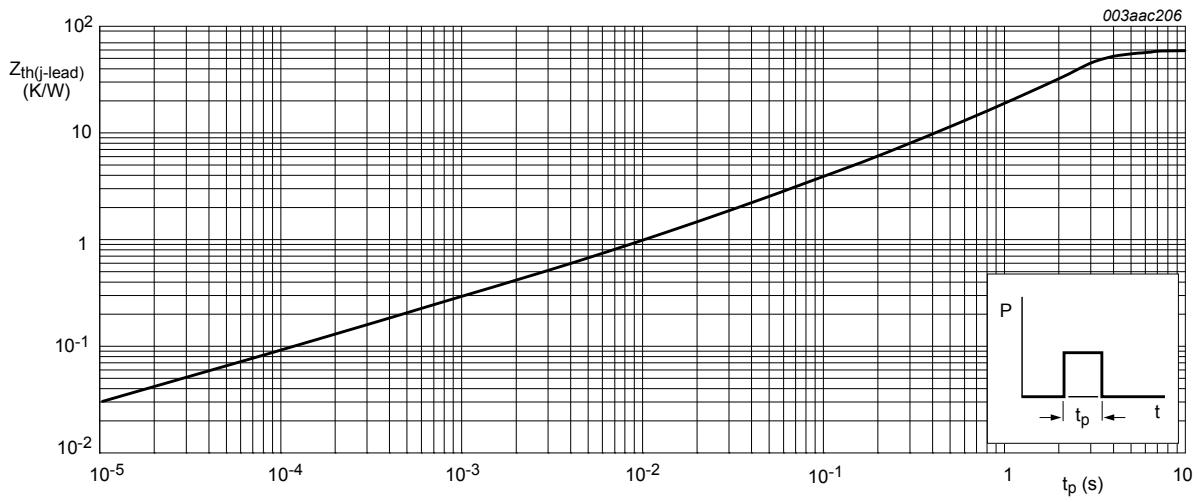


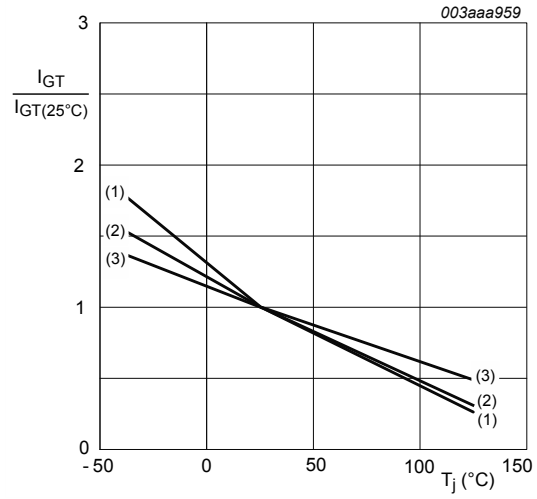
Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		0.5	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		0.5	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	-	12	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	-	20	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	-	12	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	12	mA
V_T	on-state voltage	I_T = 0.85 A; T_j = 25 °C; Fig. 10		-	1.35	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.9	2	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.2	0.3	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		600	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 0.8 A; dV_{com}/dt = 10 V/µs; gate open circuit		1.6	-	-	A/ms



(1) T2- G-
(2) T2+ G-
(3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

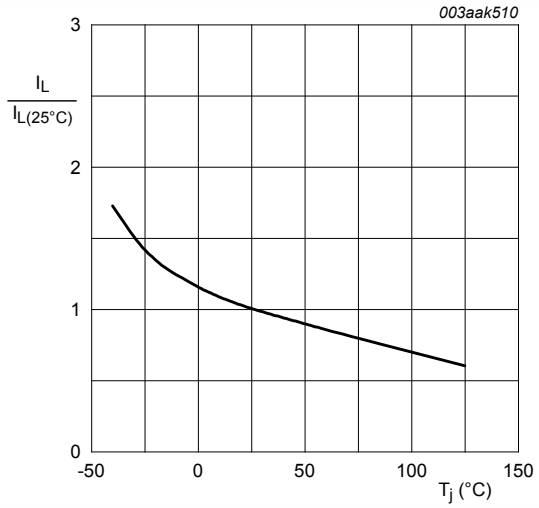


Fig. 8. Normalized latching current as a function of junction temperature

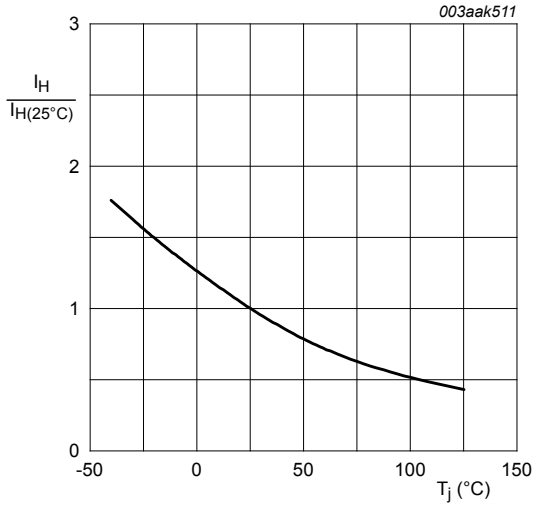
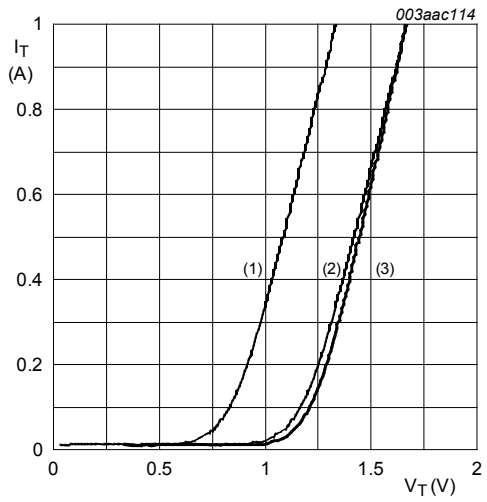


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 0.835 V; R_s = 0.50 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

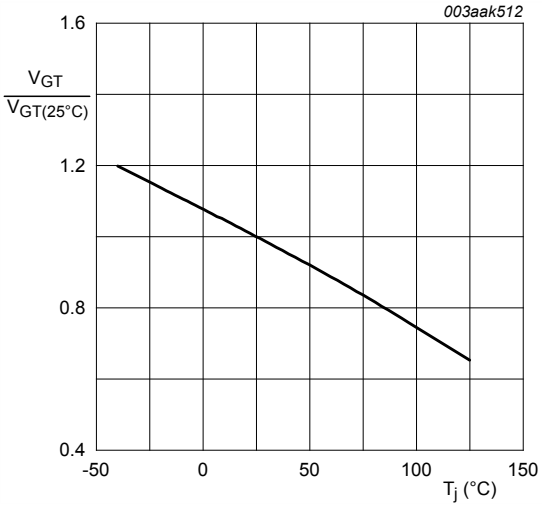
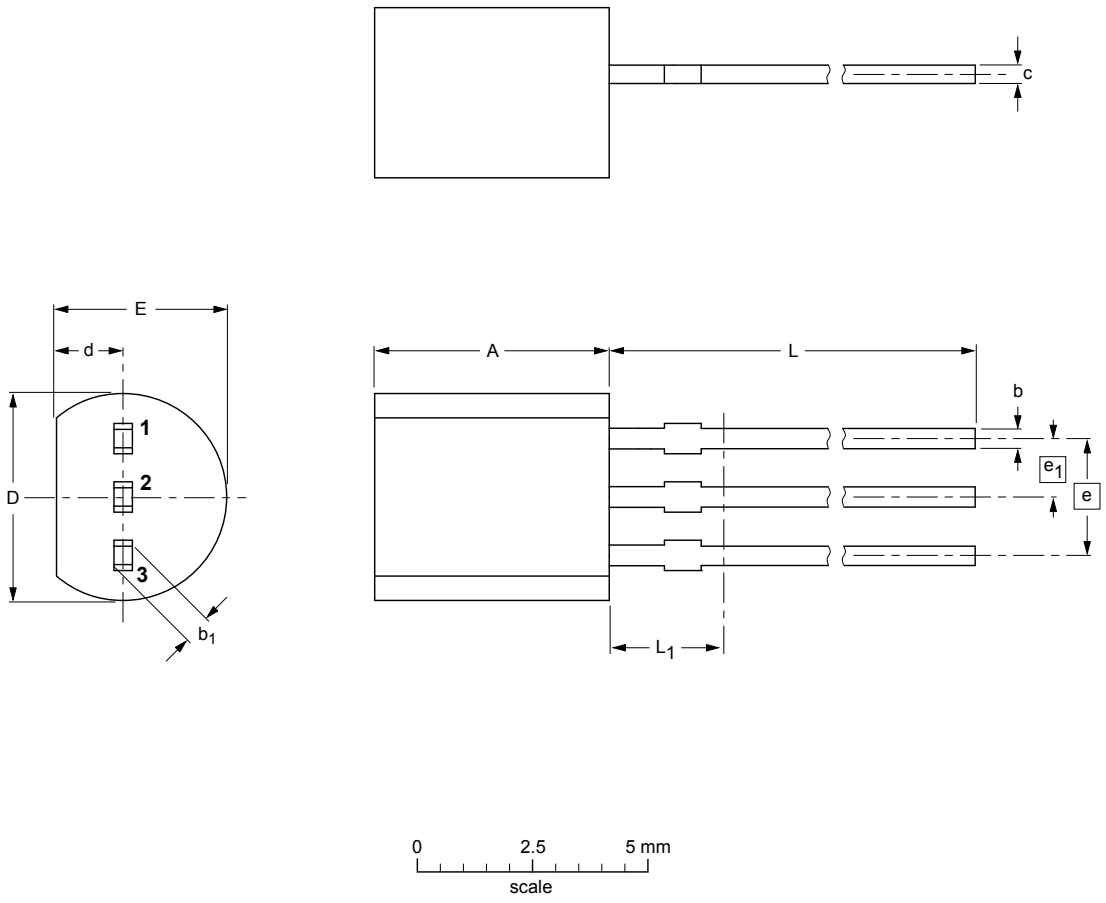


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig. 12. Package outline TO-92 (SOT54)

8. Legal information

8.1 Data sheet status

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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