# BUK7606-55B

## N-channel TrenchMOS standard level FET

Rev. 02 — 21 June 2010 Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V and 24 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

**Table 1. Quick reference data**

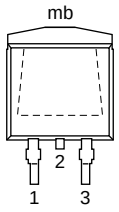
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | - | 55 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; see Figure 1; see Figure 3 | [1] | - | - | 75 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 2 | | - | - | 254 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 11; see Figure 12 | | - | 5.1 | 6 | mΩ |
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 75 A; $V_{sup} \leq 55$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped | | - | - | 680 | mJ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 10 V; $I_D$ = 25 A; $V_{DS}$ = 44 V; $T_j$ = 25 °C; see Figure 13 | | - | 19 | - | nC |

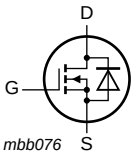
[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate | | |
| 2 | D | drain[1] | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |




**SOT404 (D2PAK)**

[1] It is not possible to make connection to pin 2.

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK7606-55B | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

# 4. Limiting values

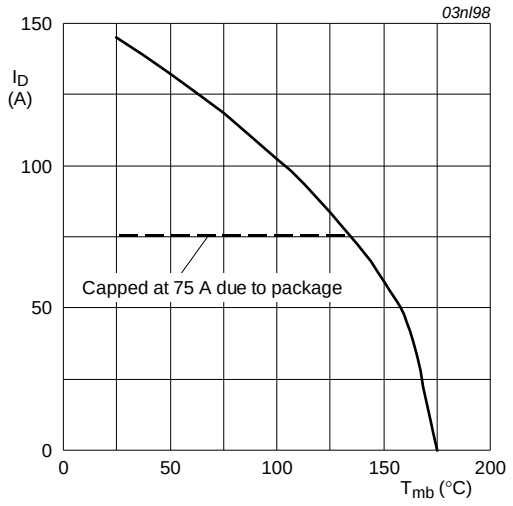
**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | - | 55 | V |
| $V_{DGR}$ | drain-gate voltage | $R_{GS}$ = 20 kΩ | | - | - | 55 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | - | 20 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see Figure 3; see Figure 1 | [1] | - | - | 145 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; see Figure 1 | [2] | - | - | 75 | A |
| | | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see Figure 1; see Figure 3 | [2] | - | - | 75 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; $t_p \leq 10$ µs; pulsed; see Figure 3 | | - | - | 582 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 2 | | - | - | 254 | W |
| $T_{stg}$ | storage temperature | | | -55 | - | 175 | °C |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Source-drain diode** | | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [1] | - | - | 145 | A |
| | | | [2] | - | - | 75 | A |
| $I_{SM}$ | peak source current | $t_p \leq 10$ µs; pulsed; $T_{mb}$ = 25 °C | | - | - | 582 | A |
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 75 A; $V_{sup} \leq 55$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped | | - | - | 680 | mJ |

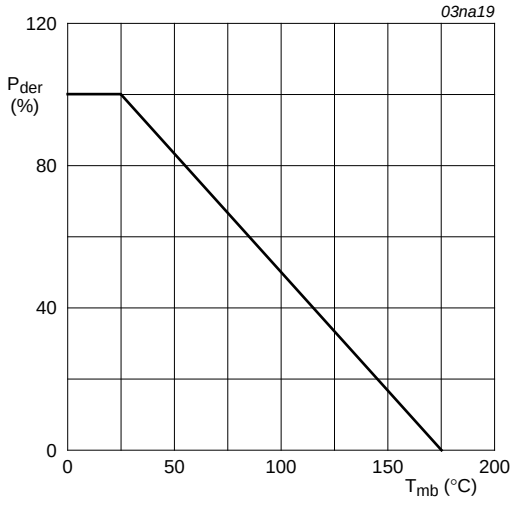
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



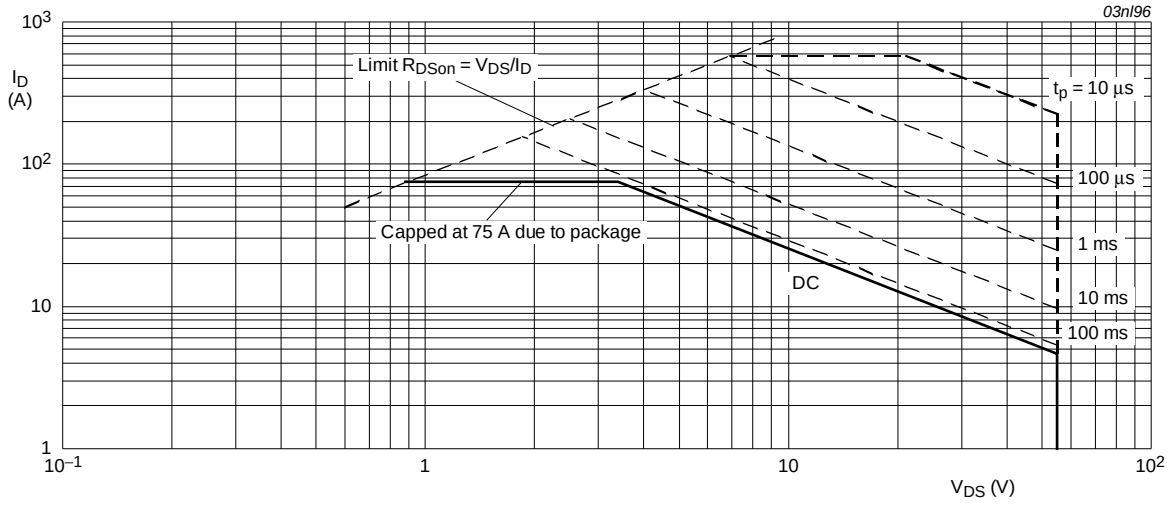

$V_{GS} \geq 10V$

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**




$T_{mb} = 25°C; I_{DM}$ is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 0.59 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | minimum footprint; mounted on a printed-circuit board | - | - | 50 | K/W |

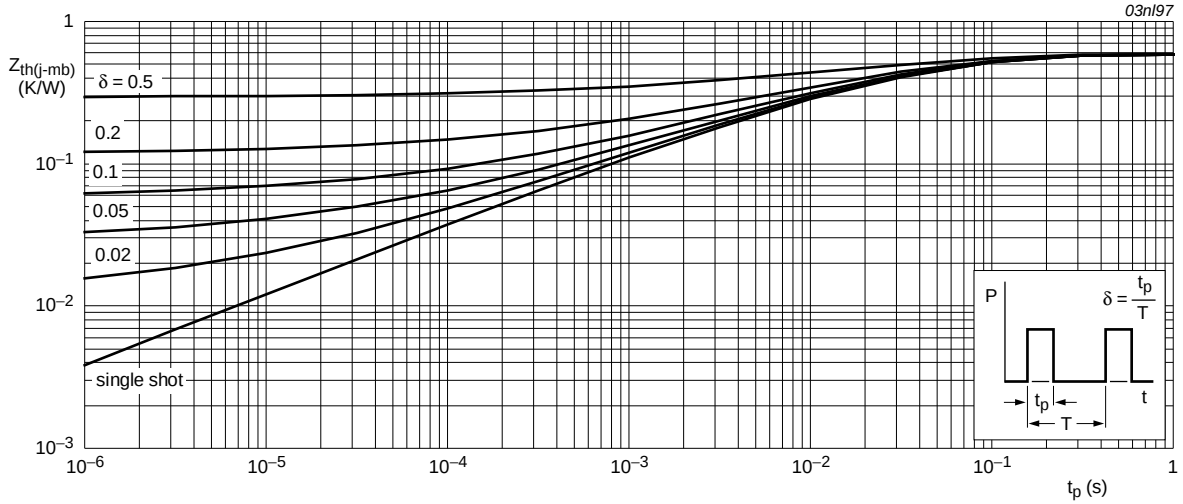
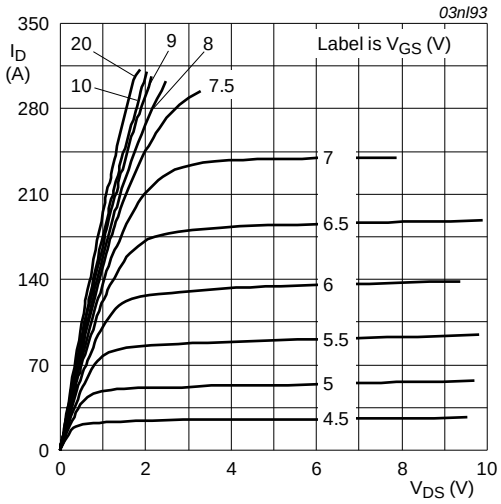



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

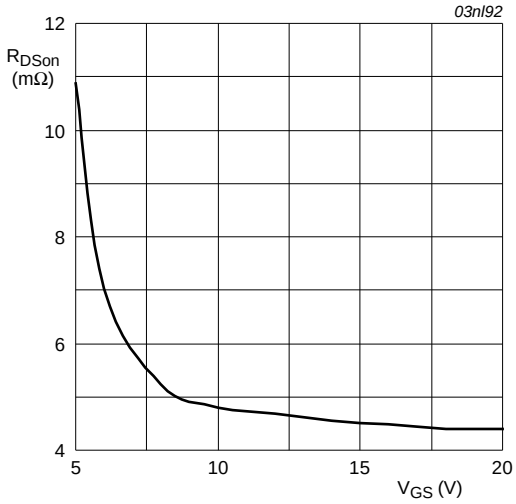
**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 0.25 mA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 55 | - | - | V |
| | | $I_D$ = 0.25 mA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 50 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 10 | - | - | 4.4 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 10 | 2 | 3 | 4 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; see Figure 10 | 1 | - | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 55 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | 0.02 | 1 | µA |
| | | $V_{DS}$ = 55 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{DS}$ = 0 V; $V_{GS}$ = 20 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| | | $V_{DS}$ = 0 V; $V_{GS}$ = -20 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C; see Figure 11; see Figure 12 | - | - | 12 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 11; see Figure 12 | - | 5.1 | 6 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 44 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; see Figure 13 | - | 64 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 14 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 19 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 14 | - | 3825 | 5100 | pF |
| $C_{oss}$ | output capacitance | | - | 783 | 940 | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 235 | 322 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 30 V; $R_L$ = 1.2 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 10 Ω; $T_j$ = 25 °C | - | 30 | - | ns |
| $t_r$ | rise time | $V_{DS}$ = 30 V; $R_L$ = 1.2 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 10 Ω; $T_j$ = 30 °C | - | 46 | - | ns |
| $t_{d(off)}$ | turn-off delay time | $V_{DS}$ = 30 V; $R_L$ = 1.2 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 10 Ω; $T_j$ = 25 °C | - | 85 | - | ns |
| $t_f$ | fall time | | - | 39 | - | ns |
| $L_D$ | internal drain inductance | from drain lead 6 mm from package to centre of die; $T_j$ = 25 °C | - | 4.5 | - | nH |
| | | from upper edge of drain mounting base to centre of die; $T_j$ = 25 °C | - | 2.5 | - | nH |
| $L_S$ | internal source inductance | from source lead to source bond pad; $T_j$ = 25 °C | - | 7.5 | - | nH |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 15 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = -10 V; $V_{DS}$ = 30 V; $T_j$ = 25 °C | - | 73 | - | ns |
| $Q_r$ | recovered charge | | - | 82 | - | nC |



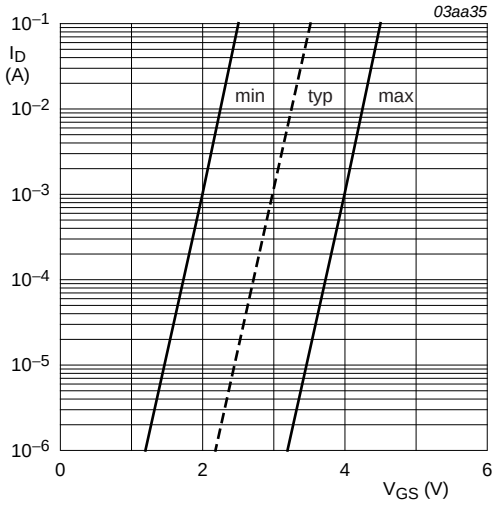

$T_j = 25°C; t_p = 300\mu s$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



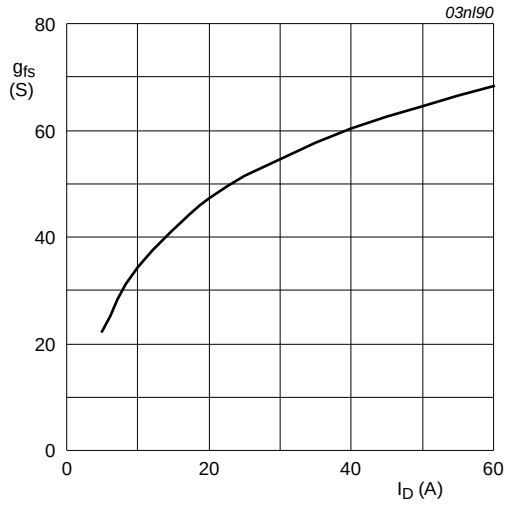

$T_j = 25°C; I_D = 25A$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



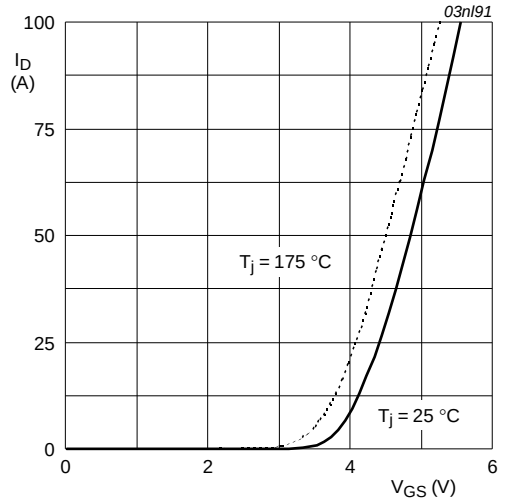

$T_j = 25°C; V_{DS} = 5V$

**Fig 7. Sub-threshold drain current as a function of gate-source voltage**



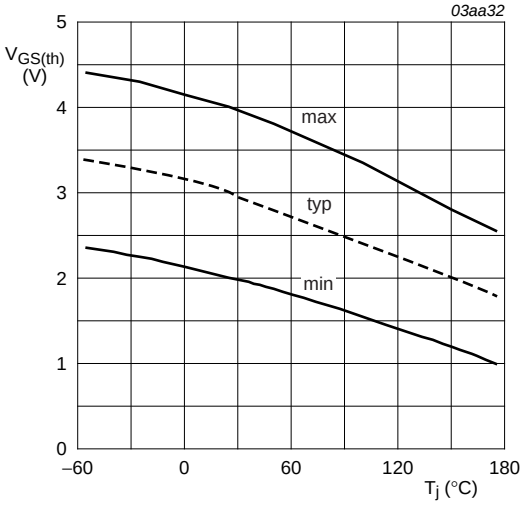

$T_j = 25°C; V_{DS} = 25V$

**Fig 8. Forward transconductance as a function of drain current; typical values**



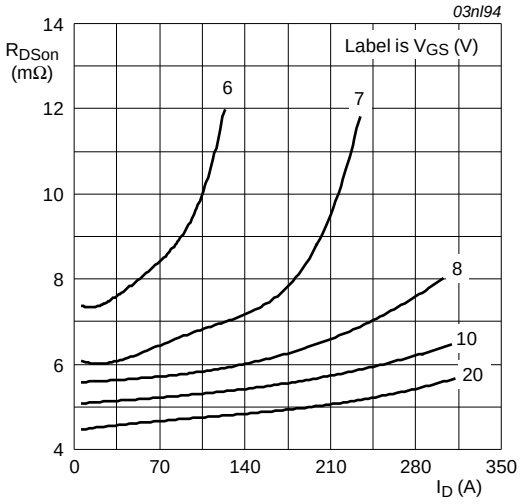

$V_{DS} = 25V$

**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



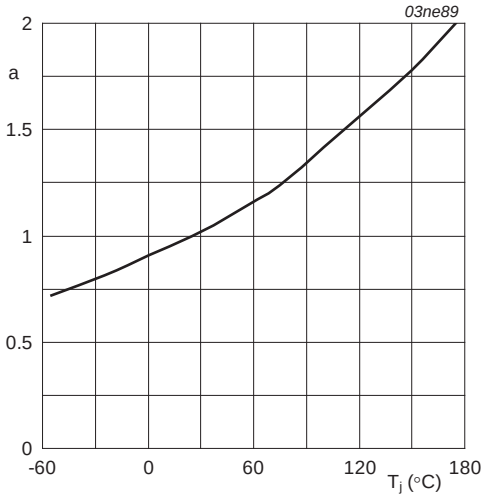

$I_D = 1mA; V_{DS} = V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**



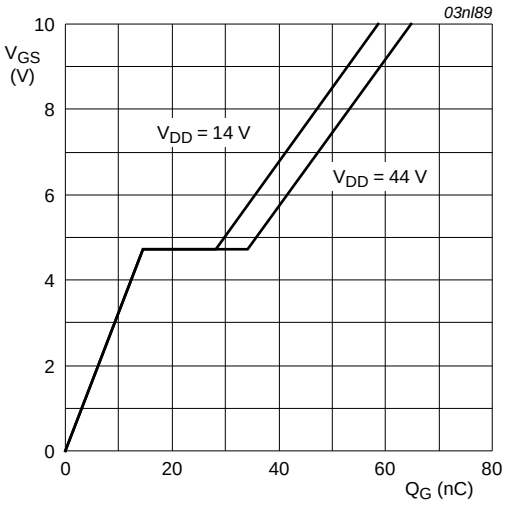

$T_j = 25°C$

**Fig 11. Drain-source on-state resistance as a function of drain current; typical values**



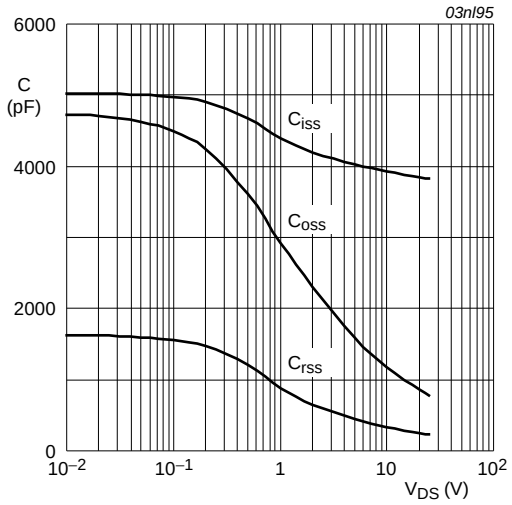

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**



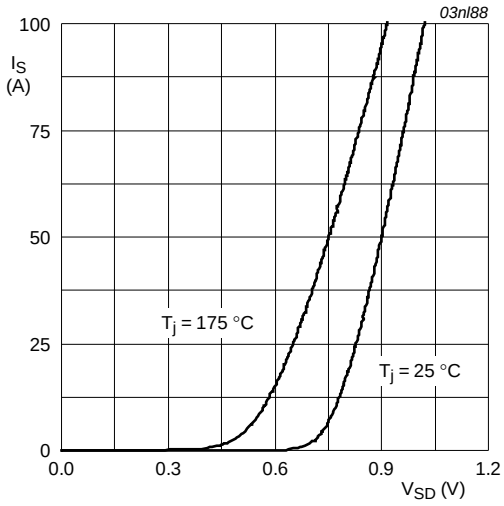

$T_j = 25°C; I_D = 25A$

**Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values**




$V_{GS} = 0V; f = 1MHz$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

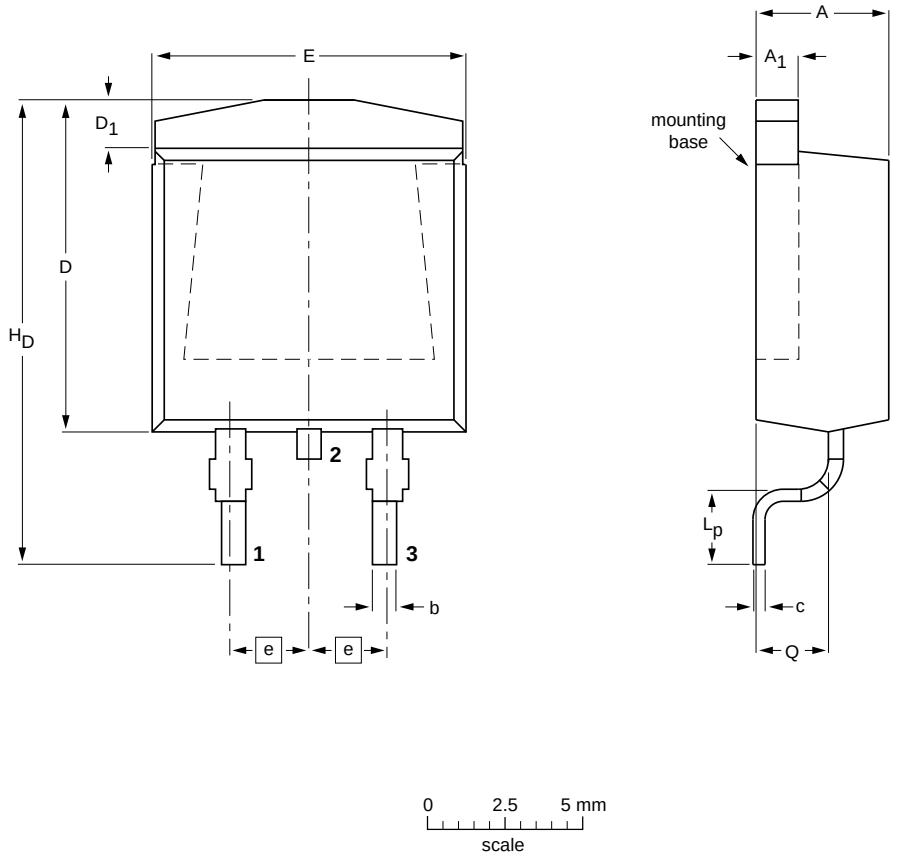



$V_{GS} = 0V$

**Fig 15. Source current as a function of source-drain voltage; typical values**

## 7. Package outline

**Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)** **SOT404**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | c | D max. | $D_1$ | E | e | $L_p$ | $H_D$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.50<br>4.10 | 1.40<br>1.27 | 0.85<br>0.60 | 0.64<br>0.46 | 11 | 1.60<br>1.20 | 10.30<br>9.70 | 2.54 | 2.90<br>2.10 | 15.80<br>14.80 | 2.60<br>2.20 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT404 | | | | | | ~~05-02-11~~<br>06-03-16 |

**Fig 16. Package outline SOT404 (D2PAK)**

## 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BUK7606-55B v.2 | 20100621 | Product data sheet | - | BUK75_7606_55B v.1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Type number BUK7606-55B separated from data sheet BUK75_7606_55B v.1. | | | |
| BUK75_7606_55B v.1 | 20030331 | Product data sheet | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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# 10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

## 11. Contents





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