



# BUK9629-100B

N-channel TrenchMOS logic level FET

Rev. 02 — 9 February 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	46	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	157	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$	-	22	27	mΩ
		$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 6</a> ; see <a href="#">Figure 7</a>	-	24	29	mΩ

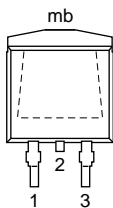
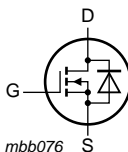


**Table 1. Quick reference data ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 46\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ }^\circ\text{C}$ ; unclamped	-	-	152	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 80\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 8</a>	-	13	-	nC

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;"><b>SOT404 (D2PAK)</b></p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

**Table 3. Ordering information**

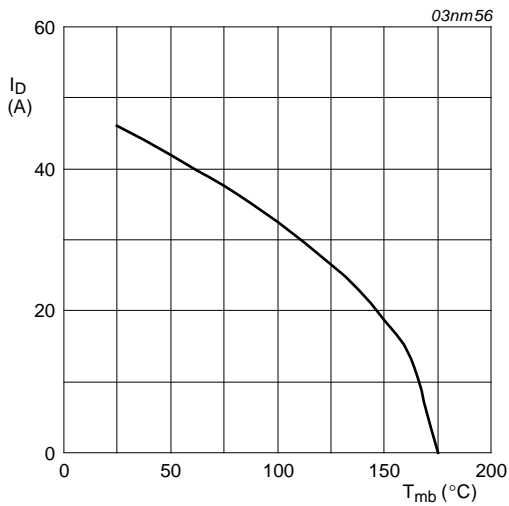
Type number	Package		Version
	Name	Description	
BUK9629-100B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

### 4. Limiting values

**Table 4. Limiting values**

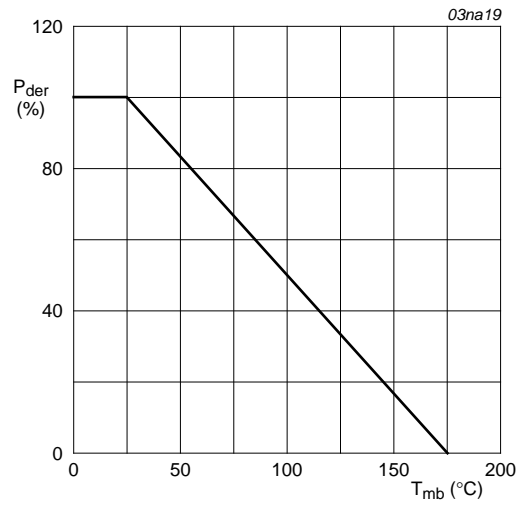
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	100	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ	-	100	V
V <sub>GS</sub>	gate-source voltage		-15	15	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	46	A
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; see <a href="#">Figure 1</a>	-	32	A
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; see <a href="#">Figure 3</a>	-	186	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	157	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	46	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	186	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 46 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped	-	152	mJ



$$V_{GS} \geq 5V$$

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**

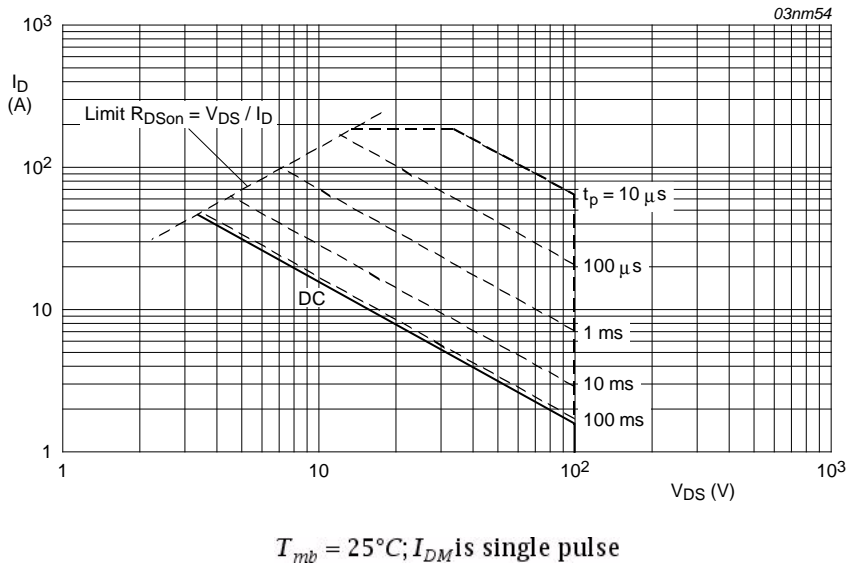


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W

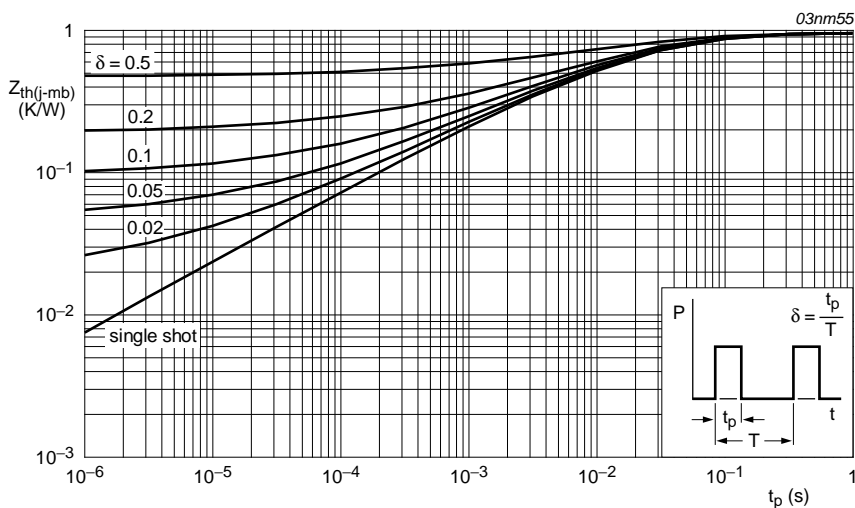


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

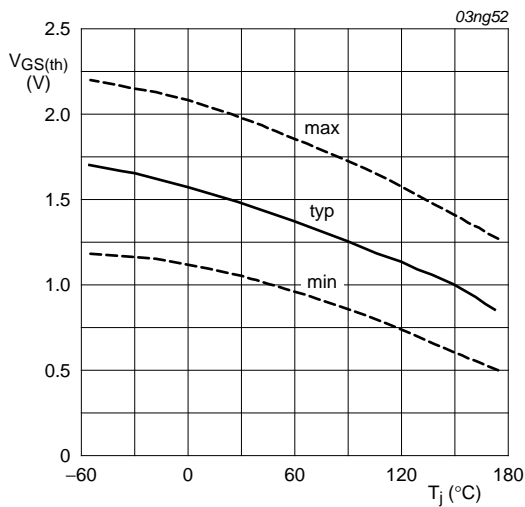
## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a>	1.1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a>	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	32	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 6</a> ; see <a href="#">Figure 7</a>	-	-	75	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	22	27	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 6</a> ; see <a href="#">Figure 7</a>	-	24	29	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a>	-	33	-	nC
$Q_{GS}$	gate-source charge		-	7	-	nC
$Q_{GD}$	gate-drain charge		-	13	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	-	3270	4360	pF
$C_{oss}$	output capacitance		-	236	283	pF
$C_{rss}$	reverse transfer capacitance		-	103	141	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	30	-	ns
$t_r$	rise time		-	86	-	ns
$t_{d(off)}$	turn-off delay time		-	96	-	ns
$t_f$	fall time		-	46	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH

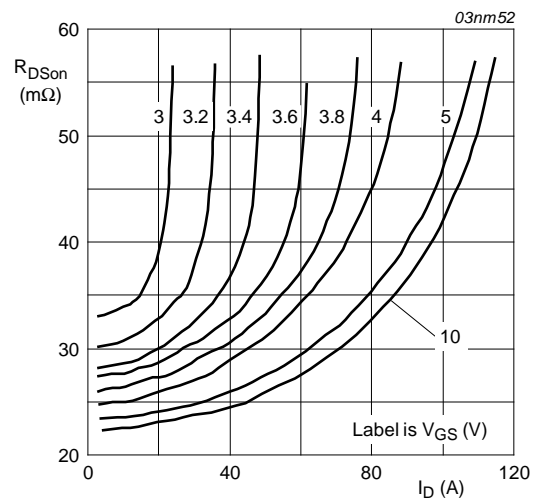
**Table 6. Characteristics ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 10</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	114	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	-	196	-	nC



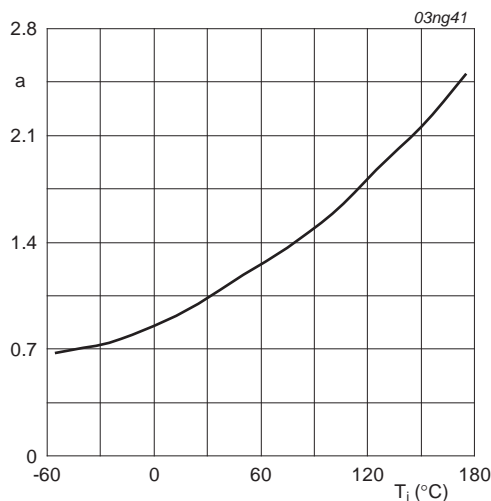
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

**Fig 5. Gate-source threshold voltage as a function of junction temperature**



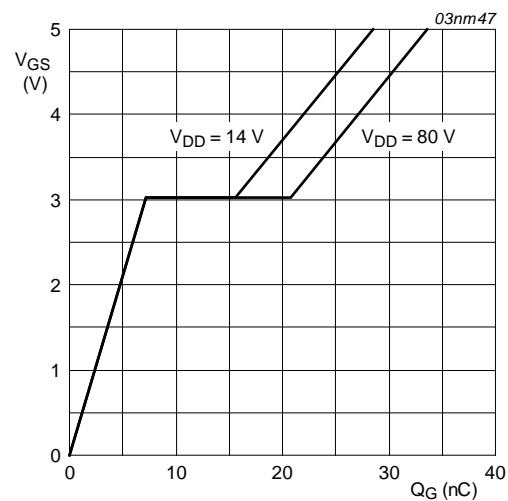
$$T_j = 25\text{ }^\circ\text{C}$$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



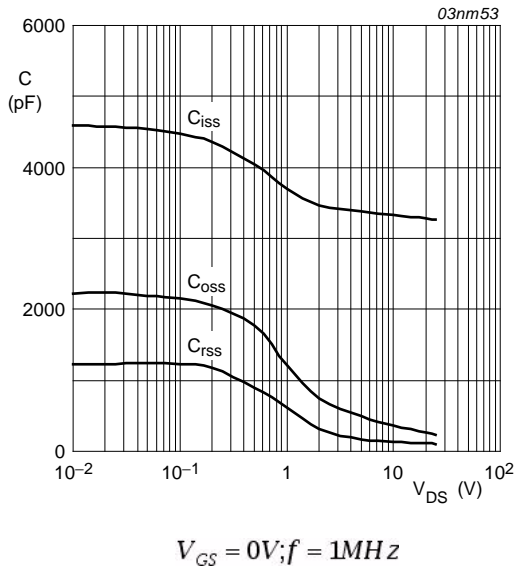
$$a = \frac{R_{DS(on)}}{R_{DS(on)25^\circ\text{C}}}$$

**Fig 7. Normalized drain-source on-state resistance factor as a function of junction temperature**

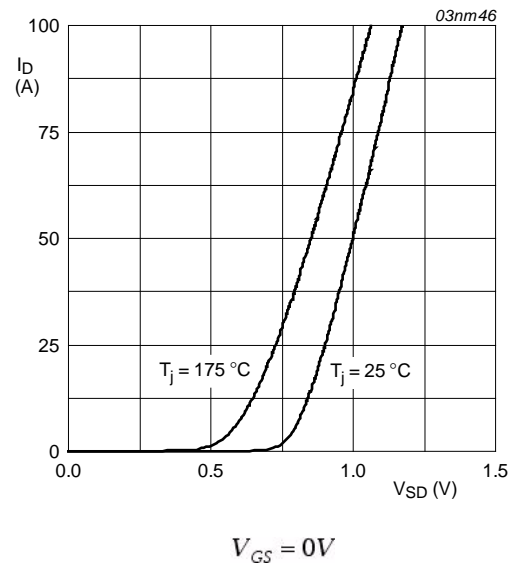


$$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$$

**Fig 8. Gate-source threshold voltage as a function of junction temperature**



**Fig 9. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

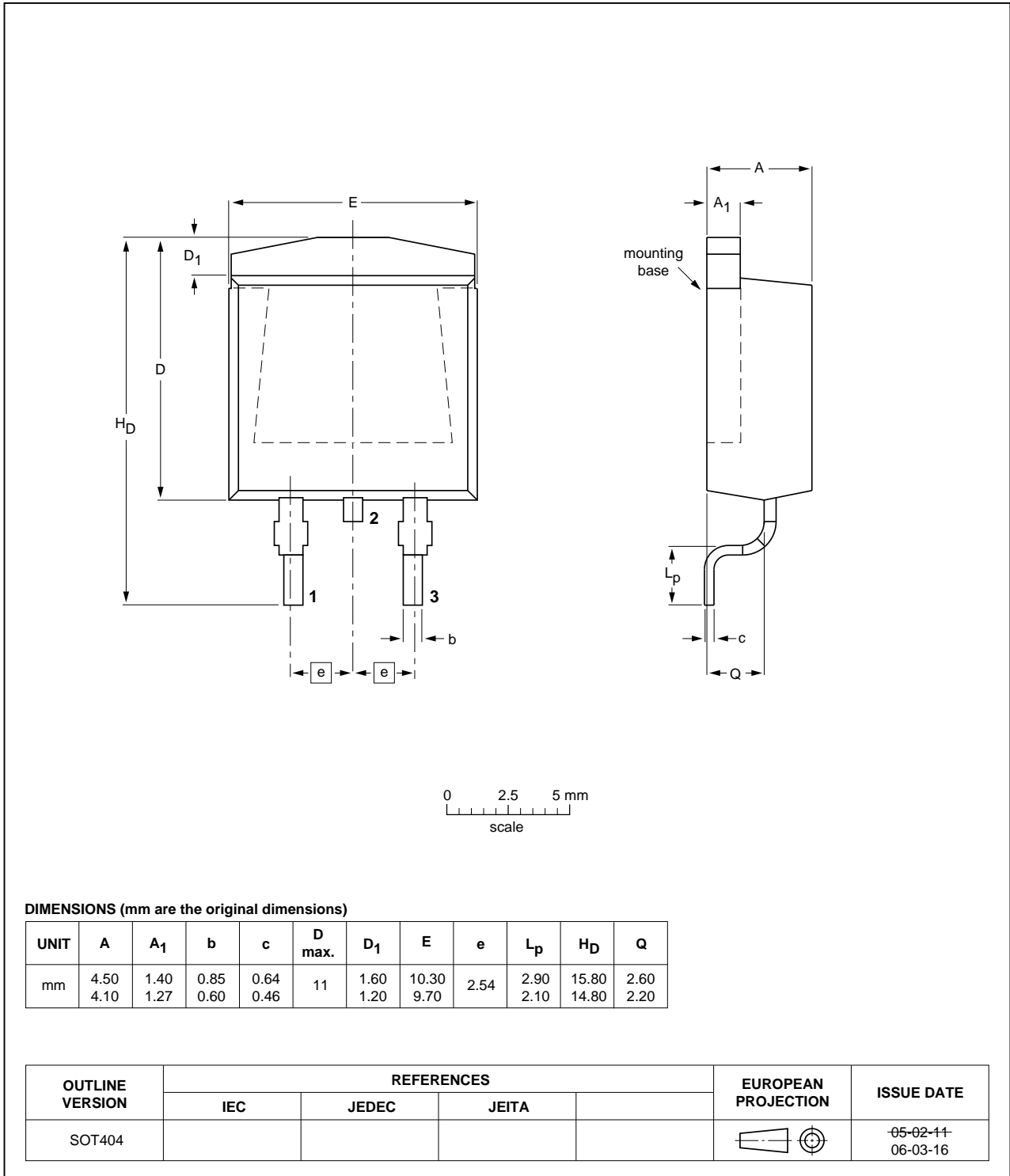


**Fig 10. Source current as a function of source-drain voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

**SOT404**



**Fig 11. Package outline SOT404 (D2PAK)**



## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9629-100B v.2	20110209	Product data sheet	-	BUK95_9629_100B v.1
Modifications:				
				<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number BUK9629-100B separated from data sheet BUK95_9629_100B v.1.</li></ul>
BUK95_9629_100B v.1 (9397 750 11249)	20030418	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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