



# NX3020NAKS

30 V, 180 mA dual N-channel Trench MOSFET

11 November 2013

Product data sheet

## 1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection
- Low threshold voltage

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	180	mA
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 100\text{ mA}; T_j = 25\text{ °C}$	-	2.7	4.5	$\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $1\text{ cm}^2$ .

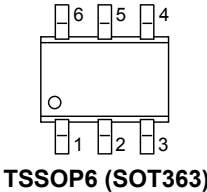
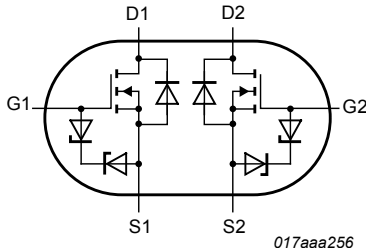


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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>TSSOP6 (SOT363)</p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3020NAKS	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

## 7. Marking

Table 4. Marking codes

Type number	Marking code
NX3020NAKS	Ua% [1]

[1] % = placeholder for manufacturing site code

## 8. Limiting values

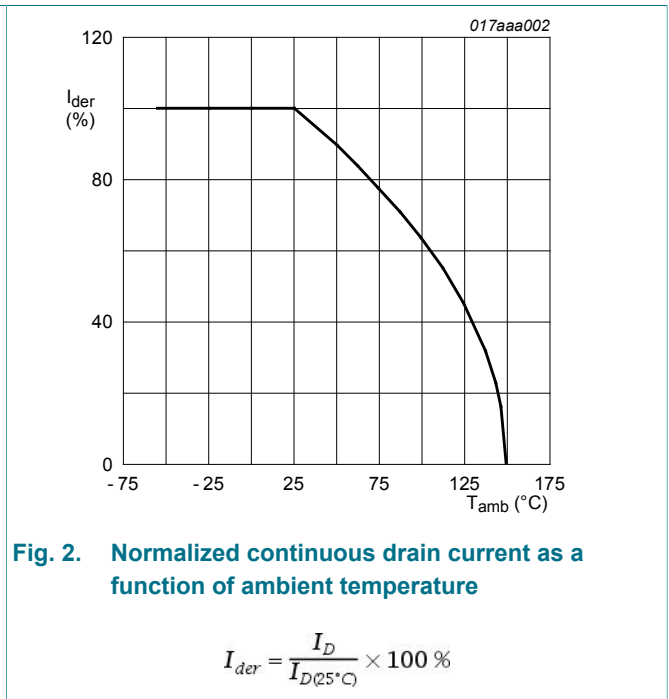
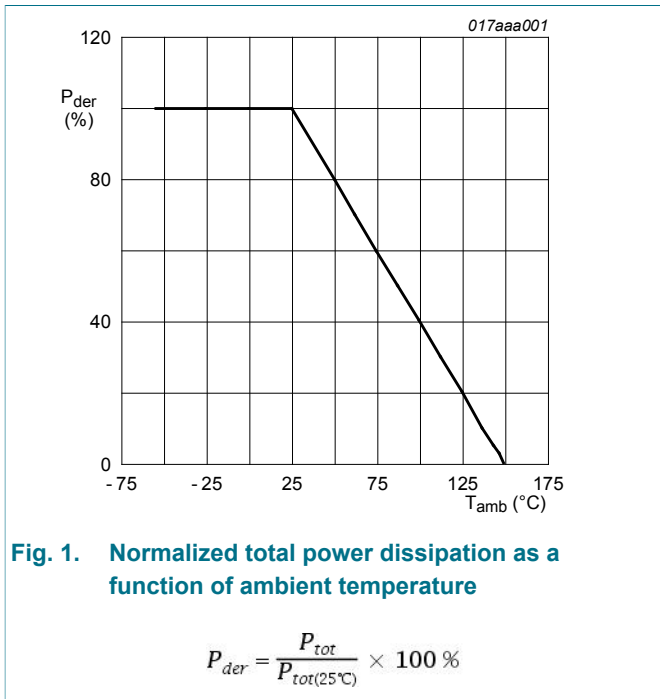
Table 5. Limiting values

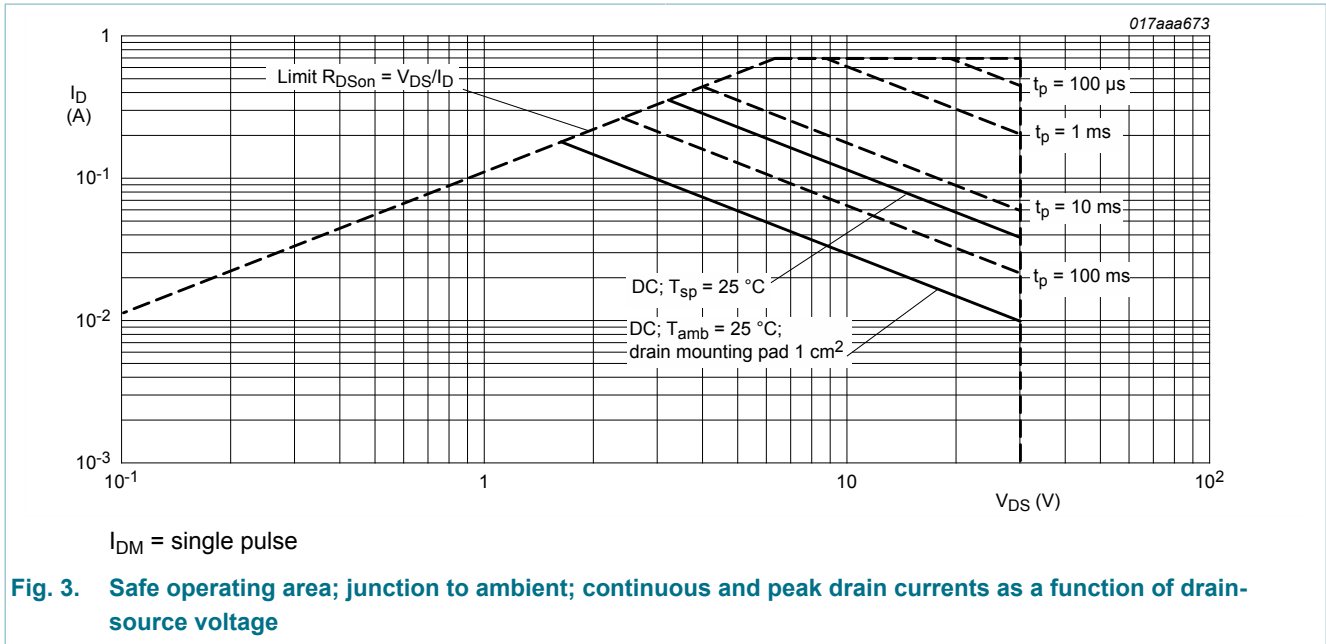
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor</b>					
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	180	mA
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	110	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$	-	720	mA
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	260	mW
			[1]	280	mW

Symbol	Parameter	Conditions		Min	Max	Unit
		T <sub>sp</sub> = 25 °C		-	1100	mW
<b>Source-drain diode</b>						
I <sub>s</sub>	source current	T <sub>amb</sub> = 25 °C		-	180	mA
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	375	mW
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	390	480	K/W
			[2]	-	380	430	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	110	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $1\text{ cm}^2$ .

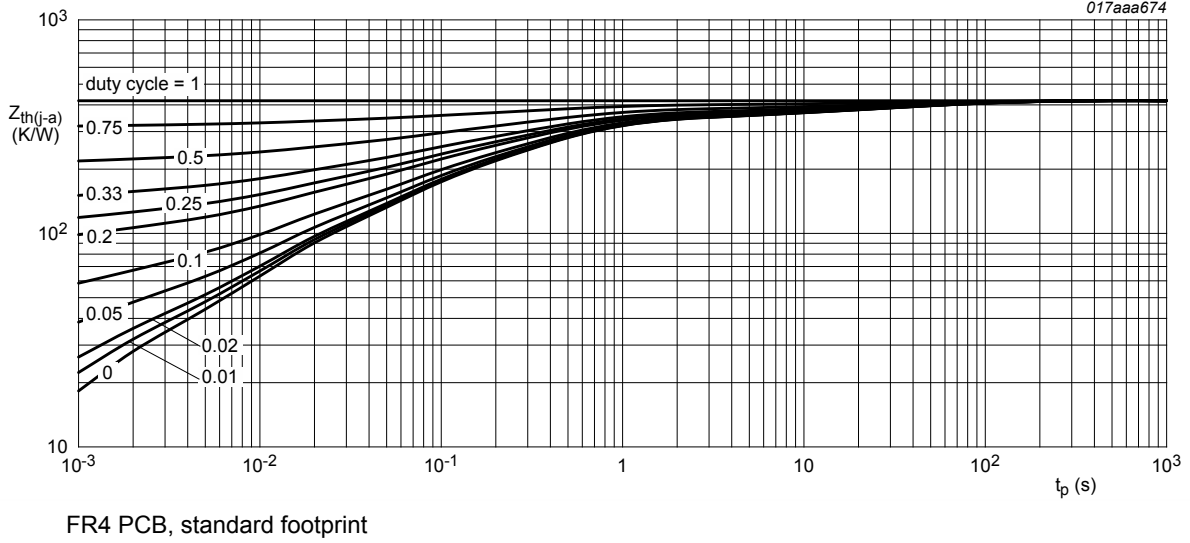


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

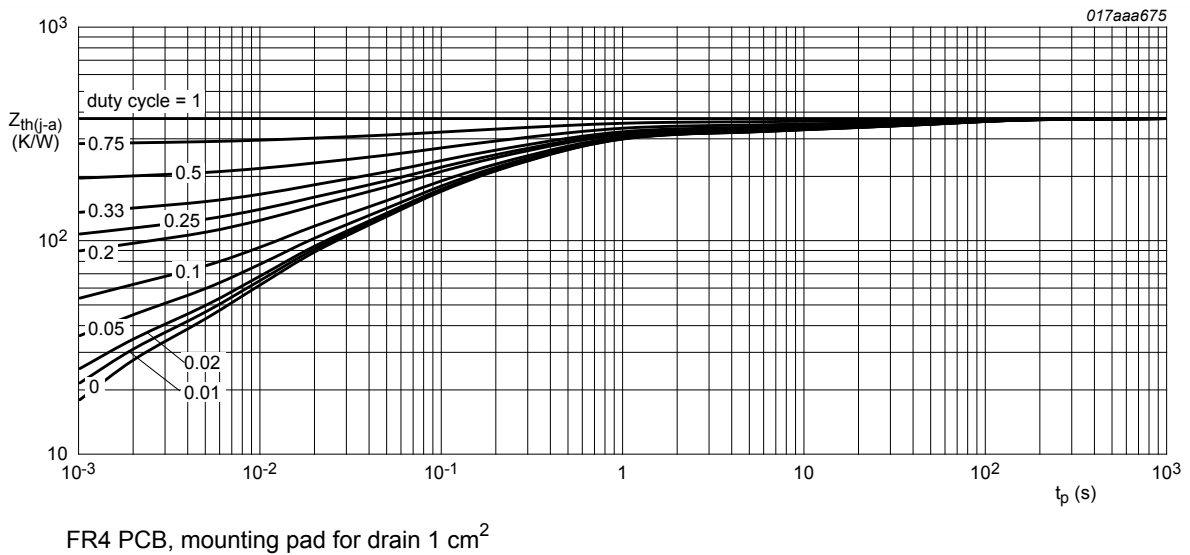
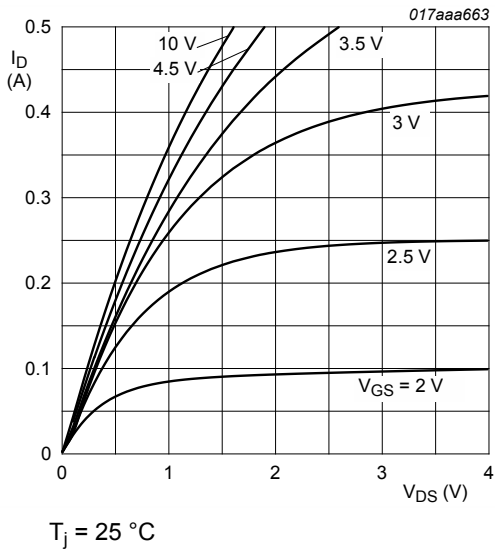


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

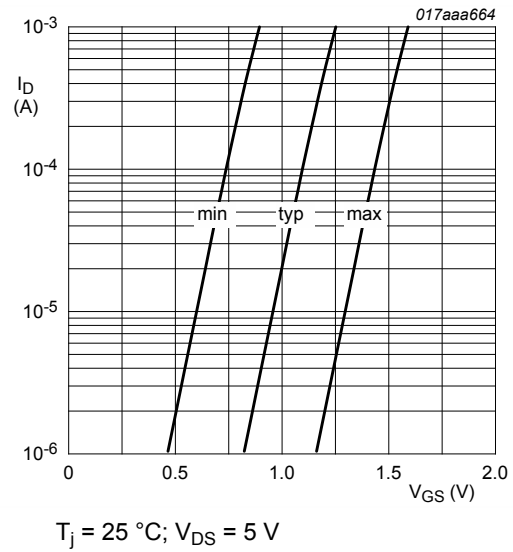
## 10. Characteristics

Table 7. Characteristics

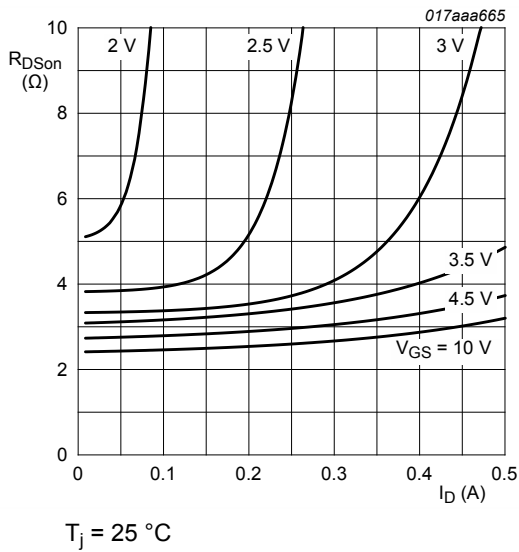
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$	0.8	1.2	1.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ C$	-	-	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	3.5	$\mu A$
		$V_{GS} = -20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	3.5	$\mu A$
		$V_{GS} = 10 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{GS} = -10 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{GS} = 4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	0.5	$\mu A$
		$V_{GS} = -4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	0.5	$\mu A$
		$V_{GS} = 10 V$ ; $I_D = 100 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	2.7	4.5	$\Omega$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V$ ; $I_D = 100 \text{ mA}$ ; $T_j = 150 \text{ }^\circ C$	-	5.5	9.2	$\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 100 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	3	5.2	$\Omega$
		$V_{GS} = 2.5 V$ ; $I_D = 10 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	4	13	$\Omega$
		$V_{GS} = 10 V$ ; $I_D = 150 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	320	-	mS
$g_{fs}$	forward transconductance	$V_{DS} = 10 V$ ; $I_D = 150 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	320	-	mS
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 V$ ; $I_D = 150 \text{ mA}$ ; $V_{GS} = 4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.34	0.44	nC
$Q_{GS}$	gate-source charge	$V_{DS} = 15 V$ ; $I_D = 150 \text{ mA}$ ; $V_{GS} = 4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.11	-	nC
$Q_{GD}$	gate-drain charge		-	0.06	-	nC
$C_{iss}$	input capacitance		$V_{DS} = 10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	13	20
$C_{oss}$	output capacitance	$V_{DS} = 10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	2.6	-	pF
$C_{rss}$	reverse transfer capacitance		-	1.1	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 20 V$ ; $R_L = 250 \Omega$ ; $V_{GS} = 10 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	5	10
$t_r$	rise time	$V_{DS} = 20 V$ ; $R_L = 250 \Omega$ ; $V_{GS} = 10 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	34	68	ns
$t_f$	fall time		-	17	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = 115 \text{ mA}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	0.47	0.7	1.2	V



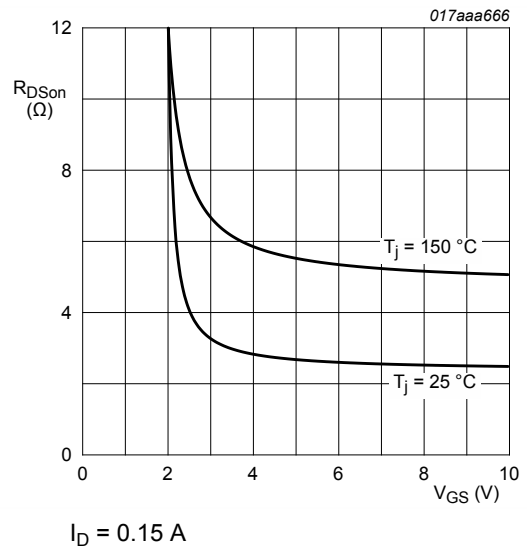
**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



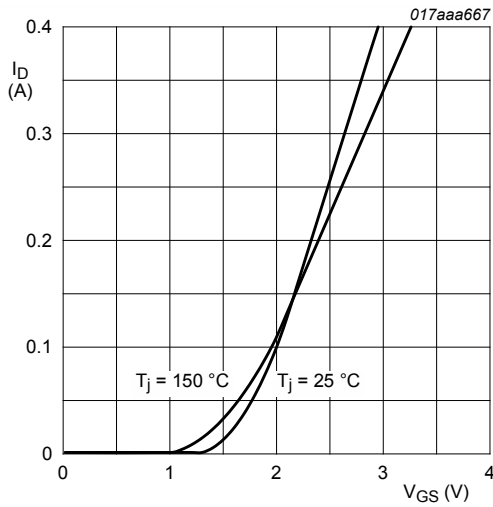
**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**



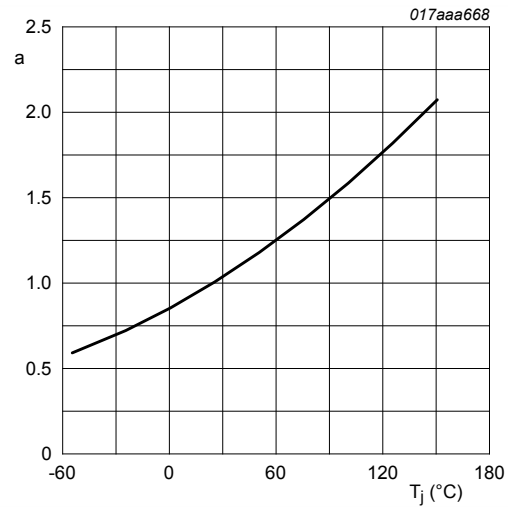
**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**

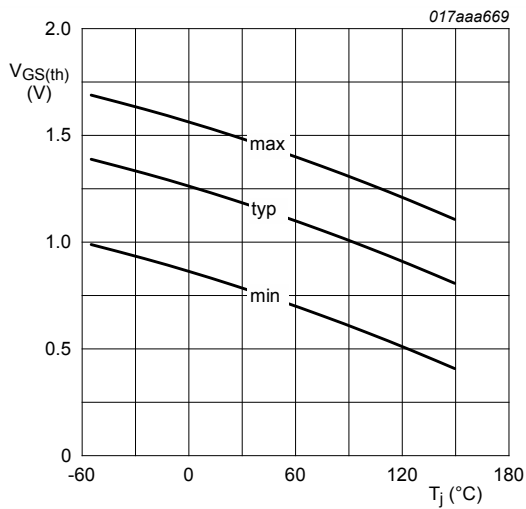


**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



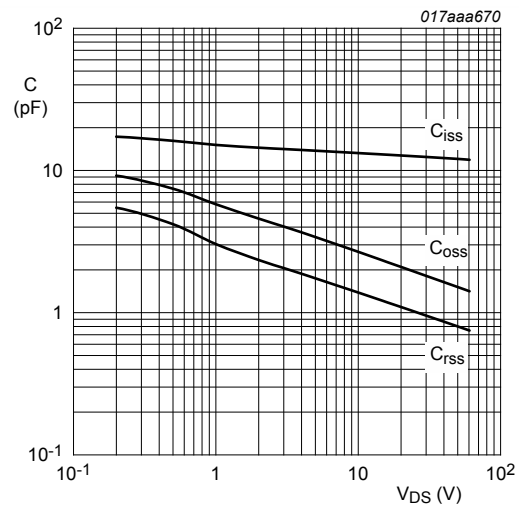
**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$



**Fig. 12. Gate-source threshold voltage as a function of junction temperature**

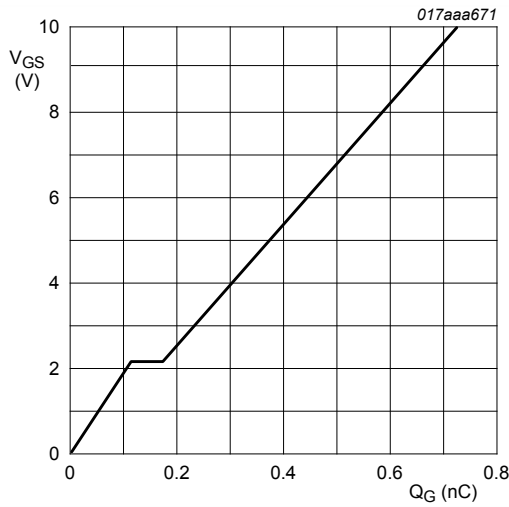
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$



**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$



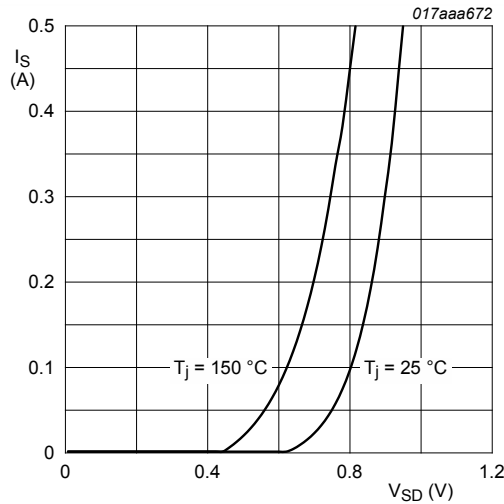


$I_D = 0.15$  A;  $V_{DS} = 15$  V;  $T_{amb} = 25$  °C

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



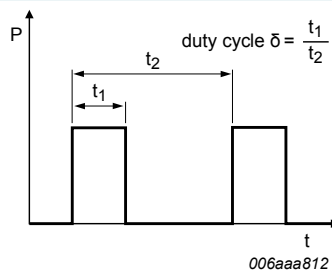
**Fig. 15. Gate charge waveform definitions**



$V_{GS} = 0$  V

**Fig. 16. Source current as a function of source-drain voltage; typical values**

## 11. Test information



**Fig. 17. Duty cycle definition**

12. Package outline

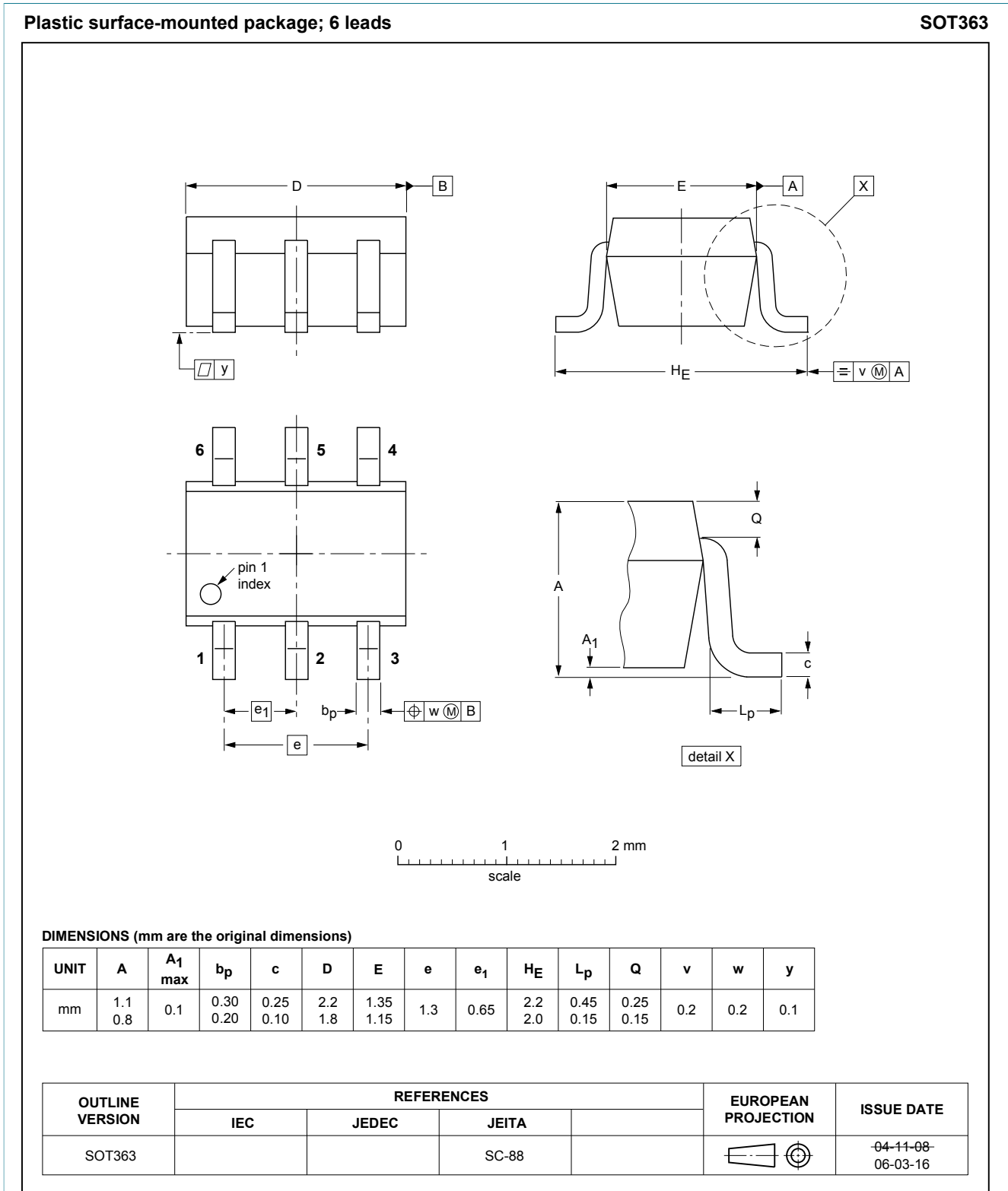


Fig. 18. Package outline TSSOP6 (SOT363)

### 13. Soldering

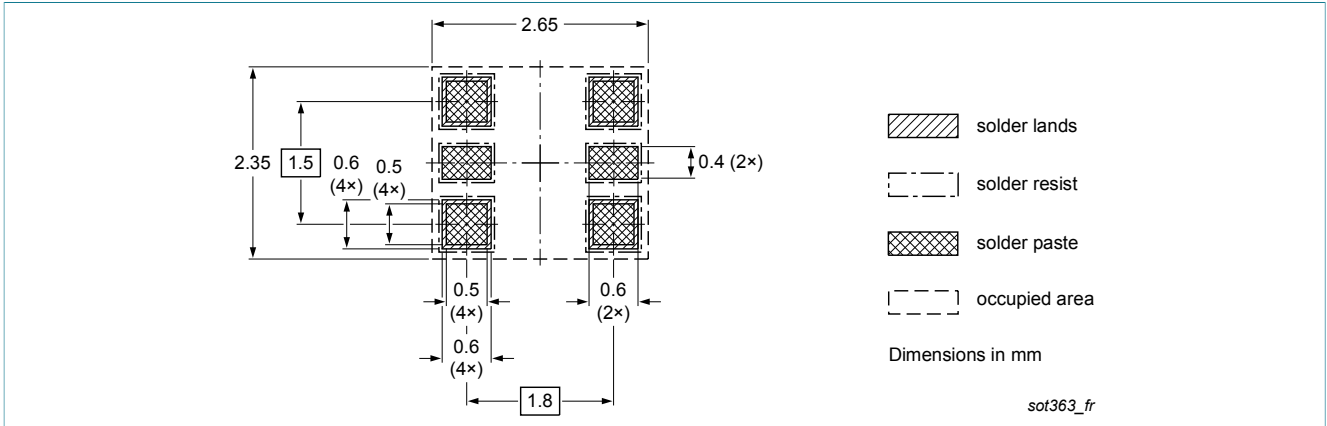


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

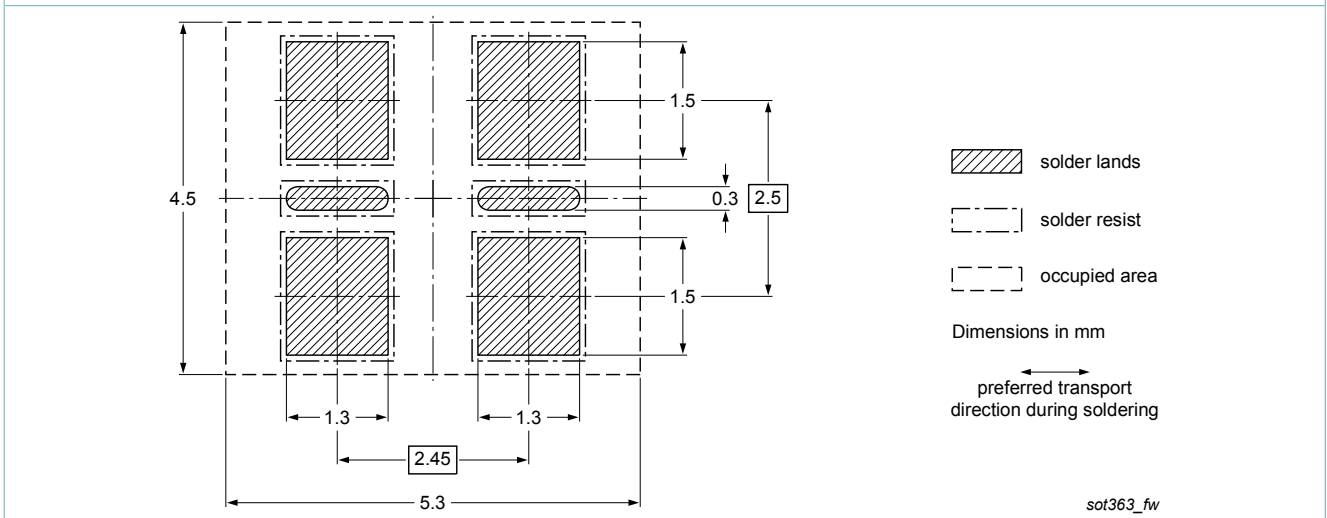


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX3020NAKS v.3	20131111	Product data sheet	-	NX3020NAKS v.2
Modifications:	<ul style="list-style-type: none"><li>Marking code corrected</li></ul>			
NX3020NAKS v.2	20131029	Product data sheet	-	NX3020NAKS v.1
NX3020NAKS v.1	20120706	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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 Date of release: 11 November 2013