



PMC85XP

30 V P-channel MOSFET with pre-biased NPN transistor

15 May 2013

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in Trench MOSFET technology and NPN Resistor-Equipped Transistor (RET) together in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Trench MOSFET technology
- NPN transistor built-in bias resistors
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

3. Applications

- Charging switch for portable devices
- High-side load switch
- USB port overvoltage protection
- Power management in battery-driven portables
- Hard disk and computing power management

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P-channel Trench MOSFET						
V_{DS}	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	-30	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $t \leq 5\text{ s}$	[1]	-	-3.4	A
P-channel Trench MOSFET; static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$; $I_D = -2.6\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$	-	85	110	m Ω
NPN RET						
V_{CEO}	collector-emitter voltage	$T_{amb} = 25\text{ }^\circ\text{C}$; open base	-	-	50	V
I_o	output current		-	-	100	mA



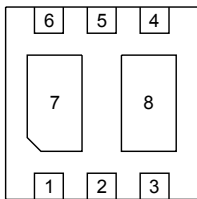
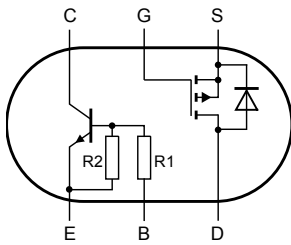
30 V P-channel MOSFET with pre-biased NPN transistor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NPN RET						
R1	bias resistor 1		3.3	4.7	6.1	kΩ
R2	bias resistor 2		-	47	-	kΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm²

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E	emitter	 <p>Transparent top view DFN2020-6 (SOT1118)</p>	 <p>017aaa396</p>
2	B	base		
3	D	drain		
4	S	source		
5	G	gate		
6	C	collector		
7	C	collector		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMC85XP	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

7. Marking

Table 4. Marking codes

Type number	Marking code
PMC85XP	1K

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P-channel Trench MOSFET						
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-3.4	A
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-2.6	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-1.6	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-8	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	485	mW
			[1]	-	1170	mW
		T _{sp} = 25 °C	[2]	-	8300	mW
P-channel Trench MOSFET; source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.2	A
NPN RET						
V _{CBO}	collector-base voltage	T _{amb} = 25 °C; open emitter		-	50	V
V _{CEO}	collector-emitter voltage	T _{amb} = 25 °C; open base		-	50	V
V _{EBO}	emitter-base voltage	T _{amb} = 25 °C; open collector		-	10	V
V _I	input voltage	positive		-	30	V
		negative		-	-5	V
I _O	output current			-	100	mA
I _{CM}	peak collector current			-	100	mA
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	465	mW
			[1]	-	985	mW
		T _{sp} = 25 °C	[2]	-	4160	mW
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm²
 [2] Device mounted on an FR4 PCB, single-sided copper; tin-plated and standard footprint.



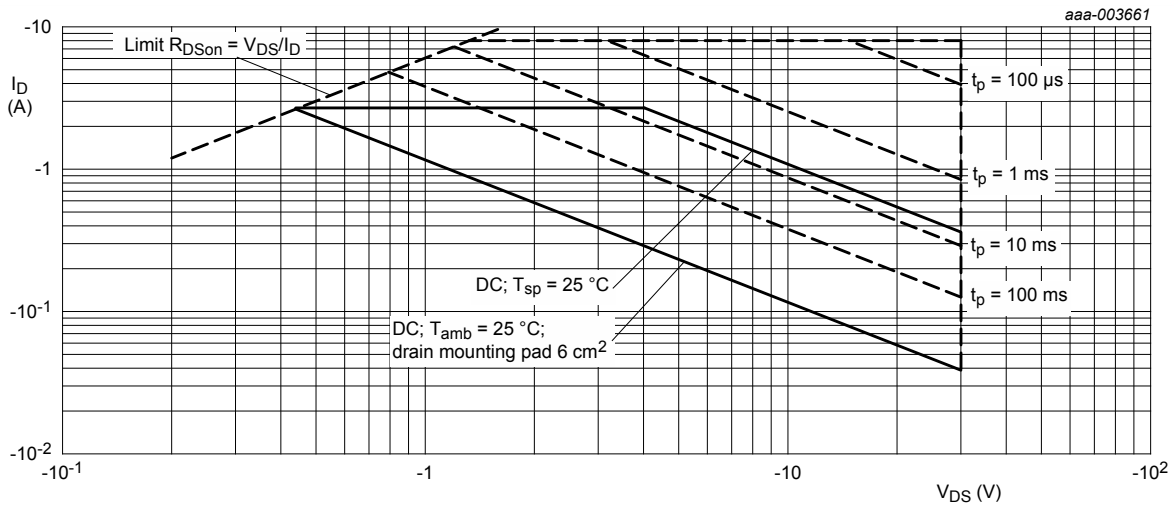
Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$



Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$



I_{DM} = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

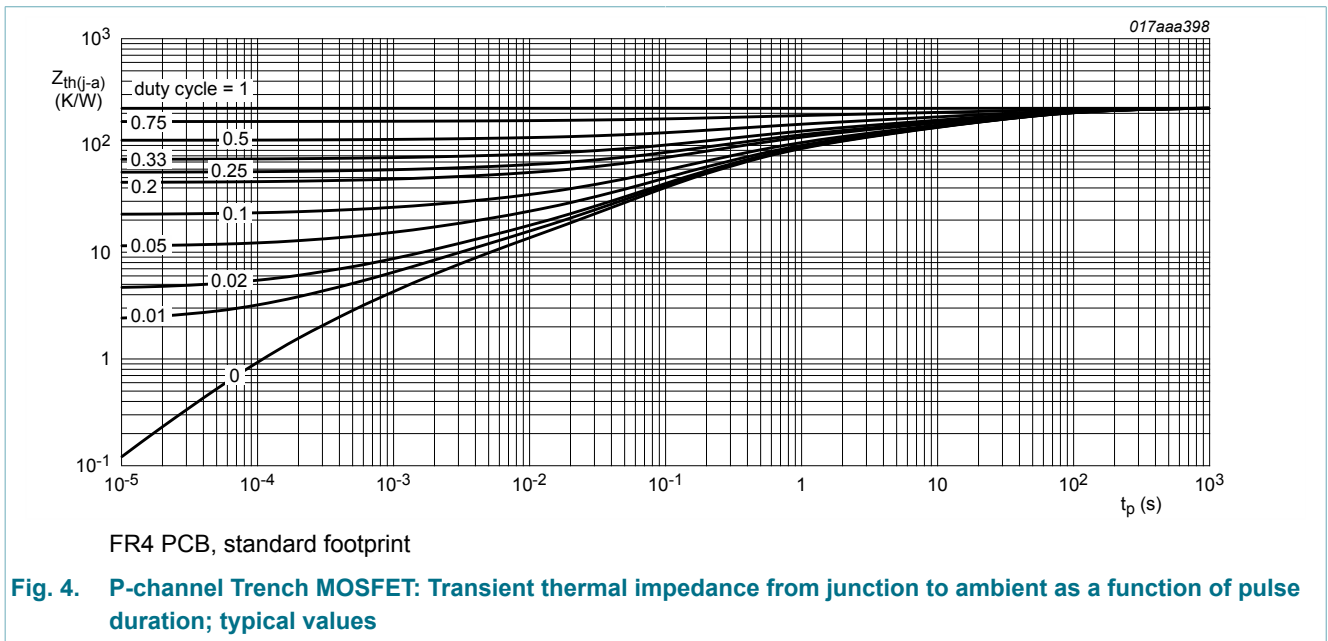
Table 6. Thermal characteristics

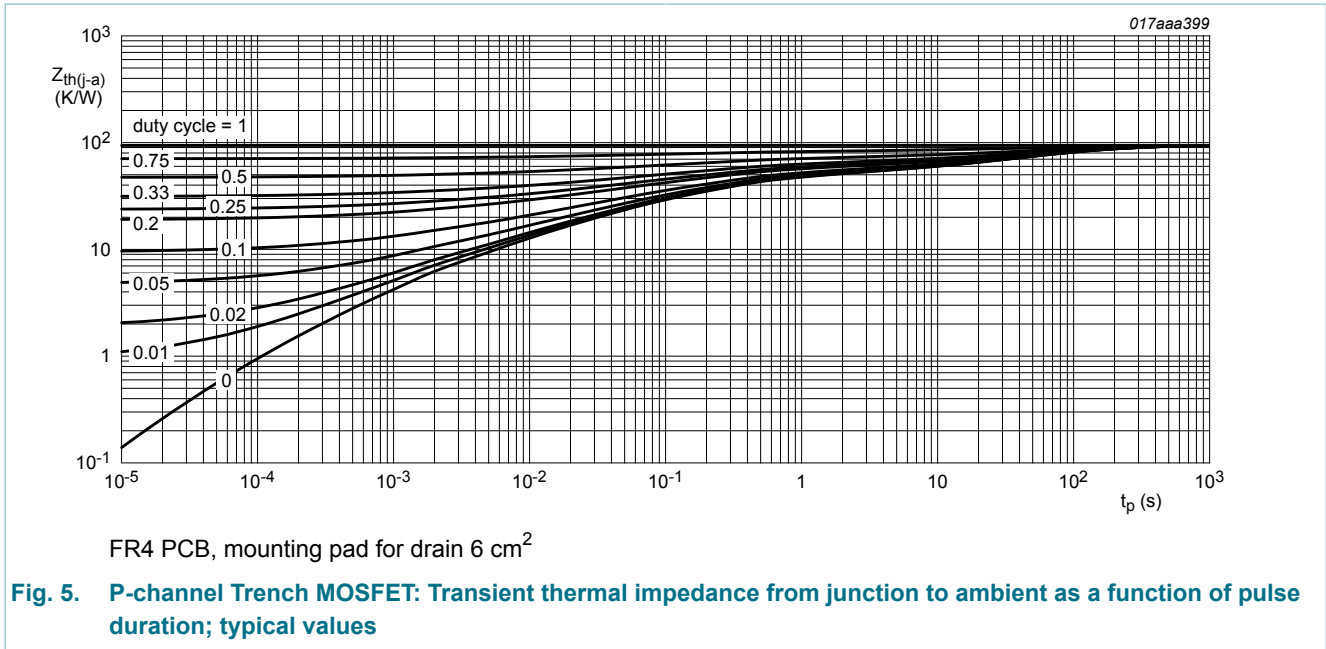
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
P-channel Trench MOSFET							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	223	256	K/W
			[2]	-	93	107	K/W
		t ≤ 5 s; in free air	[2]	-	55	63	K/W

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	10	15	K/W	
NPN RET							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	233	270	K/W
			[2]	-	110	127	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	25	30	K/W	

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm²





10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P-channel Trench MOSFET; static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 mA; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.45	-0.78	-1	V
I_{DSS}	drain leakage current	$V_{DS} = -30 V; V_{GS} = 0 V; T_{amb} = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{DS} = -30 V; V_{GS} = 0 V; T_{amb} = 150 \text{ }^\circ C$	-	-	-11	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -2.6 A; T_j = 25 \text{ }^\circ C$	-	85	110	m Ω
		$V_{GS} = -4.5 V; I_D = -2.6 A; T_j = 150 \text{ }^\circ C$	-	133	173	m Ω
		$V_{GS} = -2.5 V; I_D = -1.5 A; T_j = 25 \text{ }^\circ C$	-	105	140	m Ω
g_{fs}	transfer conductance	$V_{DS} = -10 V; I_D = -2.6 A; T_j = 25 \text{ }^\circ C$	-	10	-	S
P-channel Trench MOSFET; dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15 V; I_D = -2.6 A; V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	5.2	7.8	nC
Q_{GS}	gate-source charge		-	1.1	-	nC
Q_{GD}	gate-drain charge		-	0.95	-	nC
C_{iss}	input capacitance	$V_{DS} = -15 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	680	-	pF
C_{oss}	output capacitance		-	54	-	pF

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rSS}	reverse transfer capacitance		-	40	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15\text{ V}; I_D = -2.6\text{ A}; R_{G(ext)} = 6\ \Omega;$ $V_{GS} = -4.5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	3	-	ns
t_r	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	112	-	ns
t_f	fall time		-	48	-	ns
P-channel Trench MOSFET; source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1.2\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-0.8	-1.2	V
NPN RET						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	-	170	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; T_j = 25\text{ }^\circ\text{C}$	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}; T_j = 25\text{ }^\circ\text{C}$	-	-	100	mV
$V_{I(off)}$	off-state input voltage	$I_C = 100\ \mu\text{A}; V_{CE} = 5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.6	0.5	V
$V_{I(on)}$	on-state input voltage	$I_C = 5\text{ mA}; V_{CE} = 0.3\text{ V}; T_j = 25\text{ }^\circ\text{C}$	1.3	0.9	-	V
R1	bias resistor 1		3.3	4.7	6.1	k Ω
R2	bias resistor 2		-	47	-	k Ω
R2/R1	bias resistor ratio		8	10	12	
C_C	collector capacitance	$I_E = 0\text{ A}; i_e = 0\text{ A}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ $V_{CB} = 10\text{ V}$	-	-	2.5	pF

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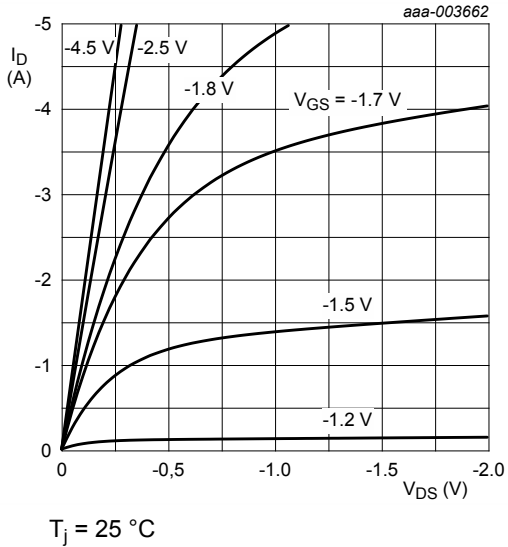


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

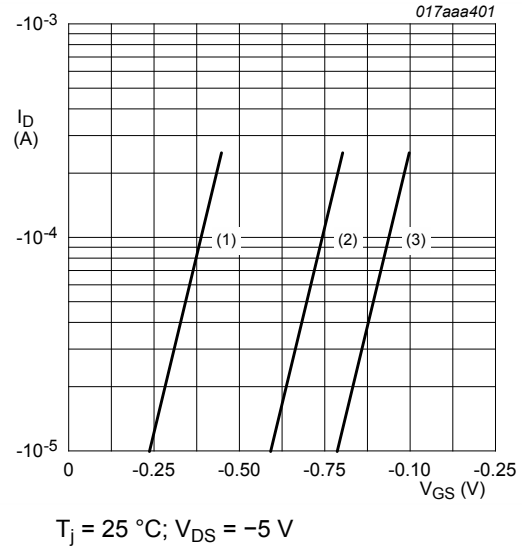


Fig. 7. Subthreshold drain current as a function of gate-source voltage

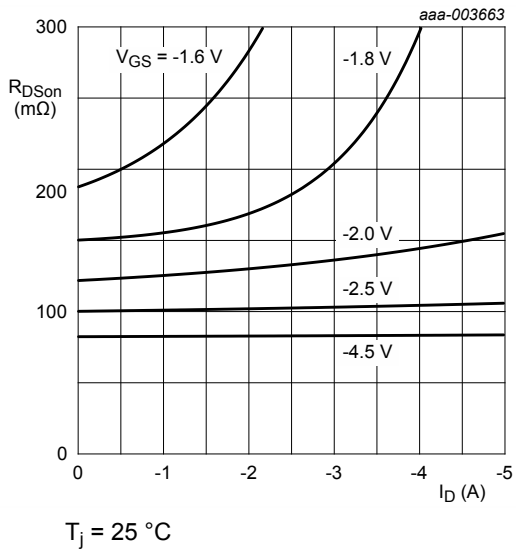


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

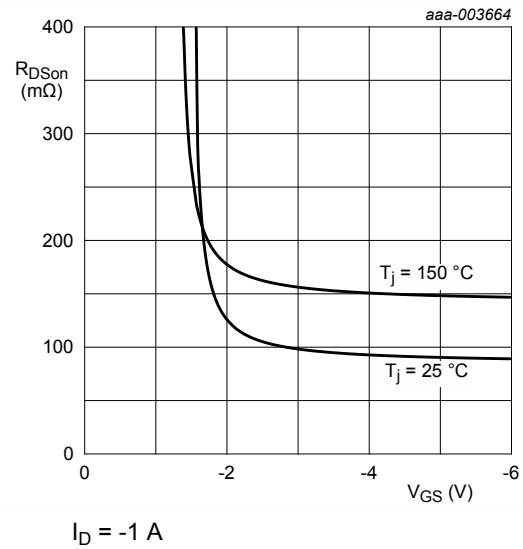
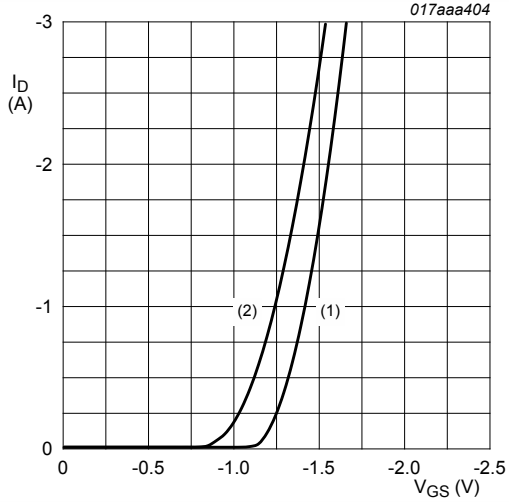


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

30 V P-channel MOSFET with pre-biased NPN transistor



$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ }^\circ\text{C}$
 (2) $T_j = 150\text{ }^\circ\text{C}$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

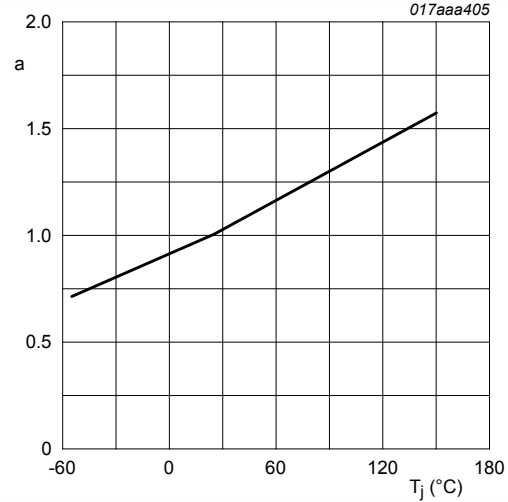
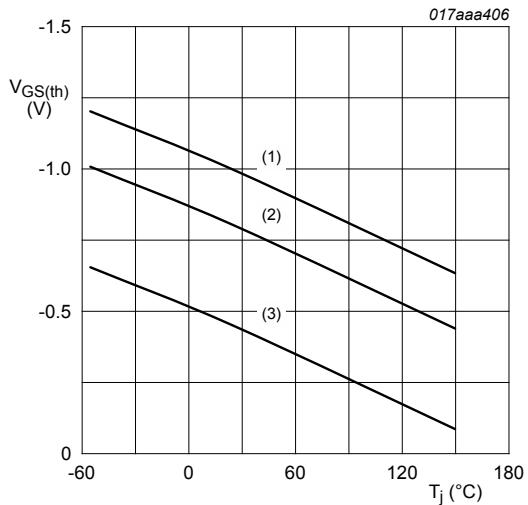


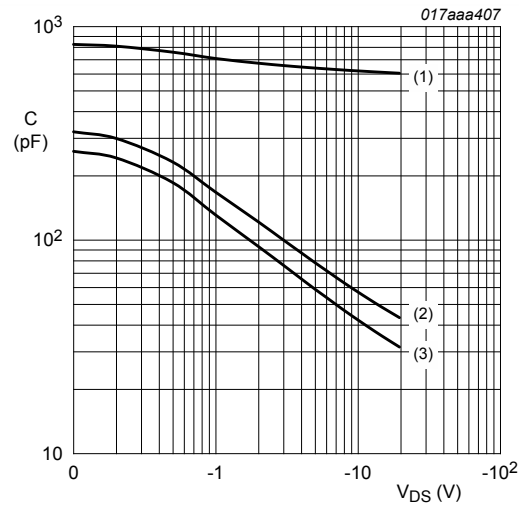
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$



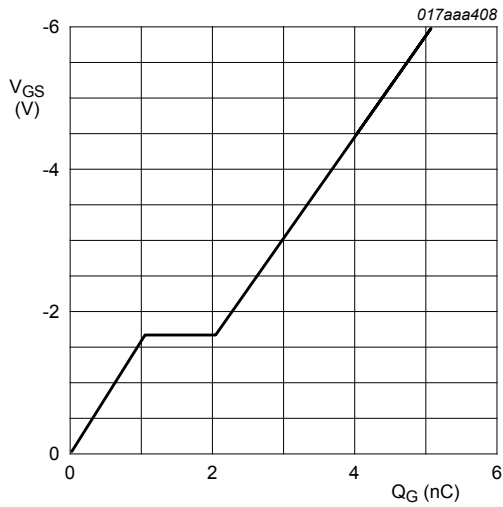
$I_D = -0.25\text{ mA}$; $V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}$; $V_{GS} = 0\text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -3.3 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

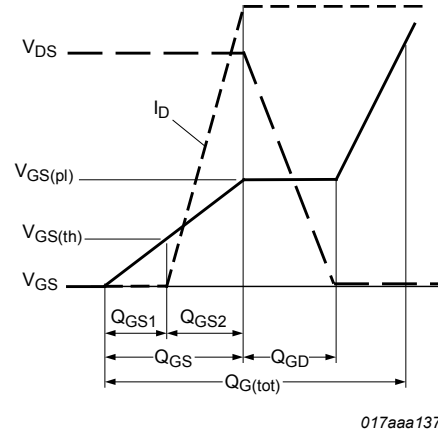
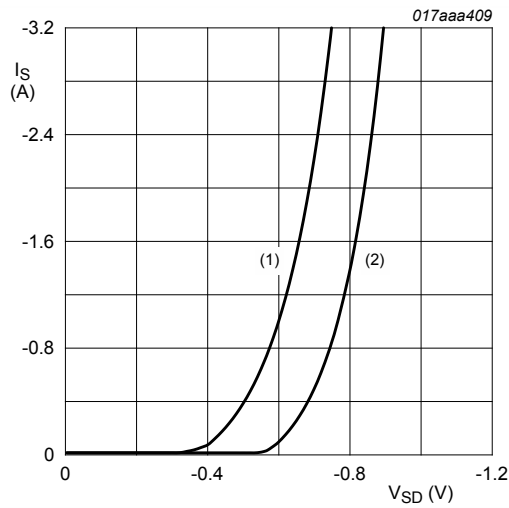


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$
 (1) $T_{amb} = 150 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

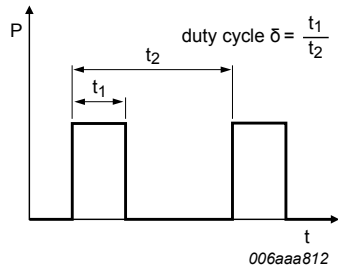


Fig. 17. Duty cycle definition

12. Package outline

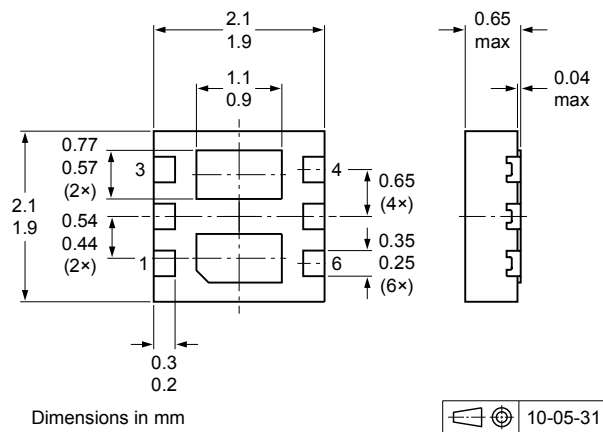


Fig. 18. Package outline DFN2020-6 (SOT1118)

13. Soldering

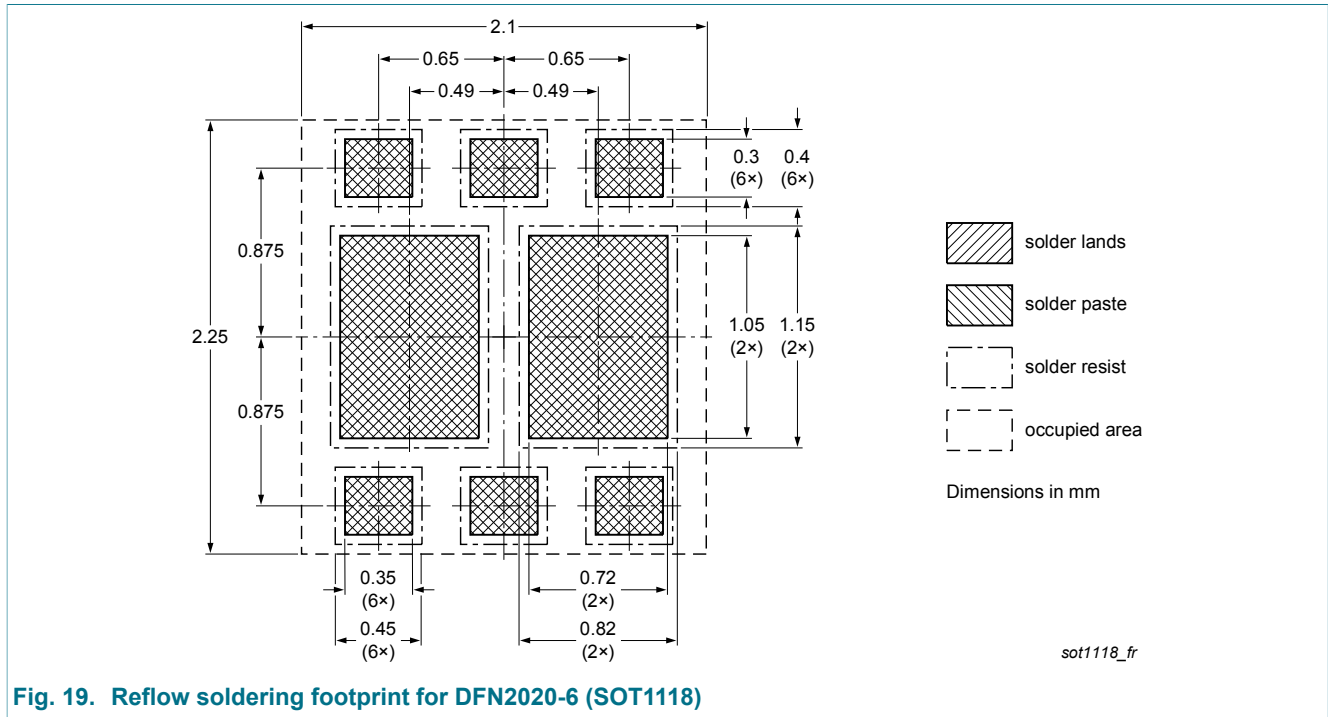


Fig. 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMC85XP v.2	20130515	Product data sheet	-	PMC85XP v.1
Modifications:	<ul style="list-style-type: none"> Pinning information: graphic symbol corrected 			
PMC85XP v.1	20120524	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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