# PMPB29XPE

# 20 V, single P-channel Trench MOSFET 5 December 2012

**Product data sheet** 

## **Product profile**

#### 1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

#### 1.2 Features and benefits

- 2.3 kV ESD protected
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated 100 % solderable side pads for optical solder inspection

#### 1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portable devices
- Hard disk and computing power management

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	-20	V
V <sub>GS</sub>	gate-source voltage			-12	-	12	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-	-5	Α
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = -4.5 V; $I_D$ = -5 A; $T_j$ = 25 °C		-	28	32.5	mΩ

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.





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## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	1 6	D I
2	D	drain	7 7	
3	G	gate		$G \left( \begin{array}{c} \Psi \\ \overline{\Psi} \end{array} \right)$
4	S	source	3 8 4	
5	D	drain	Transparent top view	
6	D	drain	DFN2020MD-6 (SOT1220)	S 017aaa259
7	D	drain		
8	S	source		

# 3. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMPB29XPE	DFN2020MD-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220			

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PMPB29XPE	1T

# 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-20	V
$V_{GS}$	gate-source voltage			-12	12	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-5	Α
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-3.2	Α
I <sub>DM</sub>	peak drain current	$T_{amb}$ = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-12	Α
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[1]	-	1.7	W
		T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	3.5	W
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Symbol	Parameter	Conditions		Min	Max	Unit
		T <sub>sp</sub> = 25 °C		-	12.5	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
Source-drai	in diode					
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1.8	Α
ESD maxim	um rating		,		,	,
V <sub>ESD</sub>	electrostatic discharge voltage	НВМ	[2]	-	2300	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Measured between all pins.

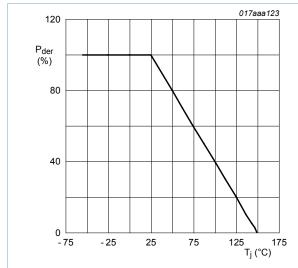


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

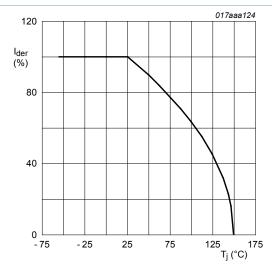


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

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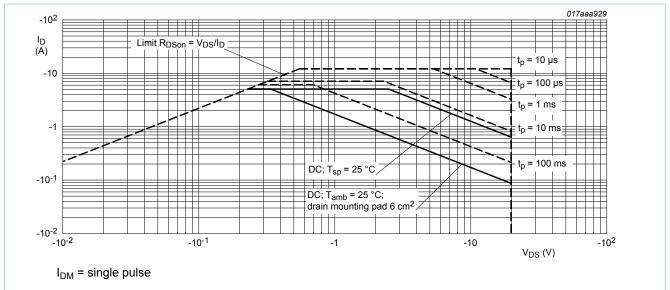


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drainsource voltage

#### Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R <sub>th(j-a)</sub> thermal resistance from junction to ambient		in free air	[1]	-	235	270	K/W
	-		[2]	-	67	74	K/W
	ambient	in free air; t ≤ 5 s	[2]	-	33	36	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			_	5	10	K/W

- Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

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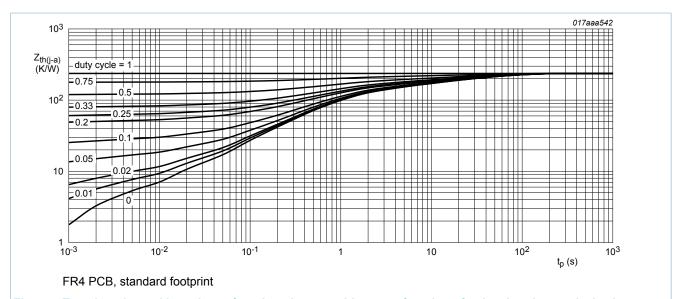


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

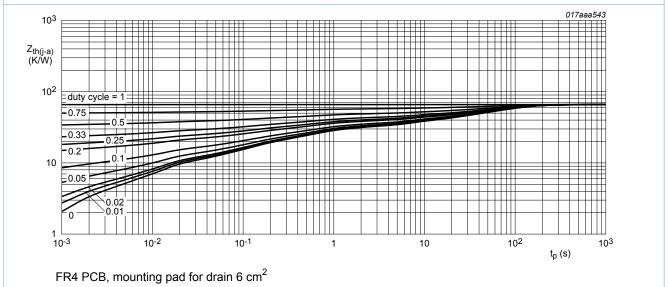


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

#### 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
Static chara	Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 °C$		-20	-	-	V	
V <sub>GSth</sub>	gate-source threshold voltage	$I_D$ = -250 $\mu$ A; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 25 °C		-0.47	-0.68	-0.9	V	
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA	
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = -8 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C		-	-	-10	μΑ	
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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	-	10	μA
R <sub>DSon</sub>	drain-source on-state	$V_{GS}$ = -4.5 V; $I_D$ = -5 A; $T_j$ = 25 °C	-	28	32.5	mΩ
	resistance	$V_{GS}$ = -4.5 V; $I_D$ = -5 A; $T_j$ = 150 °C	-	39	46	mΩ
		$V_{GS}$ = -2.5 V; $I_D$ = -5 A; $T_j$ = 25 °C	-	31	38	mΩ
		$V_{GS}$ = -1.8 V; $I_D$ = -3.7 A; $T_j$ = 25 °C	-	36	48	mΩ
g <sub>fs</sub>	forward transconductance	$V_{DS}$ = -10 V; $I_{D}$ = -5 A; $T_{j}$ = 25 °C	-	20	-	S
$R_G$	gate resistance	f = 1 MHz	-	5.3	-	Ω
Dynamic cl	haracteristics		'	'		,
Q <sub>G(tot)</sub>	total gate charge	$V_{DS}$ = -10 V; $I_{D}$ = -5 A; $V_{GS}$ = -4.5 V; $T_{j}$ = 25 °C	-	30	45	nC
$Q_{GS}$	gate-source charge		-	4.3	-	nC
$Q_{GD}$	gate-drain charge		-	7	-	nC
C <sub>iss</sub>	input capacitance	$V_{DS} = -10 \text{ V}$ ; f = 1 MHz; $V_{GS} = 0 \text{ V}$ ;	-	2970	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C	-	245	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	210	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = -10 V; $I_{D}$ = -5 A; $V_{GS}$ = -4.5 V;	-	12	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	53	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	91	-	ns
t <sub>f</sub>	fall time		-	46	-	ns
Source-dra	in diode	1	 1	1	1	
V <sub>SD</sub>	source-drain voltage	$I_S = -1.8 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	-0.7	-1.2	V
		<u> I</u>				

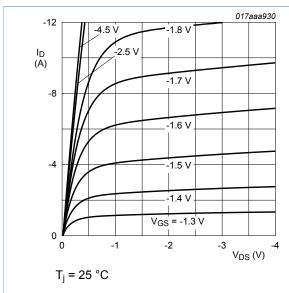


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

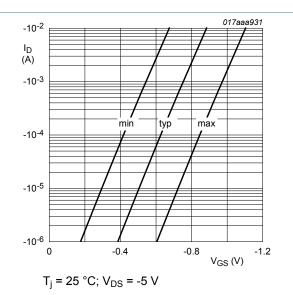


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

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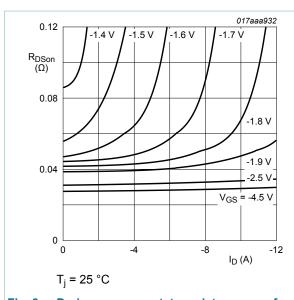


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

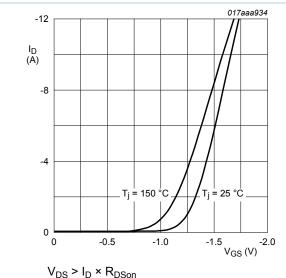


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

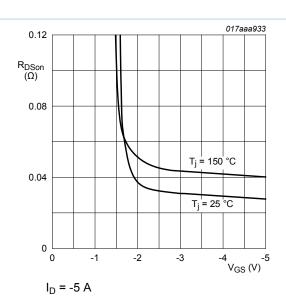


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

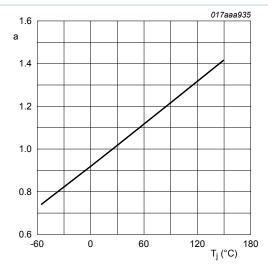


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

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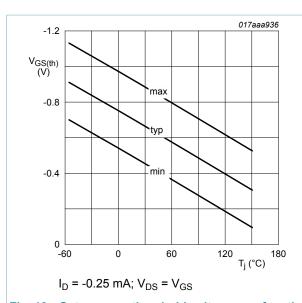


Fig. 12. Gate-source threshold voltage as a function of junction temperature

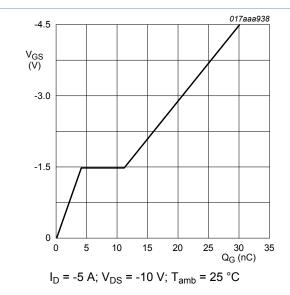
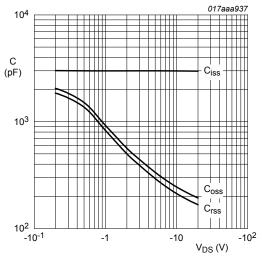


Fig. 14. Gate-source voltage as a function of gate charge; typical values



 $f = 1 MHz; V_{GS} = 0 V$ 

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

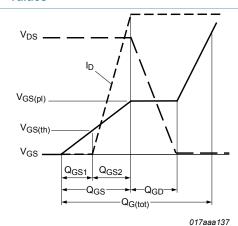
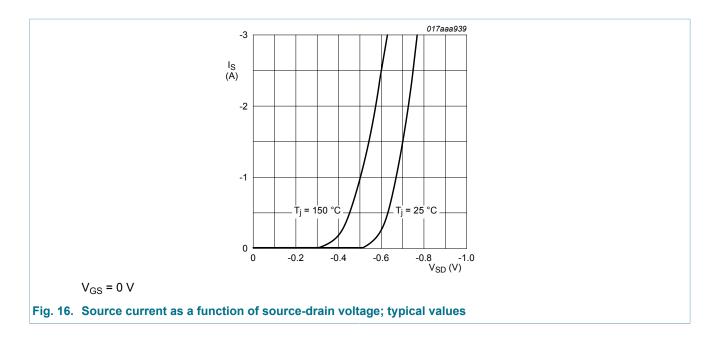


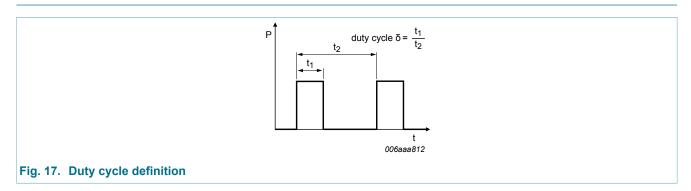
Fig. 15. MOSFET transistor: Gate charge waveform definitions

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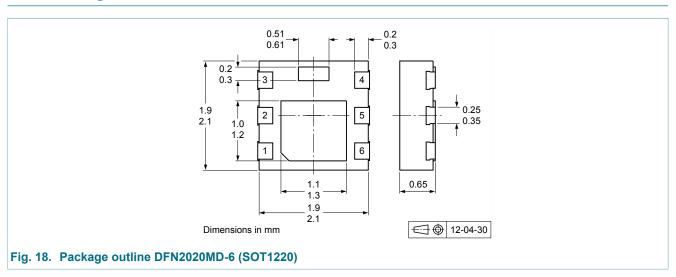
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## 8. Test information



# 9. Package outline



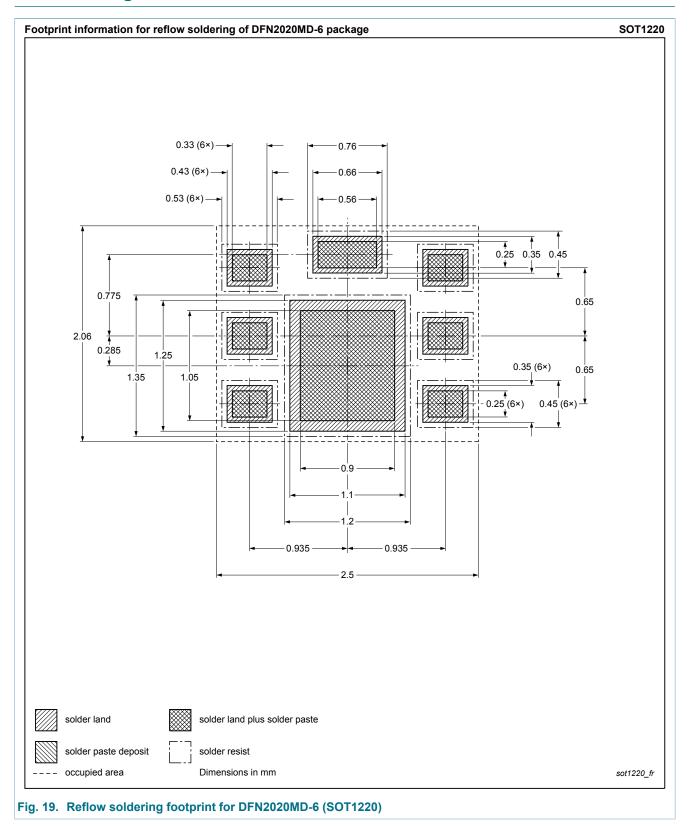
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## 10. Soldering



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# 11. Revision history

#### Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB29XPE v.1	20121205	Product data sheet	-	-

#### 20 V, single P-channel Trench MOSFET

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