# TYN16X-800RT

## SCR

19 July 2012 Product data sheet

## 1. Product profile

### 1.1 General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring very high inrush current capability, high thermal cycling performance and high junction temperature capability ($T_{j(max)}$ = 150 °C).

### 1.2 Features and benefits

- High junction operating temperature capability
- High thermal cycling performance
- High voltage capability
- Isolated package
- Planar passivated for voltage ruggedness and reliability
- Very High current surge capability

### 1.3 Applications

- Ignition circuits
- Motor control
- Protection circuits e.g. SMPS inrush current
- Voltage regulation

### 1.4 Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 800 | V |
| $V_{RRM}$ | repetitive peak reverse voltage | | | - | - | 800 | V |
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; Fig. 4; Fig. 5 | | - | - | 210 | A |
| | | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 8.3 ms | | - | - | 231 | A |
| $T_j$ | junction temperature | | | - | - | 150 | °C |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_h \leq 86$ °C; Fig. 3 | | - | - | 10.2 | A |

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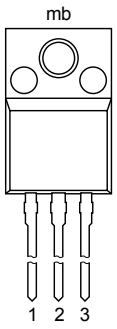
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_h \leq 86$ °C; Fig. 1; Fig. 2 | | - | - | 16 | A |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 7 | | - | 4.5 | 25 | mA |
| **Dynamic charateristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 150 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | 300 | - | - | V/µs |

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | K | cathode |  **TO-220F (SOT186A)** |  |
| 2 | A | anode | | |
| 3 | G | gate | | |
| mb | n.c. | mounting base; isolated | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TYN16X-800RT | TO-220F | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" | SOT186A |

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 800 | V |
| $V_{RRM}$ | repetitive peak reverse voltage | | | - | 800 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_h \leq 86$ °C; Fig. 3 | | - | 10.2 | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_h \leq 86$ °C; Fig. 1; Fig. 2 | | - | 16 | A |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; Fig. 4; Fig. 5 | | - | 210 | A |
| | | half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 8.3 ms | | - | 231 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p$ = 10 ms; SIN | | - | 220.5 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_T$ = 40 A; $I_G$ = 200 mA; $dI_G/dt$ = 200 mA/µs | | - | 50 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 5 | A |
| $V_{RGM}$ | peak reverse gate voltage | | | - | 5 | V |
| $P_{GM}$ | peak gate power | | | - | 20 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 1 | W |
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | | | - | 150 | °C |

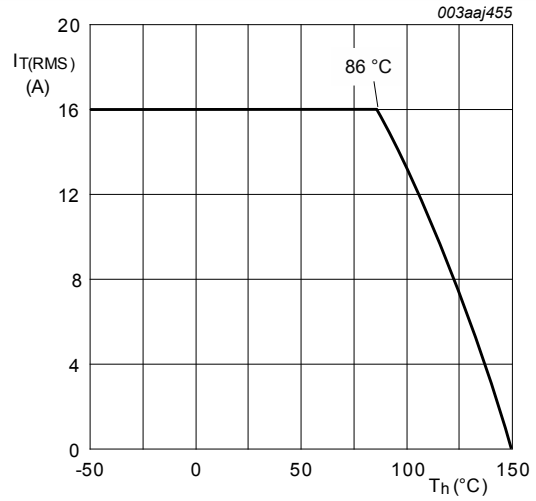



**Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values**

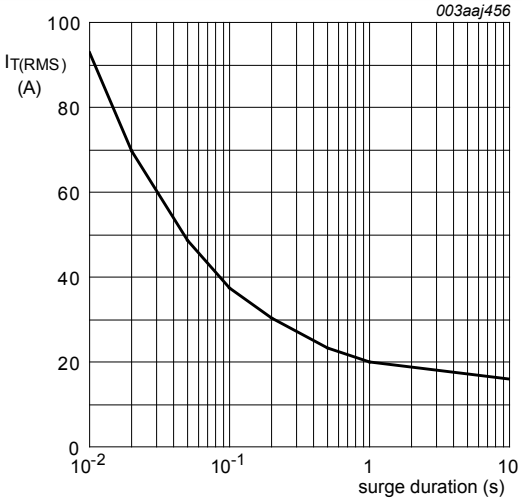



**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

f = 50 Hz; $T_h$ = 86 °C

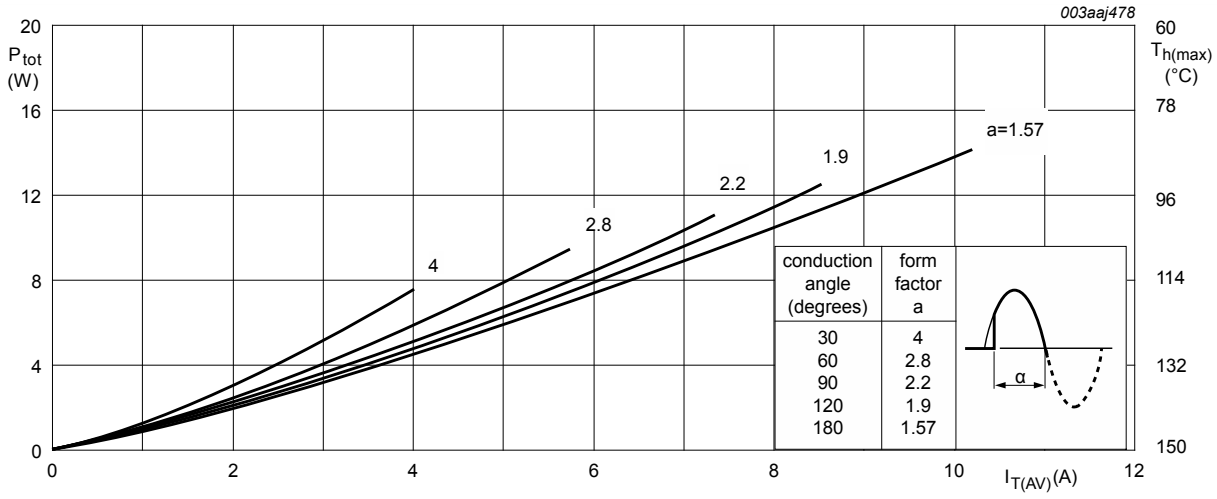



**Fig. 3. Total power dissipation as a function of average on-state current; maximum values**

$$a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$$

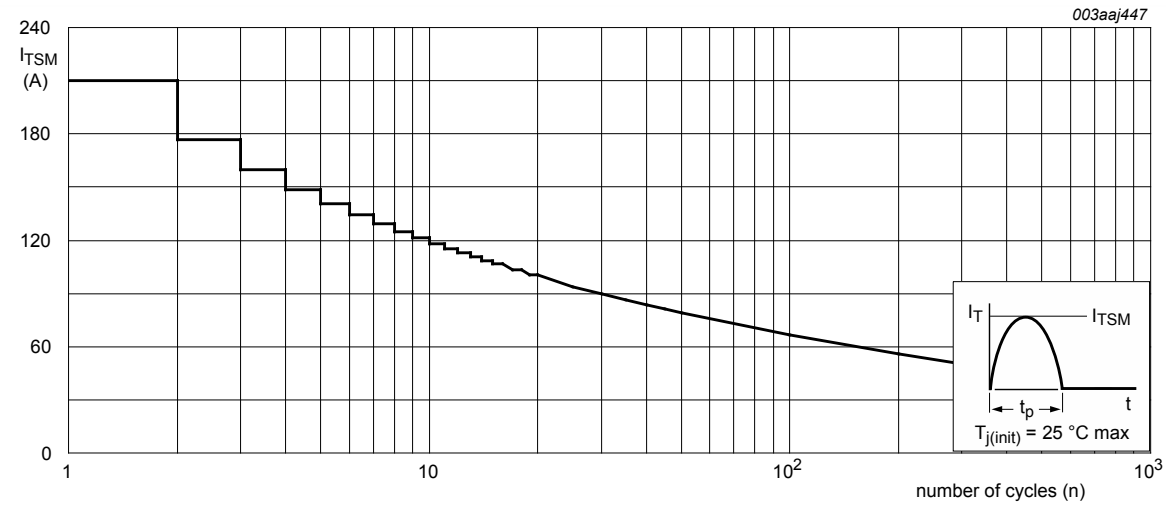



**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**

$$f = 50\ Hz$$

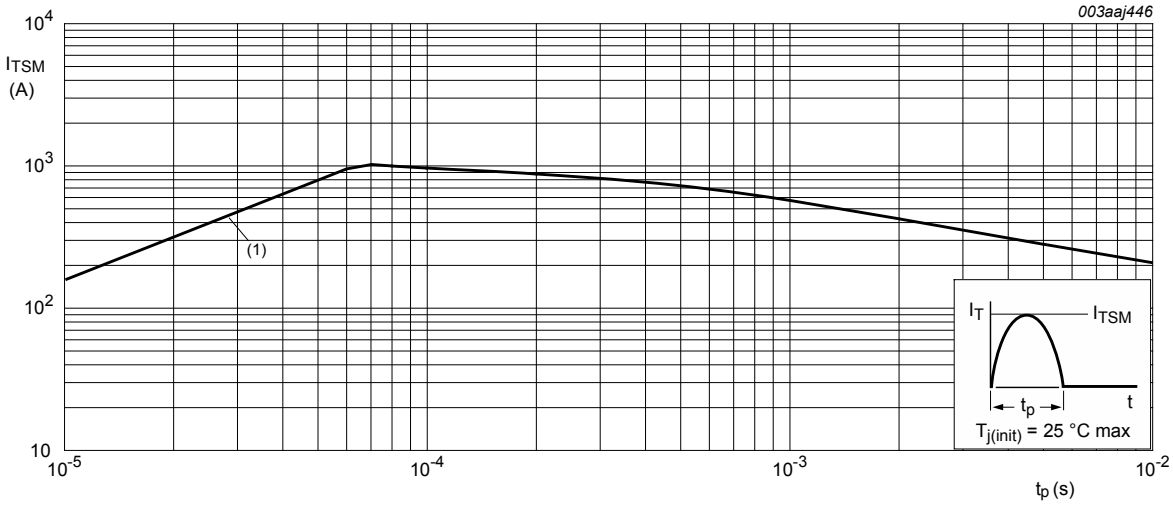


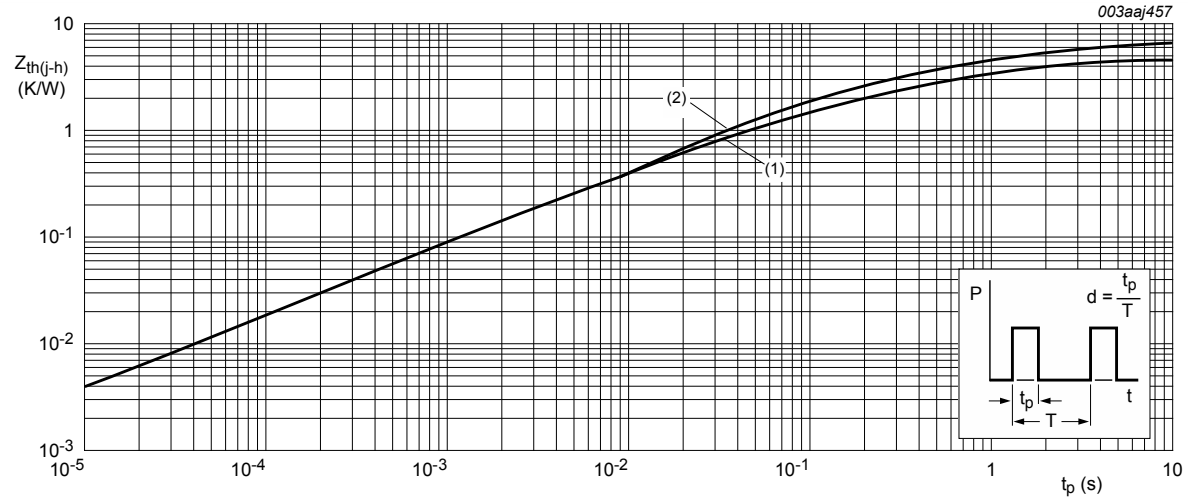

**Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values**

$t_p \leq 10$ ms; (1) $dI_T / dt$ limit

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-h)}$ | thermal resistance from junction to heatsink | full or half cycle; with heatsink compound; Fig. 6 | | - | - | 4.5 | K/W |
| | | full or half cycle; without heatsink compound; Fig. 6 | | - | - | 6.5 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | | - | 55 | - | K/W |




(1) with heatsink compound
(2) without heatsink compound

**Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width**

## 6. Isolation characteristics

**Table 6. Isolation characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{isol(RMS)}$ | RMS isolation voltage | from all terminals to external heatsink; sinusoidal waveform; clean and dust free ; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; $T_h$ = 25 °C | | - | - | 2500 | V |
| $C_{isol}$ | isolation capacitance | from anode to external heatsink ; f = 1 MHz; $T_h$ = 25 °C | | - | 10 | - | pF |

## 7. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 7 | | - | 4.5 | 25 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; $T_j$ = 25 °C; Fig. 8 | | - | 21 | 60 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | 16 | 40 | mA |
| $V_T$ | on-state voltage | $I_T$ = 32 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | 0.7 | 1.3 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 150 °C; Fig. 11 | | 0.2 | 0.4 | - | V |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_D$ | off-state current | $V_D$ = 800 V; $T_j$ = 150 °C | | - | 0.2 | 1 | mA |
| $I_R$ | reverse current | $T_j$ = 150 °C; $V_R$ = 800 V | | - | 0.2 | 1 | mA |
| **Dynamic charateristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 150 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | 300 | - | - | V/µs |

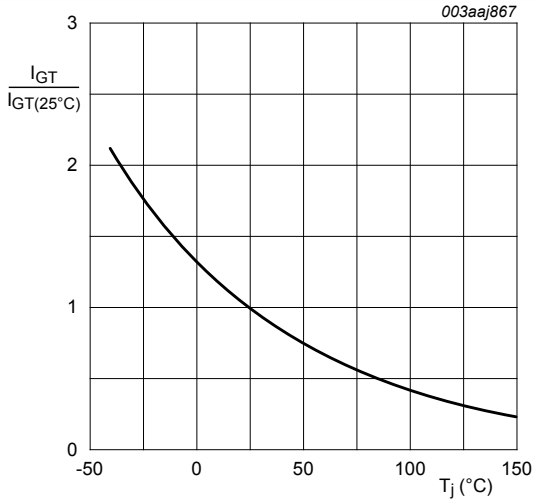



**Fig. 7. Normalized gate trigger current as a function of junction temperature**

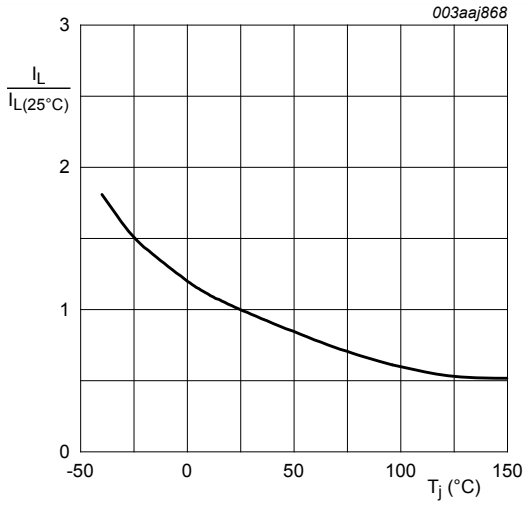



**Fig. 8. Normalized latching current as a function of junction temperature**

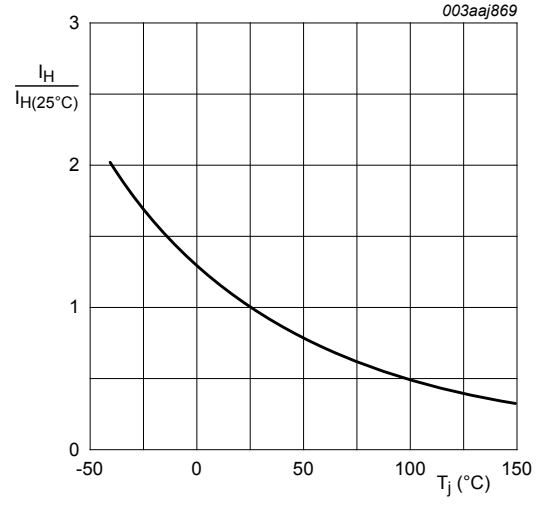
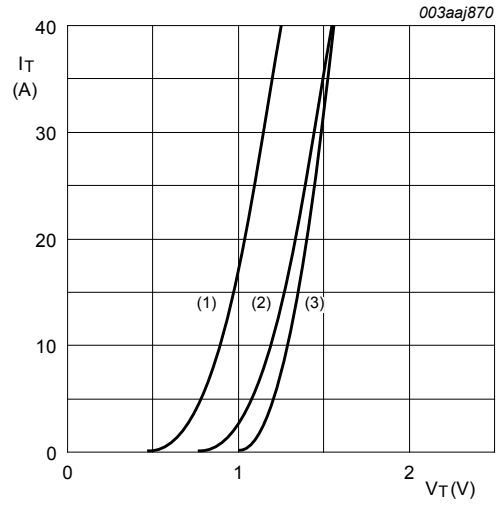



**Fig. 9. Normalized holding current as a function of junction temperature**




$V_o$ = 1.0336 V; $R_s$ = 0.0141 Ω

(1) $T_j$ = 150 °C; typical values

(2) $T_j$ = 150 °C; maximum values

(3) $T_j$ = 25 °C; maximum values

**Fig. 10. On-state current as a function of on-state voltage**

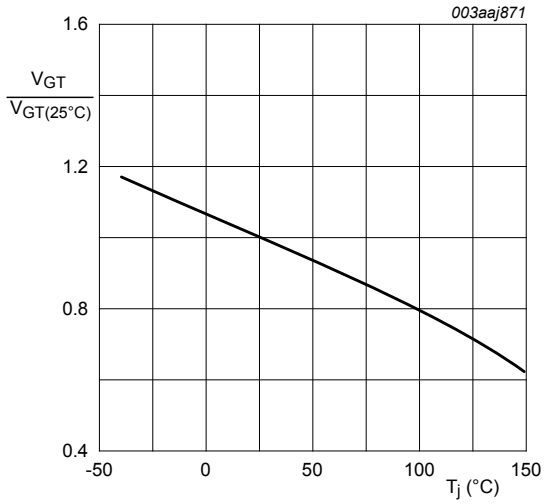
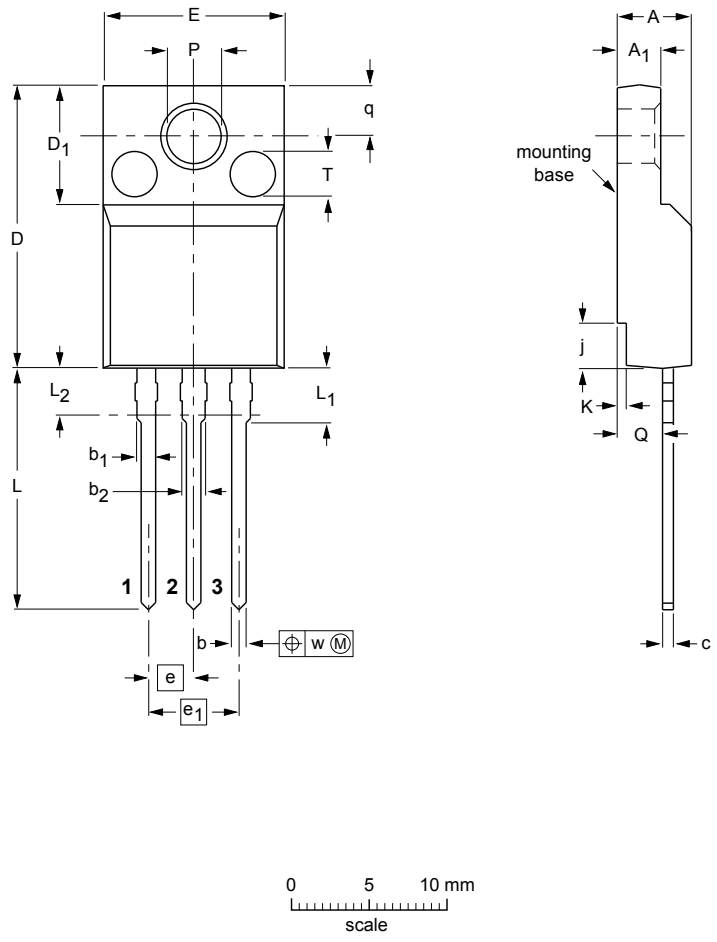



**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**

# 8. Package outline

**Plastic single-ended package; isolated heatsink mounted;**
**1 mounting hole; 3-lead TO-220 'full pack'**

**SOT186A**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | $b_2$ | c | D | $D_1$ | E | e | $e_1$ | j | K | L | $L_1$ | $L_2$ (1) max. | P | Q | q | T (2) | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.6<br>4.0 | 2.9<br>2.5 | 0.9<br>0.7 | 1.1<br>0.9 | 1.4<br>1.0 | 0.7<br>0.4 | 15.8<br>15.2 | 6.5<br>6.3 | 10.3<br>9.7 | 2.54 | 5.08 | 2.7<br>1.7 | 0.6<br>0.4 | 14.4<br>13.5 | 3.30<br>2.79 | 3 | 3.2<br>3.0 | 2.6<br>2.3 | 3.0<br>2.6 | 2.5 | 0.4 |

**Notes**

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are # 2.5 × 0.8 max. depth

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT186A | | 3-lead TO-220F | | | | ~~02-04-09~~<br>06-02-14 |

**Fig. 12. TO-220F (SOT186A)**

# 9. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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