TYN20B-800T

SCR

20 November 2012 Product data sheet

1. Product profile

1.1 General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT404 (D2PAK) surface mountable plastic package intended for use in applications requiring very high inrush current capability, high thermal cycling performance and high junction temperature capability ($T_{j(max)}$ = 150 °C).

1.2 Features and benefits

- High bidirectional blocking voltage capability
- High junction operating temperature capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Very high current surge capability

1.3 Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
V_{RRM}	repetitive peak reverse voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	210	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	-	231	A
T_j	junction temperature			-	-	150	°C

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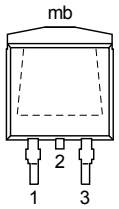
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 129$ °C; Fig. 1; Fig. 2		-	-	20	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	4.5	32	mA
Dynamic charateristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		300	-	-	V/µs

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 **D2PAK (SOT404)**	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TYN20B-800T	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
TYN20B-800T	TYN20B-800T

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
V_{RRM}	repetitive peak reverse voltage			-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 129$ °C; Fig. 3		-	12.7	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 129$ °C; Fig. 1; Fig. 2		-	20	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	210	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	231	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	220.5	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 40$ A; $I_G = 200$ mA; $dI_G/dt = 200$ mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	5	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	20	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	150	°C

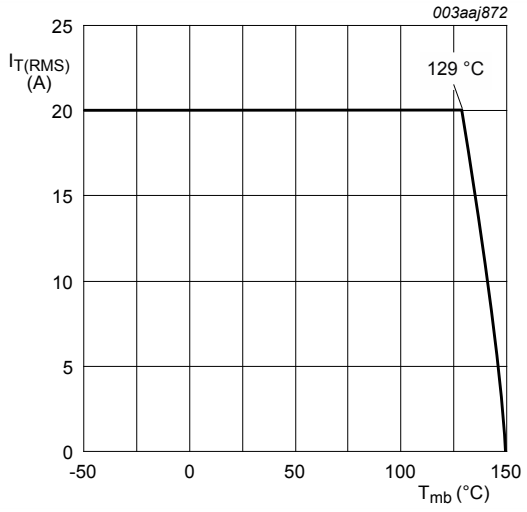


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

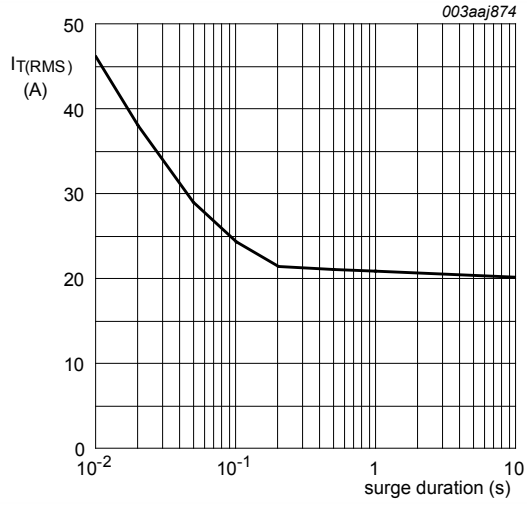


Fig. 2. RMS on-state current as a function of surge duration; maximum values

$f = 50$ Hz; $T_{mb} = 129$ °C

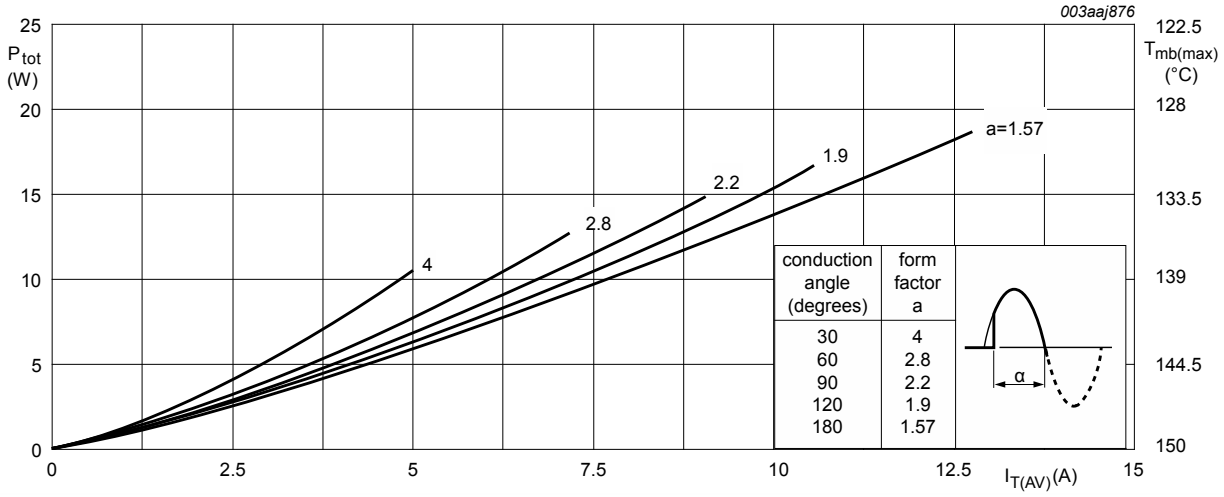


Fig. 3. Total power dissipation as a function of average on-state current; maximum values

$a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$

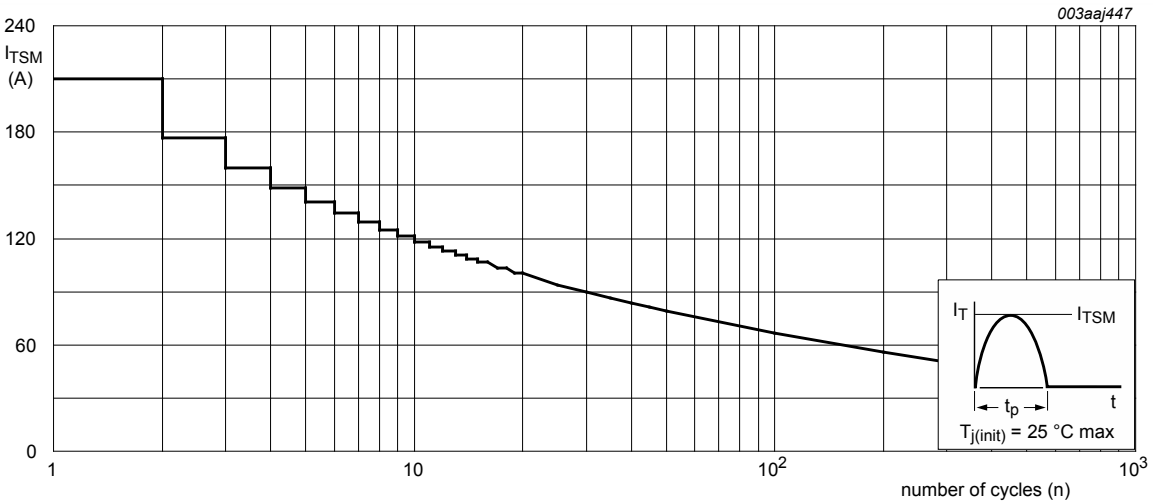


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

$f = 50\ Hz$

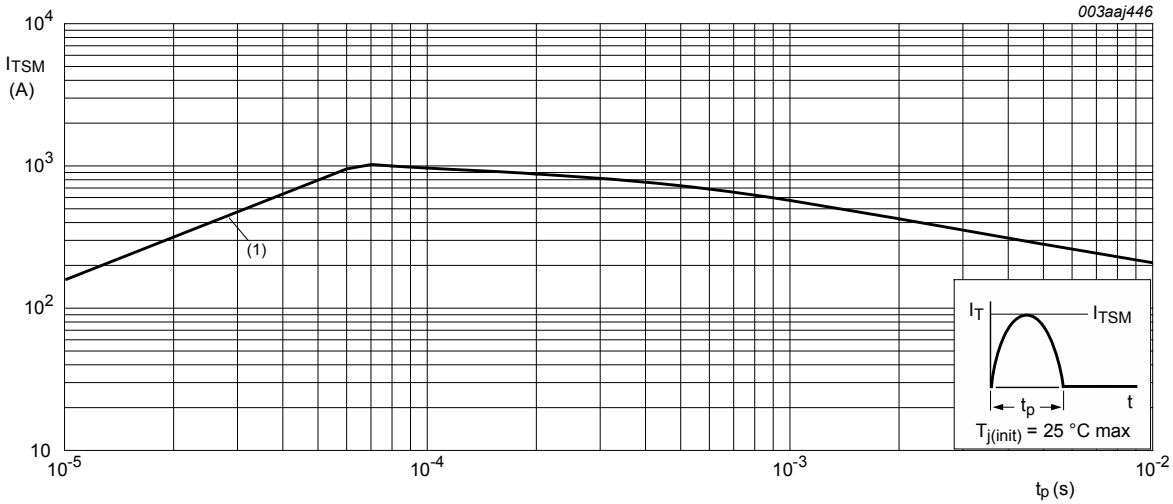


Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

$t_p \leq 10$ ms; (1) dI_T / dt limit

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint, FR4 board		-	55	-	K/W

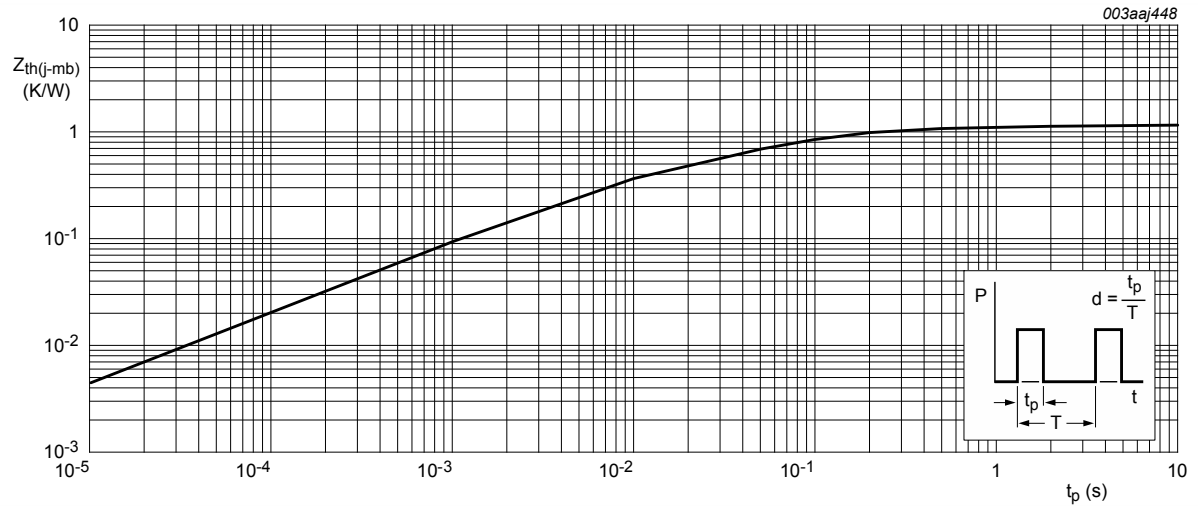


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	4.5	32	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	21	60	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	16	40	mA
V_T	on-state voltage	I_T = 32 A; T_j = 25 °C; Fig. 10		-	1.2	1.5	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1.3	V
		V_D = 400 V; I_T = 0.1 A; T_j = 150 °C; Fig. 11		0.2	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 150 °C		-	0.2	1	mA
I_R	reverse current	T_j = 150 °C; V_R = 800 V		-	0.2	1	mA
Dynamic charateristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		300	-	-	V/µs

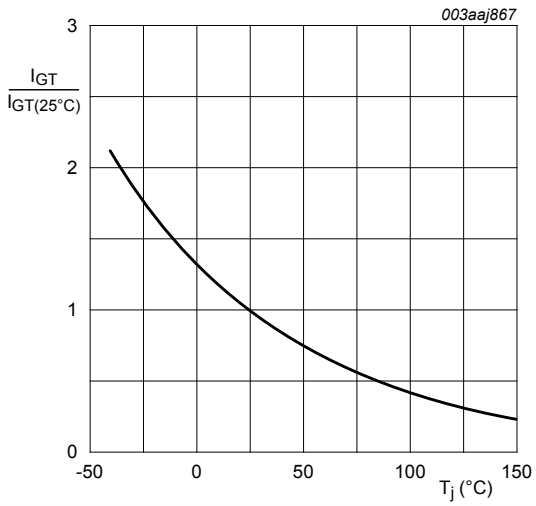


Fig. 7. Normalized gate trigger current as a function of junction temperature

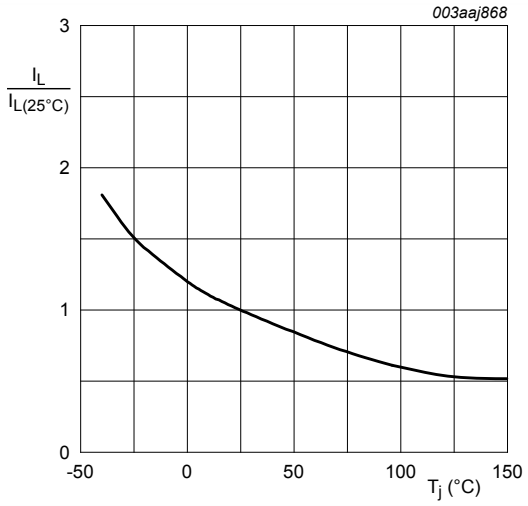


Fig. 8. Normalized latching current as a function of junction temperature

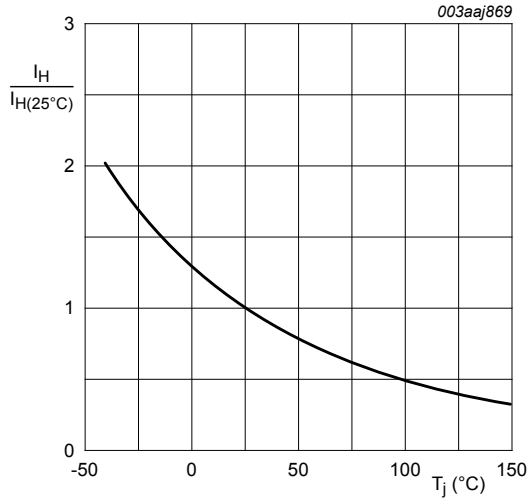
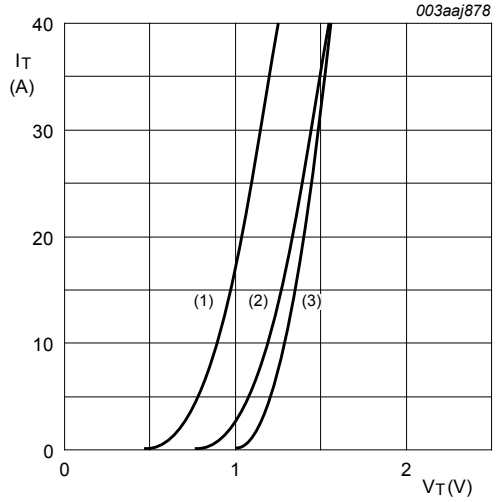


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.0485 V; R_s = 0.0133 Ω

(1) T_j = 150 °C; typical values

(2) T_j = 150 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

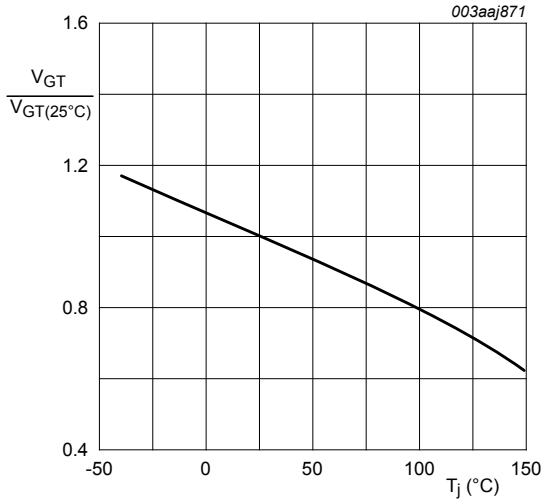
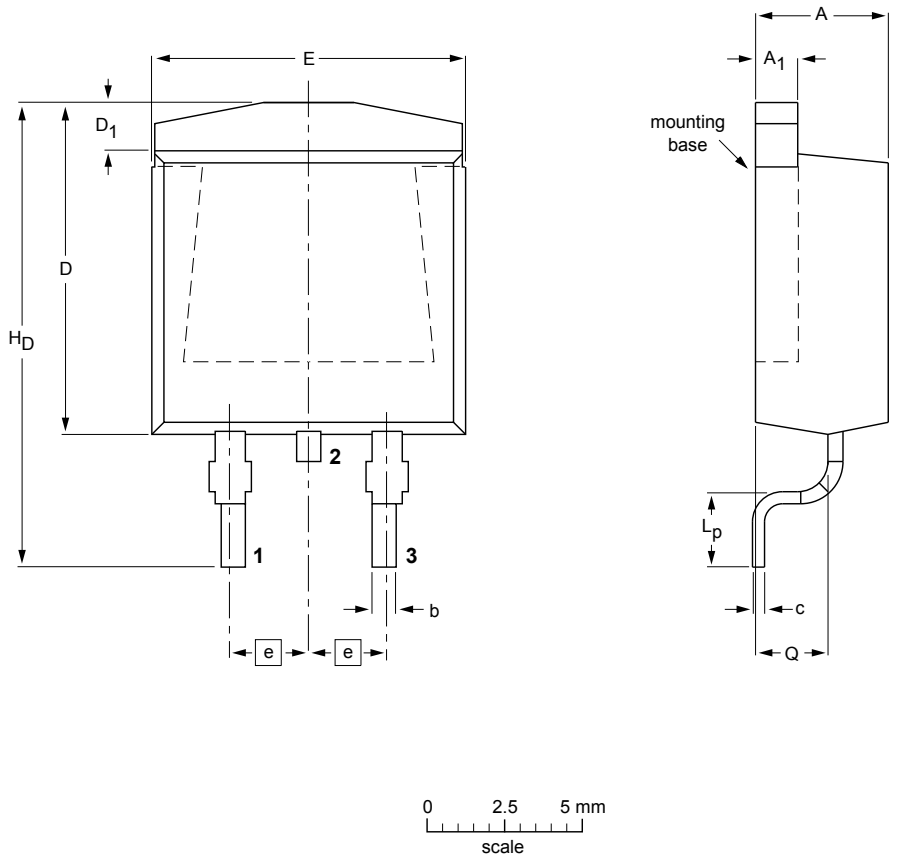


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig. 12. Package outline D2PAK (SOT404)

9. Soldering

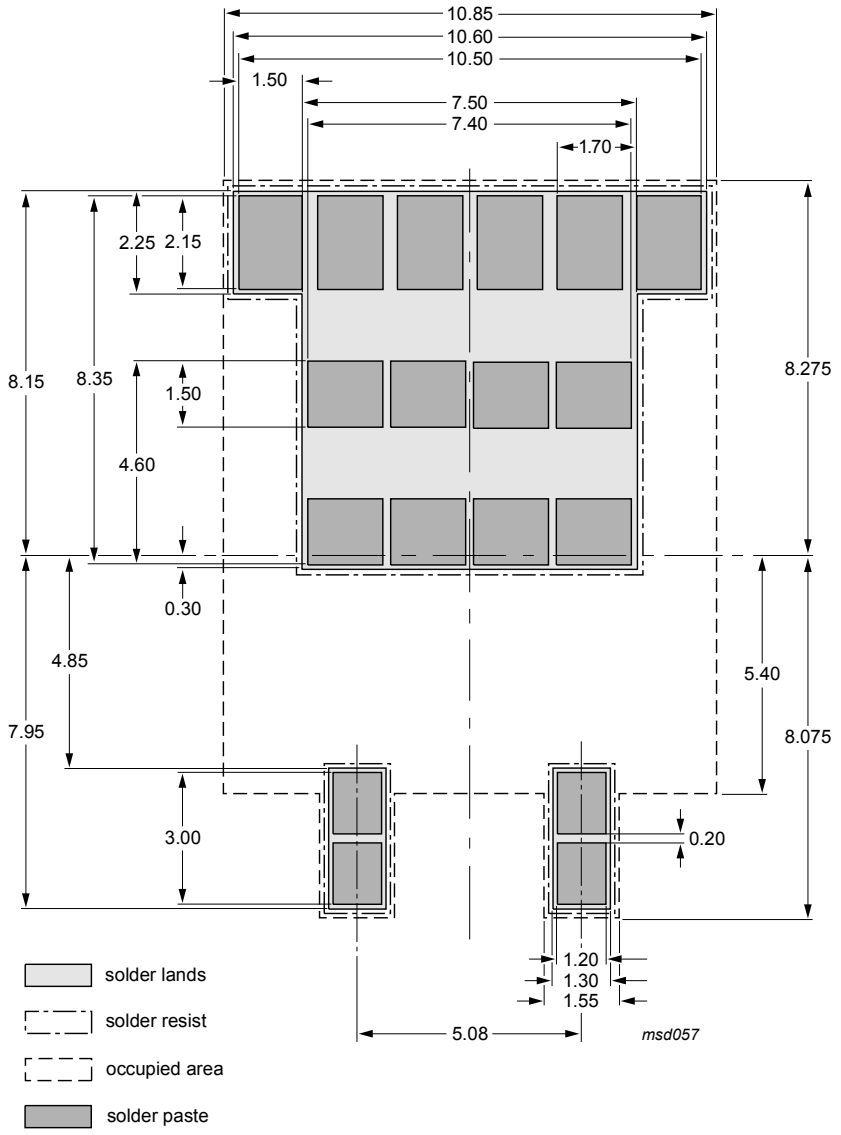


Fig. 13. Reflow soldering footprint for D2PAK (SOT404)

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