Ordering number : ENA2006

LC877G16A

CMOS IC
16K-byte ROM and 512-byte RAM
8-bit 1-chip Microcontroller

ON Semiconductor®
http://onsemi.com

Overview

The LC877G16A is an 8-bit microcontroller that, centered around a CPU running at a minimum bus cycle time of 200ns, integrates on a single chip a number of hardware features such as 16K-byte ROM, 512-byte RAM, an LCD controller/driver, a sophisticated 16-bit timer/counter (may be divided into 8-bit timers), two 8-bit timers with a prescaler, a 16-bit timer with a prescaler (may be divided into 8-bit timers), a UART interface (full duplex), infrared remote control receive function, and general-purpose I/O circuits.

Features

■ROM
- 16384 × 8 bits

■RAM
- 512 × 9 bits

■Minimum Bus Cycle Time
- 200ns (5MHz) V_{DD}=2.7 to 5.5V
  Note: The bus cycle time here refers to ROM read speed.

■Minimum Instruction Cycle Time (tCYC)
- 600ns (5MHz) V_{DD}=2.7 to 5.5V

■Operating Temperature Range
- -40°C to +85°C

■Ports

- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1-bit units: 13 (2 for UART, 1 for remote control, and 10 for key-scan signal I/O)
- Normal withstand voltage input port 1 (XT1)
- LCD ports
  Segment output: 74 (S00 to S73)
  Common output: 4 (COM0 to COM3)
  Bias power supply for LCD driving: 3 (V1 to V3)

Multiplexed pin functions
  Input/output ports: 8 (P1n)

- Dedicated oscillator ports 2 (CF1, CF2)
- Reset pin 1 (RES)
- Power pins 2 ($V_{DD}1$, $V_{SS}1$)

■LCD Controller

(1) Display duty: 1/3duty, 1/4duty
(2) Display bias: 1/2bias, 1/3bias

■UART

- Full duplex
- 7/8/9 bits data bit selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator
- Maximum transfer rate: 200kbps (5MHz)

■Timers

- Timer 0: 16-bit timer/counter with a capture register
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture registers)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 8: 16-bit timer
  Mode 0: 8-bit timer with an 8-bit prescaler × 2 channels
  Mode 1: 16-bit timer with an 8-bit prescaler

- Base Timer
  1) The clock can be selected from the system clock and timer 0 prescaler output.
  2) An interrupt can be generated at five different time intervals.

■Infrared Remote Control Receiver Circuit 1

1) Noise rejection function
2) Supports receive formats with a guide-pulse of half-clock/clock/none.
3) Determines an end of receive by detecting a no-signal period (no carrier).
(Supports same receive format with a different bit length.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Interrupts

- 14 sources, 8 vectors

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, an interrupt into the smallest vector address is given priority.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	T0L/remote control receiver1
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6			
7	00033H	H or L	UART receive/T8L/T8H
8	0003BH	H or L	UART transmit
9			
10	0004BH	H or L	Port 0/T4/T5

- Priority levels: X > H > L
- When interrupts of the same level occur at the same time, an interrupt with the smallest vector address is given priority.

■Subroutine Stack Levels

- Up to 256 levels mum (stack is allocated in RAM)

■Oscillator Circuits

- RC oscillator circuit (internal): For system clock
- CF oscillator circuit: For system clock, with internal Rf, and external Rd

■ System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle can be selected from among 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 5MHz).

■Standby Function

- HALT mode: HALT mode is used to minimize power dissipation of the IC.
  Halts instruction execution while allowing the peripheral circuits to continue operation.
  (Some serial transfer functions are suspended.)
  1) Oscillators do not stop automatically.
  2) Released by a system reset or occurrence of an interrupt.
- HOLD mode: HOLD mode is used to minimize power dissipation of the IC.
  Suspends instruction execution and operation of the peripheral circuits.
  1) The CF and RC oscillators automatically stop operation.
  2) There are three ways of releasing HOLD mode.
    (1) Setting the reset pin to a low level
    (2) Setting at least one of the INT0, INT1, and INT3 pins to the specified level
    (3) Establishing an interrupt source at port 0

■Package Form

- TQFP100 (14×14) “Lead-free and halogen-free product”

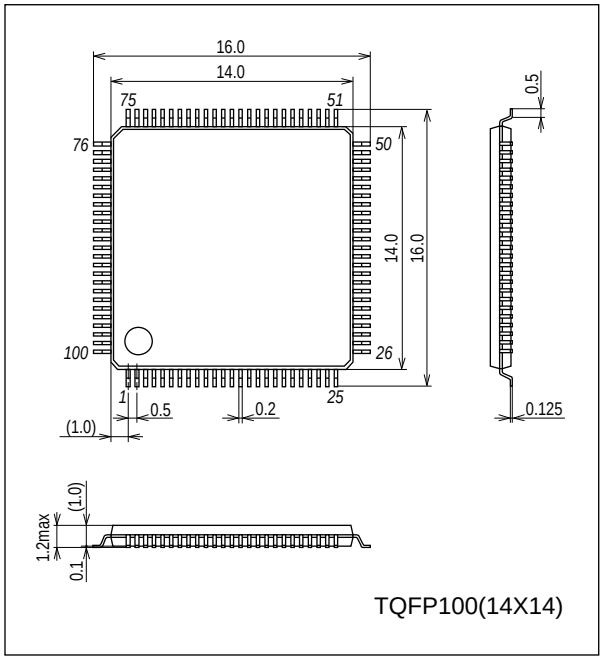
■Development Tools

- On-chip debugger: TCB87-Type B + LC87D7G16A
  TCB87-Type C (3-wire cable) + LC87D7G16A

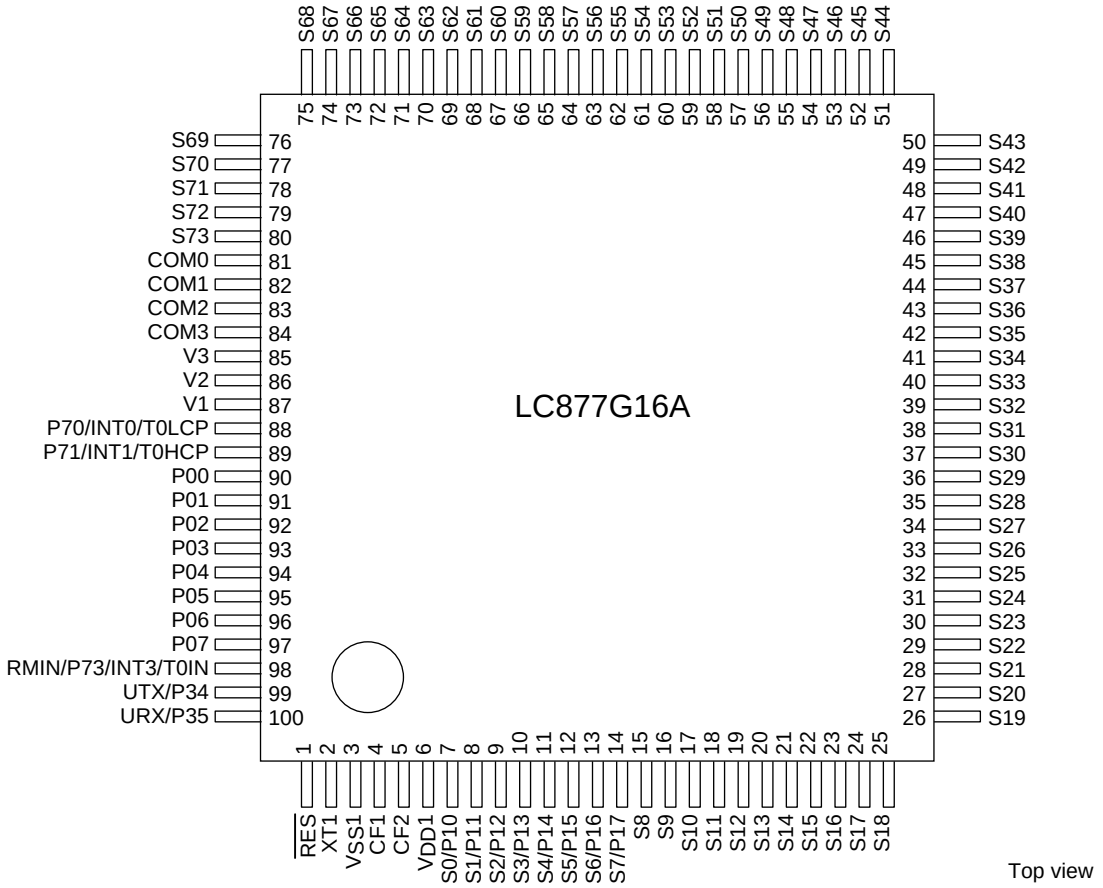
Package Dimensions

unit : mm (typ)

3274



Pin Assignment

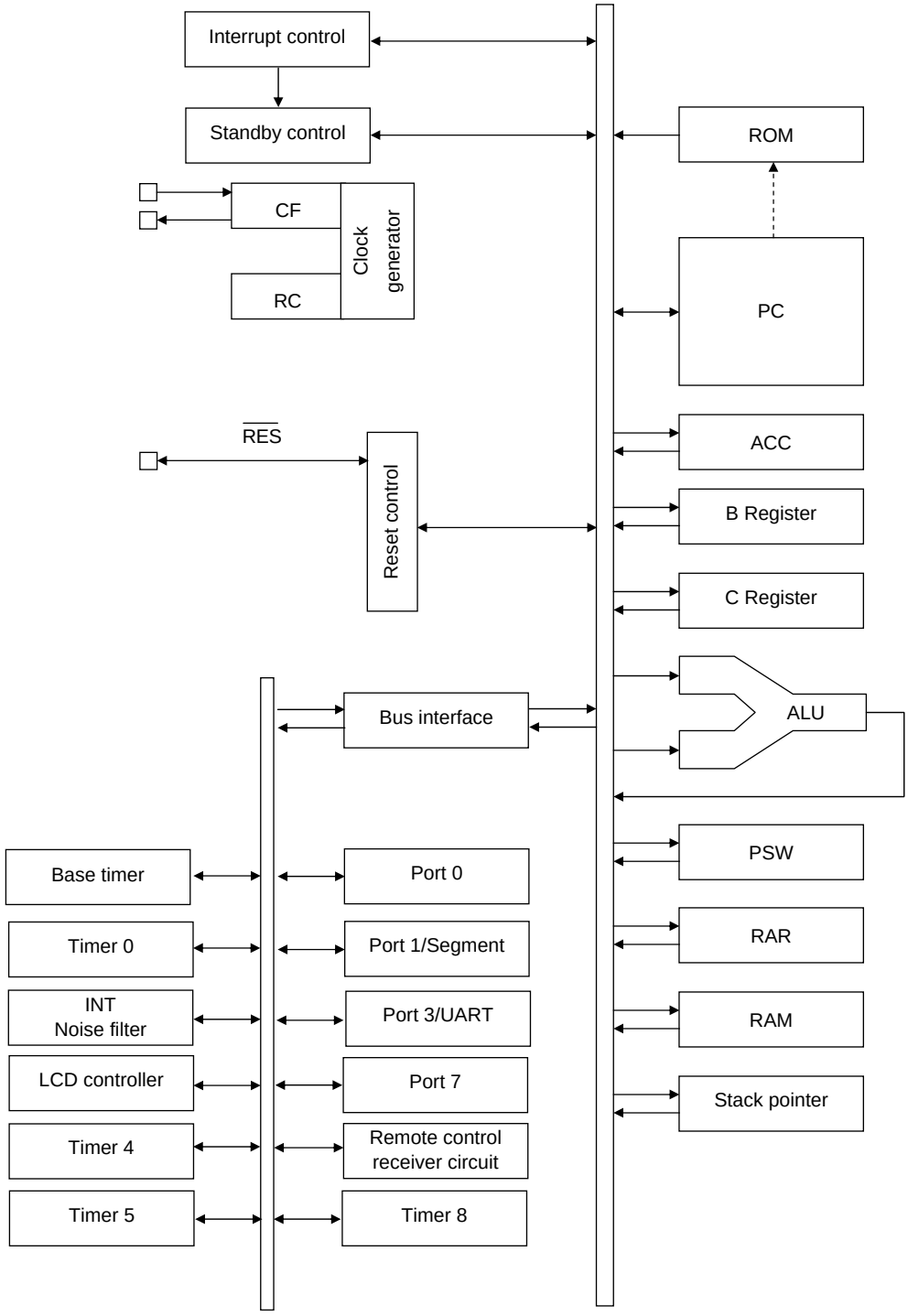


TQFP100 (14×14) “Lead-free and halogen-free product”

PIN No.	NAME
1	$\overline{RES}$
2	XT1
3	$V_{SS}1$
4	CF1
5	CF2
6	$V_{DD}1$
7	S0/P10
8	S1/P11
9	S2/P12
10	S3/P13
11	S4/P14
12	S5/P15
13	S6/P16
14	S7/P17
15	S8
16	S9
17	S10
18	S11
19	S12
20	S13
21	S14
22	S15
23	S16
24	S17
25	S18
26	S19
27	S20
28	S21
29	S22
30	S23
31	S24
32	S25
33	S26
34	S27
35	S28
36	S29
37	S30
38	S31
39	S32
40	S33
41	S34
42	S35
43	S36
44	S37
45	S38
46	S39
47	S40
48	S41
49	S42
50	S43

PIN No.	NAME
51	S44
52	S45
53	S46
54	S47
55	S48
56	S49
57	S50
58	S51
59	S52
60	S53
61	S54
62	S55
63	S56
64	S57
65	S58
66	S59
67	S60
68	S61
69	S62
70	S63
71	S64
72	S65
73	S66
74	S67
75	S68
76	S69
77	S70
78	S71
79	S72
80	S73
81	COM0
82	COM1
83	COM2
84	COM3
85	V3
86	V2
87	V1
88	P70/INT0/T0LCP
89	P71/INT1/T0HCP
90	PO0
91	P01
92	P02
93	P03
94	P04
95	P05
96	P06
97	P07
98	RMIN/P73/INT3/T0IN
99	UTX/P34
100	URX/P35

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>$V_{SS}1$</td><td>-</td><td>- power supply</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>-</td><td>+ power supply</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O can be specified in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.
• HOLD release input
• Port 0 interrupt input</td><td>Yes</td></tr>
<tr><td>Port 3
P34, P35</td><td>I/O</td><td>• 2-bit I/O port
• I/O can be specified in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.
• Multiplexed pin function
UTX: UART transmit data output
URX: UART receive data input</td><td>Yes</td></tr>
<tr><td>XT1</td><td>I</td><td>• Test pin
• 1-bit input port</td><td>No</td></tr>
<tr><td>Port 7
P70, P71, P73</td><td>I/O</td><td>• 3-bit I/O port
• I/O can be specified in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.
• Multiplexed pin function
P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD release input/timer 0H capture input
P73: INT3 input (with noise filter input/timer 0 event input/timer 0H capture input/infrared remote control receive input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr>
<tr><td>INT1</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr>
<tr><td>INT3</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>S0/P10 to S7/P17</td><td>I/O</td><td>• LCD display segment output
• Can be used as a general-purpose I/O port (P1).</td><td>No</td></tr>
<tr><td>S8 to S73</td><td>O</td><td>• LCD segment output</td><td>No</td></tr>
<tr><td>COM0 to COM3</td><td>O</td><td>• LCD common output</td><td>No</td></tr>
<tr><td>V1 to V3</td><td>I/O</td><td>• LCD bias</td><td>No</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>• Reset pin</td><td>No</td></tr>
<tr><td>CF1</td><td>I</td><td>• Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>O</td><td>• Ceramic resonator output pin</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P34 to P35	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P70	-	No	N-channel open drain	Programmable
P71, P73	-	No	CMOS	Programmable
S0/P10 to S7/P17	-	No	CMOS	Programmable
S8 to S73	-	No	Dedicated LCD output	No
COM0 to COM3	-	No	Dedicated LCD output	No
V1 to V3	-	No	Dedicated LCD input	No
XT1	-	No	Input only	No

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1$ = 0V

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$			-0.3		+6.5	V
LCD supply voltage		VLCD	V1, V2, V3			-0.3		V_{DD}	
Input voltage		V_I(1)	XT1, CF1, $\overline{RES}$			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 3, 7			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 34, 35	• CMOS output selected • Each pin used		-10			mA
		IOPH(2)	Ports 71, 73	• Each pin used		-5			
		IOPH(3)	Port 1	• Each pin used		-5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 34, 35	• CMOS output selected • Each pin used		-7.5			
		IOMH(2)	Ports 71, 73	• Each pin used		-3			
		IOMH(3)	Port 1	• Each pin used		-3			
	Total output current	ΣIOAH(1)	Ports 0,1,34, 35, 7	Total of all pins		-45			
Low level output current	Peak output current	IOPL(1)	Ports 0, 34, 35	• Each pin used				20	
		IOPL(2)	Port 7	• Each pin used				10	
		IOPL(3)	Port 1	• Each pin used				10	
	Mean output current (Note 1-1)	IOML(1)	Ports 0, 34, 35	• Each pin used				15	
		IOML(2)	Ports 7	• Each pin used				7.5	
		IOML(3)	Port 1	• Each pin used				7.5	
	Total output current	ΣIOAL(1)	Ports 0,1,34, 35, 7	Total of all pins				80	
Allowable power dissipation		Pd max	TQFP100(14×14)	Ta=-40 to +85°C				231	mW
Operating ambient temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage range (Note 2-1)	$V_{DD}(1)$	$V_{DD}1$	0.588µs≤tCYC≤30µs		2.7		5.5	V
Memory retention supply voltage	VHD	$V_{DD}1$	Keep RAM and register data in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 0, 1, 3, 7	• Output disabled • When INT1VTSL=0 (P71 only)	2.7 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	P71 interrupt side	• Output disabled • When INT1VTSL=1	2.7 to 5.5	$0.85V_{DD}$		V_{DD}	
	$V_{IH}(3)$	XT1, CF1, $\overline{RES}$		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 0, 1	Output disabled	4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
				2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 34, 35, 7	• Output disabled • When INT1VTSL=0 (P71 only)	4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	P71 interrupt side	• Output disabled • When INT1VTSL=1	2.7 to 5.5	V_{SS}		$0.45V_{DD}$	
	$V_{IL}(4)$	XT1		2.7 to 5.5	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(5)$	CF1, $\overline{RES}$		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			2.7 to 5.5	0.588		30	µs
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ration=1/1 • External system clock duty=50 ± 5%	2.7 to 5.5	0.1		5	MHz
			• CF2 pin open • System clock frequency division ratio = 1/2	2.7 to 5.5	0.2		10	
Oscillation frequency range (Note 2-3)	FmCF (1)	CF1, CF2	5MHz ceramic resonator oscillation See Fig. 1.	2.7 to 5.5		5		
	FmRC		Internal RC oscillation	2.7 to 5.5	0.3	1.0	2.0	

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 3, 7	• Output disabled • Pull-up resistor off • $V_{IN}=V_{DD}$ (Including output Tr off-leakage current)	2.7 to 5.5			1	µA
	$I_{IH}(2)$	$\overline{RES}$	$V_{IN}=V_{DD}$	2.7 to 5.5			1	
	$I_{IH}(3)$	XT1	• Input port specification • $V_{IN}=V_{DD}$	2.7 to 5.5			1	
	$I_{IH}(4)$	CF1	$V_{IN}=V_{DD}$	2.7 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 3, 7	• Output disabled • Pull-up resistor off • $V_{IN}=V_{SS}$ (Including output Tr off-leakage current)	2.2 to 5.5	-1			
	$I_{IL}(2)$	$\overline{RES}$	$V_{IN}=V_{SS}$	2.2 to 5.5	-1			
	$I_{IL}(3)$	XT1	• Input port specification • $V_{IN}=V_{SS}$	2.2 to 5.5	-1			
	$I_{IL}(4)$	CF1	$V_{IN}=V_{SS}$	2.2 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	CMOS output ports 0, 34, 35	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.2mA	2.7 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	Ports 71 to 73	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(5)$		I_{OH}=-0.2mA	2.7 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$	Port 1	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(7)$		I_{OH}=-0.2mA	2.7 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 34, 35	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=1mA	2.7 to 5.5			0.4	
	$V_{OL}(4)$	Port 7	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(5)$		I_{OL}=1mA	2.7 to 5.5			0.4	
	$V_{OL}(6)$	Port 1	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(7)$		I_{OL}=1mA	2.7 to 5.5			0.4	
LCD output voltage	VODLS	S0 to S73	• I_O=0mA • VLCD, 2/3VLCD 1/3VLCD level output • See Fig. 6.	2.7 to 5.5	0		±0.2	
	VODLC	COM0 to COM3	• I_O=0mA • VLCD, 2/3VLCD 1/2VLCD, 1/3VLCD level output • See Fig. 6.	2.7 to 5.5	0		±0.2	
LCD bias resistor	RLCD(1)	Resistance per one bias resistor	See Fig. 6.	2.7 to 5.5		60		kΩ
	RLCD(2)	• Resistance per one bias resistor • Resistor division 1/2 mode	See Fig. 6.	2.7 to 5.5		30		
Pull-up MOS Tr. resistor	Rpu(1)	• Ports 0, 1, 3, 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	
	Rpu(2)			2.7 to 4.5	18	50	150	
Hysteresis voltage	VHYS(1)	• Port 7 • $\overline{RES}$		2.7 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• For pins other than that under test: $V_{IN}=V_{SS}$ • f=1MHz • Ta=25°C	2.7 to 5.5		10		pF

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71)	• Interrupt source flag can be set. • Event input for timer 0 is enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (Noise rejection ratio is 1/1.)	• Interrupt source flag can be set. • Event input for timer 0 is enabled.	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (Noise rejection ratio is 1/32.)	• Interrupt source flag can be set. • Event input for timer 0 is enabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (Noise rejection ratio is 1/128.)	• Interrupt source flag can be set. • Event input for timer 0 is enabled.	2.7 to 5.5	256			
	tPIH(5) tPIL(5)	RMIN(P73)	Recognized as a signal by infrared remote control receiver circuit	2.7 to 5.5	4			RMCK (Note4-1)
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	2.7 to 5.5	200			µs

Note 4-1: RMCK denotes the reference frequency of the remote control receiver circuit (40tCYC/50tCYC).

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 5-1)	IDDOP(1)	$V_{DD}1$	• FmCF=5MHz ceramic resonator oscillation • System clock set to CF 5MHz side • Internal RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		2.9	7.2	mA
	IDDOP(2)			2.7 to 3.6		1.6	3.9	
	IDDOP(3)		• FmCF=0Hz (oscillation stopped) • System clock set to internal RC oscillation • 1/2 frequency division ratio	4.5 to 5.5		0.4	1.3	
	IDDOP(4)			2.7 to 3.6		0.2	0.6	
HALT mode consumption current (Note 5-1)	IDDHALT(1)		HALT mode • FmCF=5MHz ceramic resonator oscillation • System clock set to CF 5MHz side • Internal RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		1.1	3.2	
	IDDHALT(2)			2.7 to 3.6		0.5	1.5	
	IDDHALT(3)		HALT mode • FmCF=0Hz (oscillation stopped) • System clock set to internal RC oscillation • 1/2 frequency division ratio	4.5 to 5.5		0.3	0.8	
	IDDHALT(4)			2.7 to 3.6		0.2	0.3	
HOLD mode consumption current	IDDHOLD(1)		HOLD mode • CF1=V_{DD} or open (When using external clock)	4.5 to 5.5		0.14	14	µA
	IDDHOLD(2)			2.7 to 3.6		0.03	10	

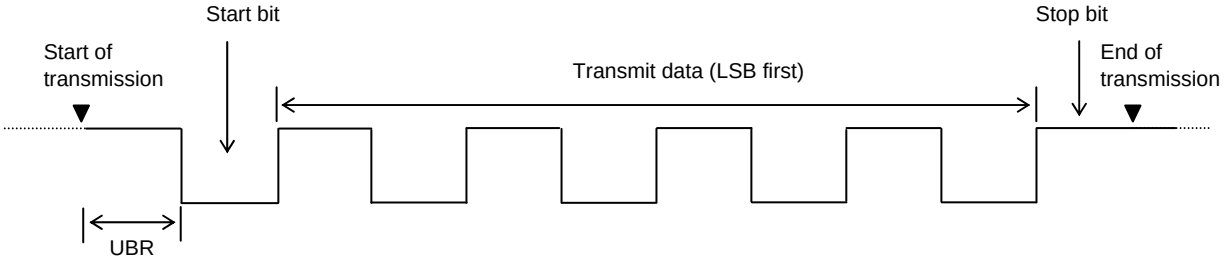
Note 5-1: The consumption current value do not include current that flows into the output transistors and internal pull-up resistors.

UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1$ = 0V

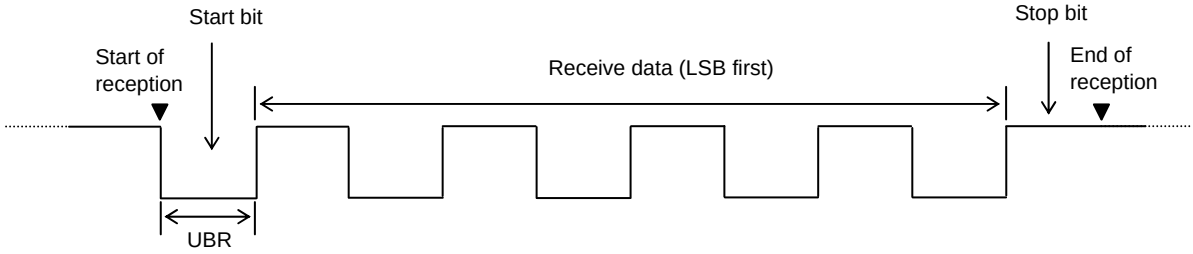
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	UTX(P34), URX(P35)		2.7 to 5.5	16/3		8192/3	tCYC

Data length: 7/8/9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



Example of 8-bit Data Reception Mode Processing (Receive Data=55H)



Main System Clock Oscillator Circuit Characteristics

Given below are the characteristics of a sample main system clock oscillator circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a sample main system clock oscillator circuit with a ceramic resonator

Frequency	Manufacturer	Resonator Name	Circuit Parameters				Operating Voltage Range[V]	Oscillation Stabilization Time		Notes
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
5MHz	Murata	CSTCR5M00G53-R0	(15)	(15)	Open	2.2k	2.7 to 5.5	0.05	0.15	Values shown in parentheses are capacitance included in the resonator
		CSTLS5M00G53-B0	(15)	(15)	Open	2.2k	2.7 to 5.5	0.05	0.15	

The oscillation stabilization time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (See Fig. 3)

Notes: Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

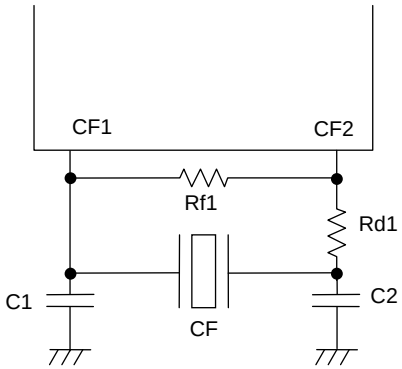


Figure 1 Ceramic Oscillator Circuit

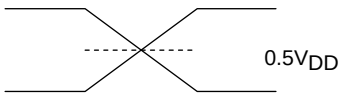
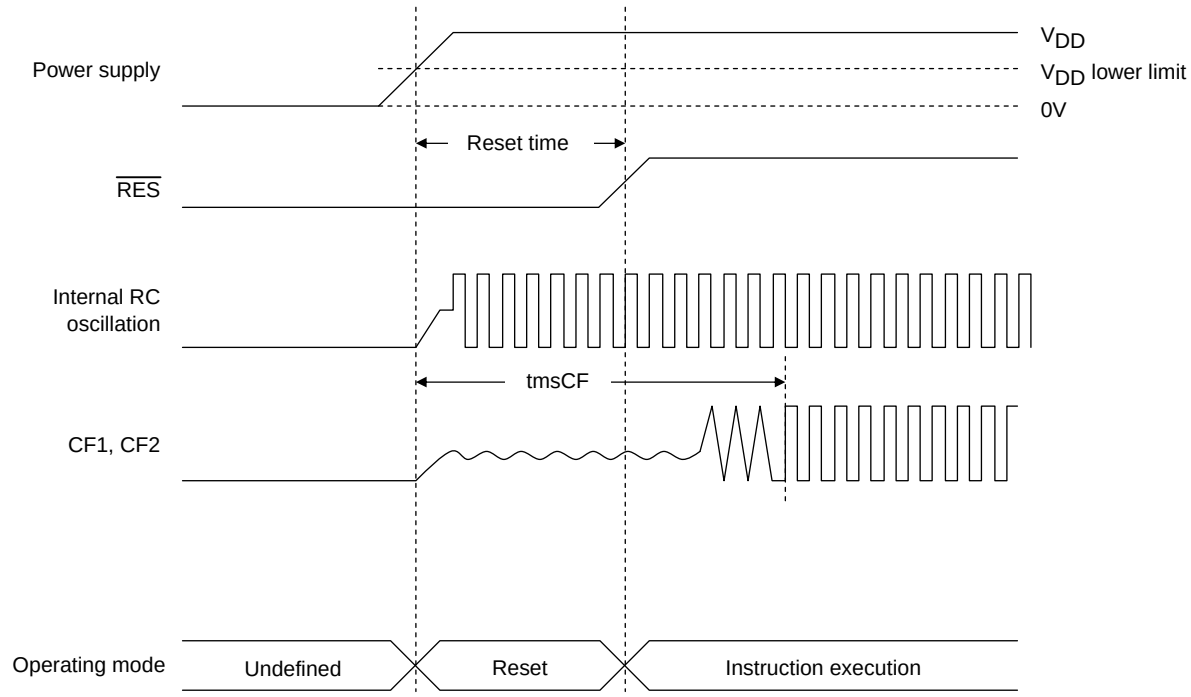
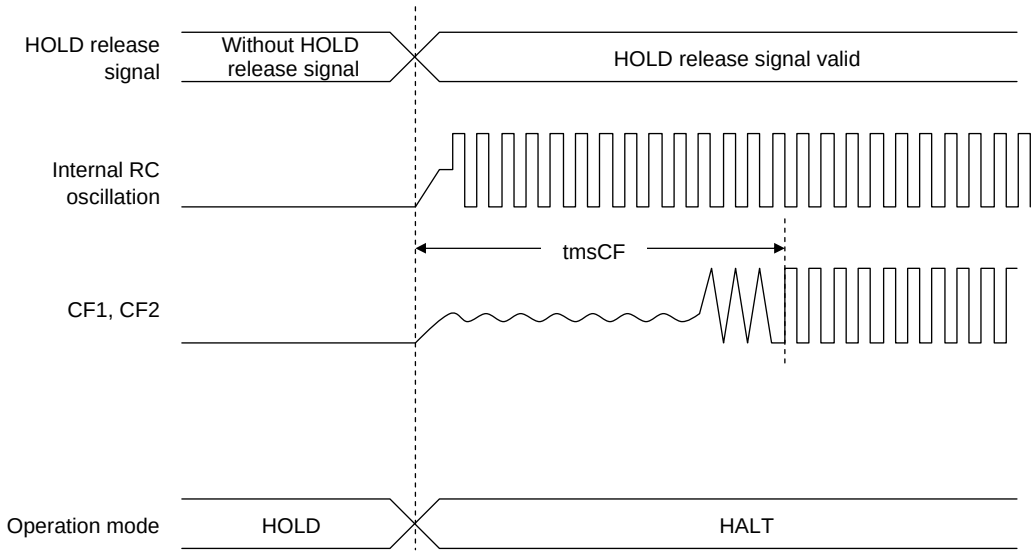


Figure 2 AC Timing Measurement Point

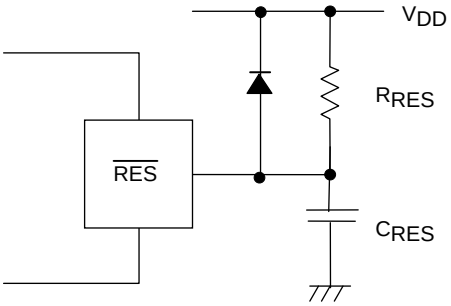


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 3 Oscillation Stabilization Time



Note:
Select C_{RES} and R_{RES} value to assure that at least 200μs reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 4 Reset Circuit

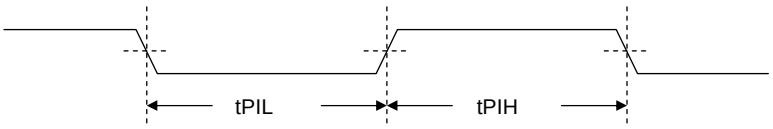


Figure 5 Pulse Input Timing Signal Waveform

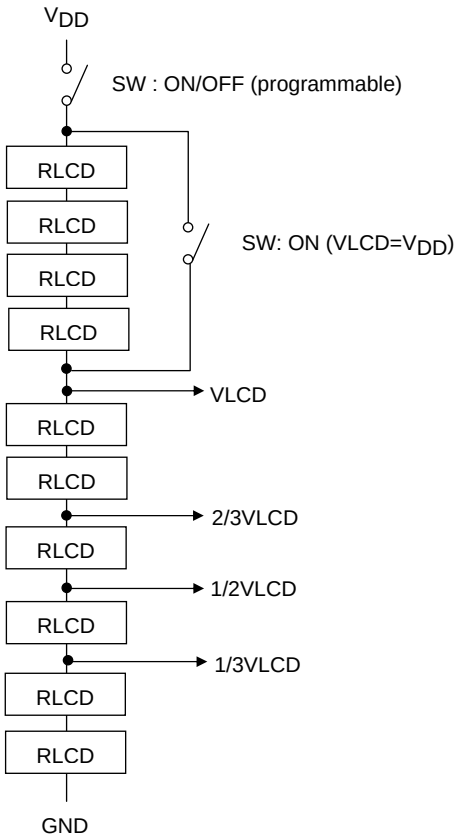


Figure 6 LCD Bias Resistor