TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT CMOS STATIC RAM

TC5518CP-15/CPL-15/CP-20/CPL-20
TC5518CF-15/CFL-15/CF-20/CFL-20

DESCRIPTION

The TC5518CP/CF is a 16384-bit high speed and low power sully static random access memory organized as 2048 words by a 8 bits using CMOS technology, and operates from a single 5V supply. The TC5518CP/CF has two chip enable inputs, $\overline{CE1}$ and $\overline{CE2}$, which are used for device selection and can be used in order to achieve minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved.

Thus the TC5518CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518CPL/CFL guaranteed a standby current epual to or less than 1μA at 60°C ambient temperature available. And the TC5518CP/CPL is pin compatible with 2716 type EPROM. This means that the TC5518CP/CPL and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

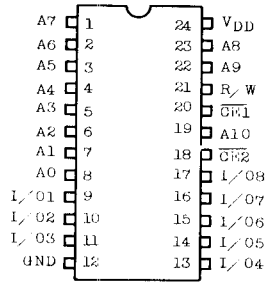
- Low Power Dissipation
  5mA/MHz (MAX.) Operating
  0.2μA(MAX.) at Ta=25°C Standby
  1.0μA(MAX.) at Ta=60°C Standby
- 5V Single Power Supply
- Low Voltage Operation : V_{DD}=3V
  $t_{CO1, 2}$=1μs(MAX.) Ta=60°C
- Wide Temperature Operation
  Ta=−40~85°C
- Fully Static Operation
- Data Retention Voltage : 2.0V~5.5V
- Two Chip Enables ($\overline{CE1}$, $\overline{CE2}$)
  Simple Memory Expansion and Battery Back Up

- Access Time

	TC5518CP-15/CPL-15	TC5518CP-20/CPL-20
	TC5518CF-15/CFL-15	TC5518CF-20/CFL-20
Address Access Time (MAX.)	150ns	200ns
$\overline{CE1}$ Access Time (MAX.)	150ns	200ns
$\overline{CE2}$ Access Time (MAX.)	150ns	200ns

- Directly TTL Compatible: All Inputs and Outputs
- 24 Pin Standard Plastic Package : TC5518CP
- 24 Pin Flat Package : TC5518CF

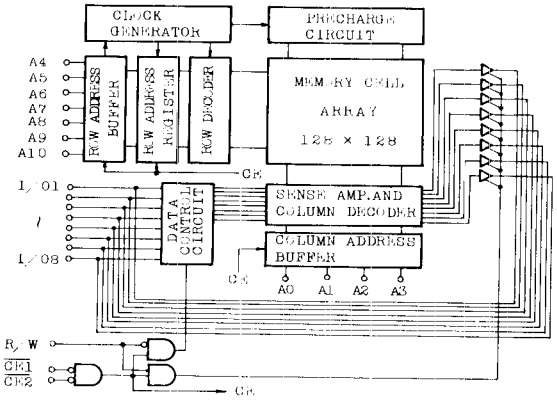
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{10}	Address Inputs
R/W	Read/Write Control Input
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE_2}$	$\overline{CE_1}$	R/W	A_0~A_{10}	I/O_1~I/O_8	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	L	L	Stable	Data In	I_{DDO}
** Standby 1	*	H	*	*	High Impedance	I_{DDS}
** Standby 2	H	*	*	*	High Impedance	I_{DDS}

Note : * : H or L ** : Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3~7.0V
V_{IN}	Input Voltage	−0.3V~V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V~V_{DD}+0.3V
P_D	Power Dissipation(Ta=85°C)	0.8W(0.45W)*
T_{STG}	Storage Temperature	−55°C~150°C
T_{OPR}	Operating Temperature	−40°C~85°C
T_{SOLDER}	Soldering Temperature·Time	260°C·10sec.

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta=−40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D. C. CHARACTERISTICS (Ta=−40~85°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS			TC5518CP-15 CF-15 MIN.	TC5518CP-15 CF-15 MAX.	TC5518CP-20 CF-20 MIN.	TC5518CP-20 CF-20 MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			—	±1.0	—	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE_2}=V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			—	±5.0		±5.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			−1.0	—	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			2.0	—	2.0	—	mA
I_{DDS1}	Standby Current	$\overline{CE_2}$=2.2V or $\overline{CE_1}$=2.2V			—	3.0	—	3.0	mA
I_{DDS2}	Standby Current	$\overline{CE_2}=V_{DD}-0.5V$ or $\overline{CE_1}=V_{DD}-0.5V$, V_{DD}=2~5.5V	TC5518CPL/CFL	Ta=25°C	—	0.2	—	0.2	μA
				Ta=60°C	—	1.0	—	1.0	
			TC5518CP/CF	Ta=25°C	—	1.0	—	1.0	
				Ta=60°C	—	5.0	—	5.0	
				Ta=85°C	—	30	—	30	
I_{DDO1}	Operating Current	t_{cycle}=Min. cycle, $\overline{CE_1}=\overline{CE_2}$=0V, I_{OUT}=0mA		$V_{IN}=V_{IH}/V_{IL}$	—	45		30	mA
I_{DDO2}				$V_{IN}=V_{DD}/GND$	—	40		25	
I_{DDO3}		t_{cycle}=1μs, $\overline{CE_1}$=		$V_{IN}=V_{IH}/V_{IL}$	—	10	—	10	
I_{DDO4}		$\overline{CE_2}$=0V, I_{OUT}=0mA		$V_{IN}=V_{DD}/GND$	—	5	—	5	

Note : Typical values are at Ta=25°C, V_{DD}=5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	—	5	10	pF
$C_{I/O}$	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	—	200	—	ns
t_{ACC}	Address Access Time	—	150	—	200	
t_{CO1}	$\overline{CE_1}$ to Output Valid	—	150	—	200	
t_{CO2}	CE_2 to Output Valid	—	150	—	200	
t_{COE}	$\overline{CE_1}$ or CE_2 to Output Active	10	—	10	—	
t_{OD}	Output High-Z Deselection	—	50	—	60	
t_{OH}	Output Hold from Address Charge	15	—	20	—	

Write Cycle

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	150	—	200	—	ns
t_{WP}	Write Pulse Width	120	—	150	—	
t_{AW}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	Output High-Z from R/W	—	50	—	60	
t_{OEW}	Output Active from R/W	10	—	10	—	
t_{DS}	Data Set up Time	60	—	80	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6V, 2.4V

Timing Measurement Reference Levels

Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

3V OPERATE SPECIFICATION

D. C. RECOMMENDED OPERATING CONDITIONS (Ta = −10~60°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	V_{DD}−0.2	—	V_{DD}	V
V_{IL}	Input Low Voltage	0	—	0.2	V

D. C. and OPERATING CHARACTERISTICS ($Ta = -10 \sim 60°C$)

SYMBOL	PARAMETER	CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0V \leqq V_{IH} \leqq V_{DD}$			—	—	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$, $2 = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			—	—	±5.0	μA
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.2V$			−100	—	—	μA
I_{OL}	Output Low Current	$V_{OL} = 0.2V$			100	—	—	μA
I_{DDS}	Standby Current	$\overline{CE1} = \overline{CE2} = V_{IH}$	TC5518CPL/CFL	Ta = 25°C	—	—	0.2	μA
				Ta = 60°C	—	—	1.0	
			TC5518CP/CF	Ta = 25°C	—	—	1.0	
				Ta = 60°C	—	—	5.0	
I_{DDO}	Operating Current	$\overline{CE1}$, $2 = 0V$, $I_{OUT} = 0mA$, tr, tf ≦ 20μsec		$t_{cycle} = 1\mu sec$	—	2.0	3.0	mA
				$t_{cycle} = 10\mu sec$	—	0.3	0.5	

● All voltage is measured from GND.

A. C. CHARACTERISTICS ($Ta = -10 \sim 60°C$, $V_{DD} = 3V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	—	—	ns
t_{ACC}	Address Access Time	—	250	1000	ns
t_{CO1}	$\overline{CE1}$ to Output Valid	—	250	1000	ns
t_{CO2}	$\overline{CE2}$ to Output Valid	—	250	1000	ns
t_{COE}	$\overline{CE1}$ or $\overline{CE2}$ Output Active	10	—	—	ns
t_{OD}	Output High-Z Deselection	—	—	200	ns
t_{OH}	Output Hold from Address Change	20	—	—	ns

Write Cycle

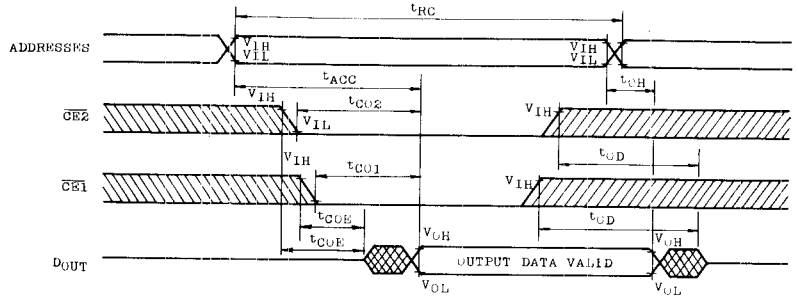
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	—	—	ns
t_{WP}	Write Pulse Width	500	—	—	ns
t_{AW}	Address Set up Time	100	—	—	ns
t_{WR}	Write Recovery Time	100	—	—	ns
t_{ODW}	Output High-Z from R/W	—	—	200	ns
t_{OEW}	Output Active from R/W	10	—	—	ns
t_{DS}	Data Set up Time	400	—	—	ns
t_{DH}	Data Hold Time	50	—	—	ns

A. C. TEST CONDITIONS

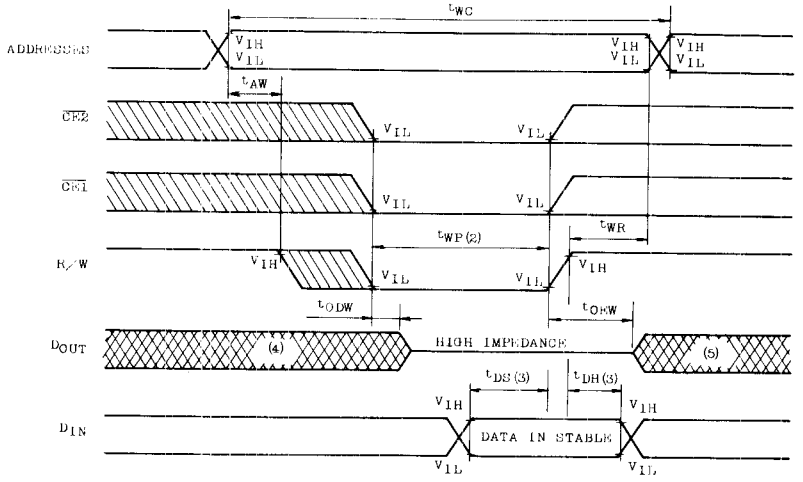
Output Load		: 100pF (Include Jig)
Input Pulse Levels		: 0.2V, $V_{DD} - 0.2V$
Timing Measurement Level	Input	: 1.5V , 1.5V
	Output	: 1.5V , 1.5V
Input Pulse Rise and Fall Times		: ≦20ns

TIMING WAVEFORMS

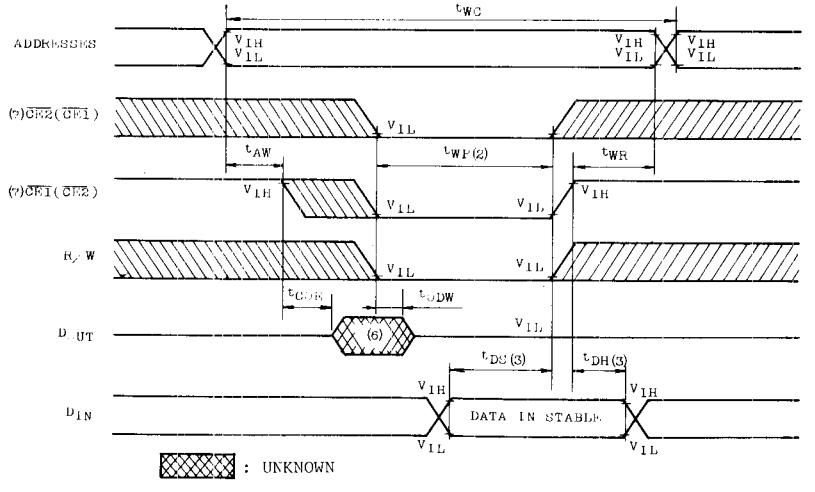
- Read Cycle



- Write Cycle 1



- Write Cycle 2



Note :

1. R/W is high for a read Cycle.
2. t_{WP} is specified as logical "AND" of $\overline{CE_1}$, $\overline{CE_2}$ and R/W.
   t_{WP} is measured from the latter of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going low to the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
3. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
4. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE_1}$ or $\overline{CE_2}$ low transition, the output buffers remain in a high impedance state in this peried.
7. A write occurs during the overlap of a low $\overline{CE_1}$, low $\overline{CE_2}$ and low R/W.
   In write cycle 2, write is controlled by either $\overline{CE_1}$ or $\overline{CE_2}$.

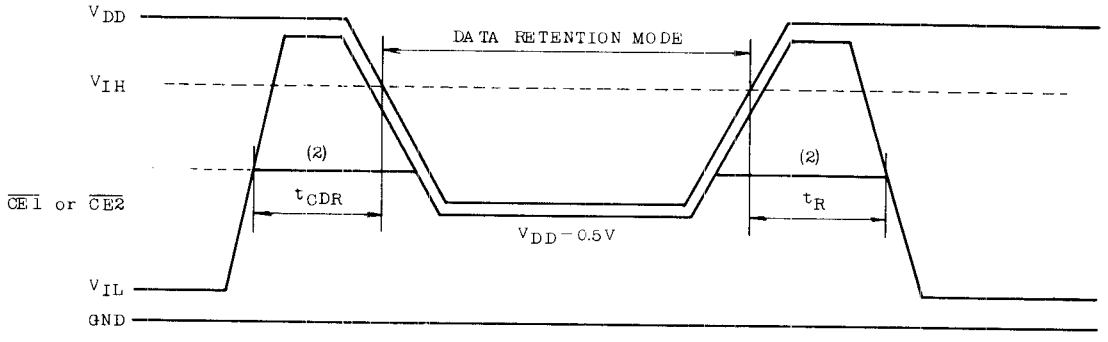
DATA RETENTION CHARACTERISTICS

(Ta = −40~85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	—	5.5	V
I_{DDS2}	Standby Current	TC5518CPL/CFL	Ta = 25°C	—	0.005	0.2	μA
			Ta = 60°C	—	—	1.0	
		TC5518CP/CF	Ta = 25°C	—	0.05	1.0	
			Ta = 60°C	—	—	5.0	
			Ta = 85°C	—	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	—	—	μs
t_R	Recovery Time			t_{RC}(1)	—	—	μS

Note :

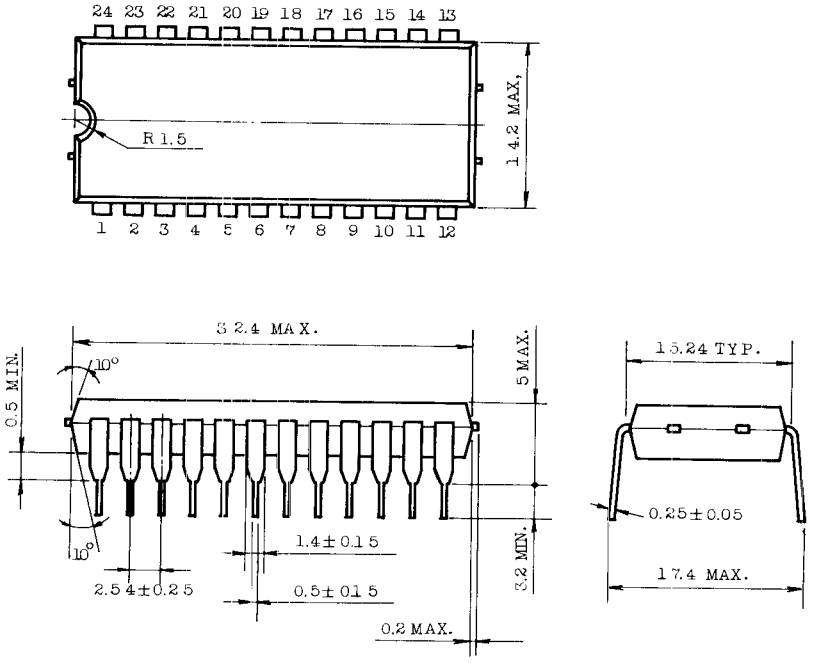
(1) t_{RC} : Read Cycle Time



(2) If the V_{IH} level of $\overline{CE_2}$ ($\overline{CE_1}$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

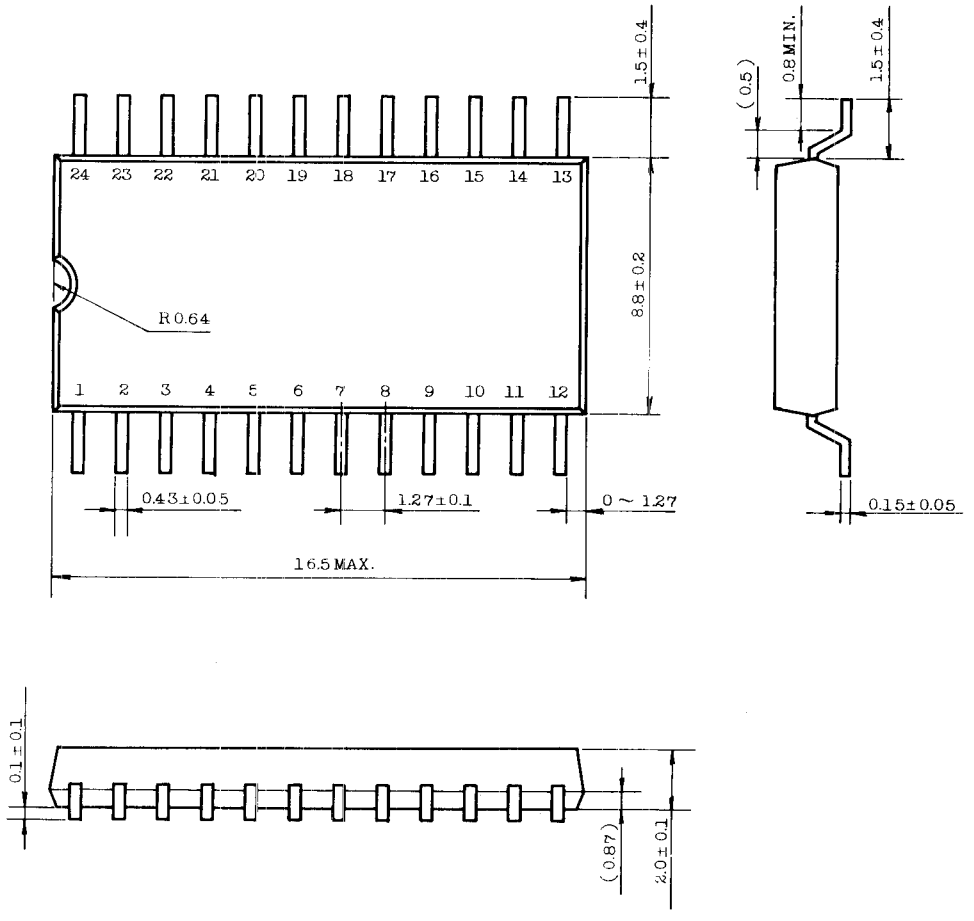
OUTLINE DRAWINGS

- Plastic DIP



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

● Plastic FP



Note : Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKGE INFORMATION FOR FLAT PACKAGE

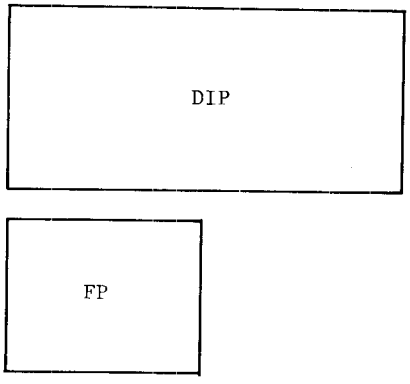
This new flat package is a very small and this compared with conventional standard dual-in-line package. Differences as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2, Comparison in occupied space



3. Advantage of this package
Small dimensions
Capability of High Density Assembly
Capability of thin Assembly ——
Capability of Assembly on both side of PC board.

4. PC pattern layout example