16,384 WORD x 4 BIT CMOS STATIC RAM

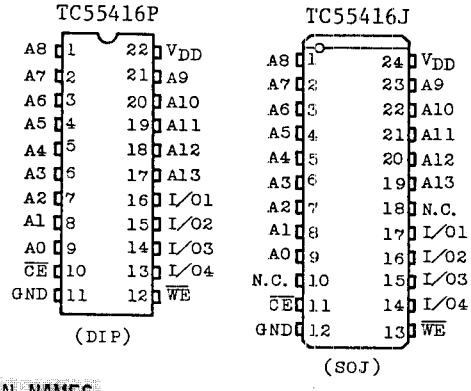
DESCRIPTION

The TC55416P/J is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 120mA/100mA/100mA at minimum cycle time.
The TC55416P/J also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 20mA.
The TC55416P/J is suitable for use in cache memory and high speed storage, where high speed/high density are required.
The TC55416P/J is moulded in a 22 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly.
The TC55416P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time:
  - TC55416P/J-25 25ns(MAX.)
  - TC55416P/J-35 35ns(MAX.)
  - TC55416P/J-45 45ns(MAX.)
- Low power dissipation:
  - Operation TC55416P/J-25 120mA(MAX.)
  - TC55416P/J-35 100mA(MAX.)
  - TC55416P/J-45 100mA(MAX.)
  - Standby 20mA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- Package:
  - 22 pin plastic 300mil DIP (TC55416P)
  - 24 pin plastic 300mil SOJ (TC55416J)

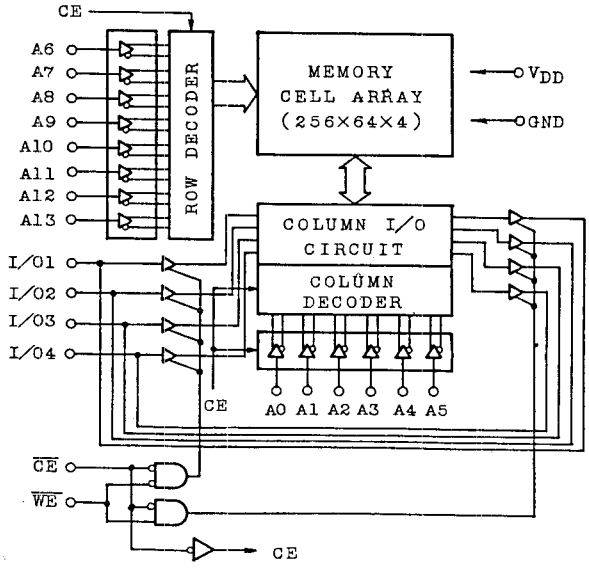
PIN CONNECTION



PIN NAMES

A0 ∿ A13	Address Inputs
I/01 ∿ I/04	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	$-0.5 \sim V_{DD}+0.5$	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	0~70	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO}	Operating Current	V_{DD}=5.5V t_{cycle}=Min cycle $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	-25	-	-	120	mA
			-35	-	-	100	
			-45	-	-	100	
I_{DDS1}	Standby Current	V_{DD}=5.5V, t_{cycle}=Min cycle $\overline{CE}=V_{IH}$, Other Input=V_{IH}/V_{IL}		-	-	20	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input=$V_{DD}-0.2V$ or 0.2V		-	-	1	

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	7	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	9	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55416P-25 TC55416J-25		TC55416P-35 TC55416J-35		TC55416P-45 TC55416J-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	ns
t_{CO}	Chip Enable Access Time	-	25	-	35	-	45	ns
t_{COE}	Chip Enable to Output in Low-Z	0	-	0	-	0	-	ns
t_{COD}	Chip Enable to Output in High-Z	-	15	-	15	-	20	ns
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	ns

Write Cycle

SYMBOL	PARAMETER	TC55416P-25 TC55416J-25		TC55416P-35 TC55416J-35		TC55416P-45 TC55416J-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{WP}	Write Pulse Width	20	-	30	-	35	-	ns
t_{CW}	Chip Enable to End of Write	20	-	30	-	35	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{ODW}	$\overline{WE}$ to Output High-Z	-	10	-	15	-	15	ns
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	-	0	-	0	-	ns
t_{DS}	Data Set Up Time	12	-	15	-	20	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns

A.C. TEST CONDITIONS

Input Pulse Levels	0.0V, 3.0V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.8V, 2.0V
Output Load	See Fig.1

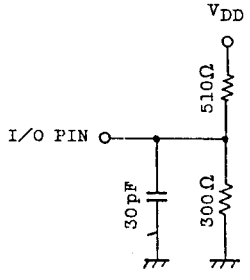
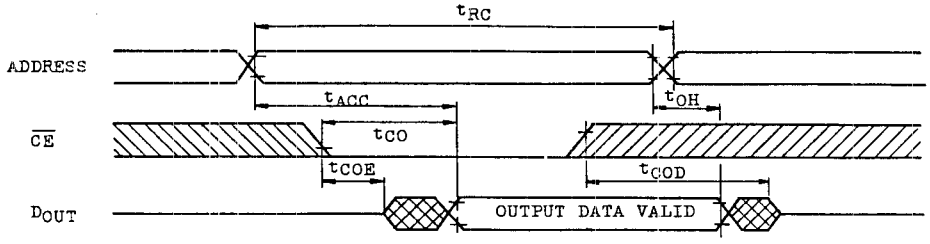


Fig.1 OUTPUT LOAD

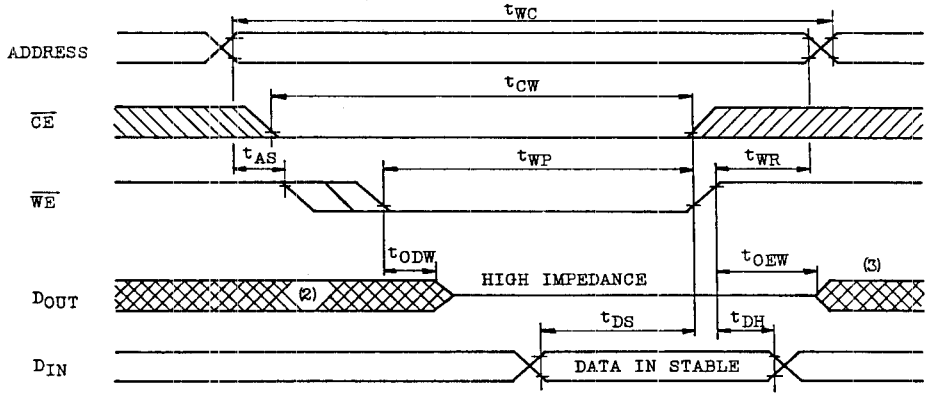
Note: In all condition, t_{COD} max is less than t_{COE} min both for a given device and from device to device.

TIMING WAVEFORMS

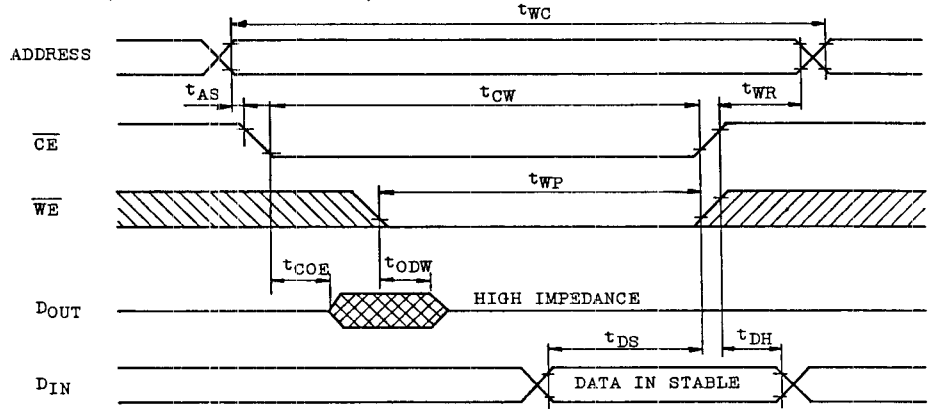
READ CYCLE(1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

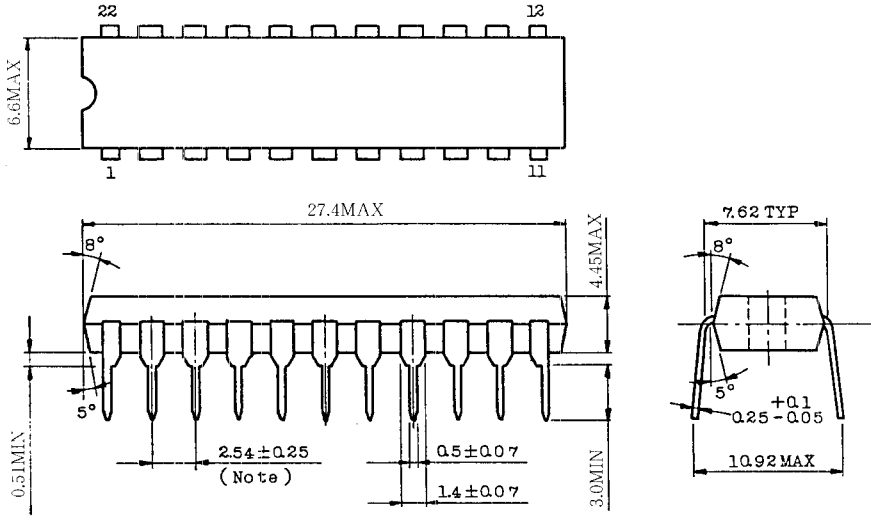


Note: 1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm

∘ Plastic DIP

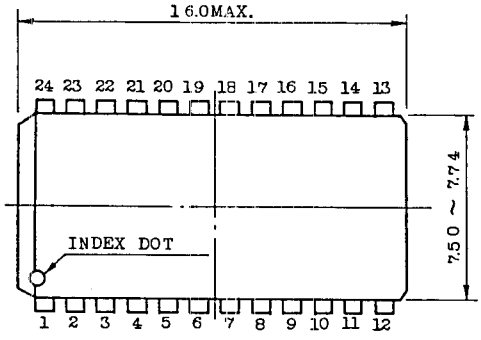


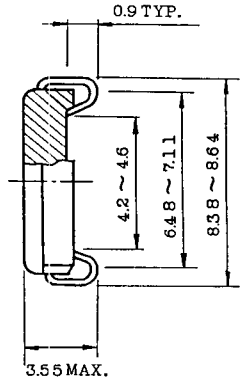
Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

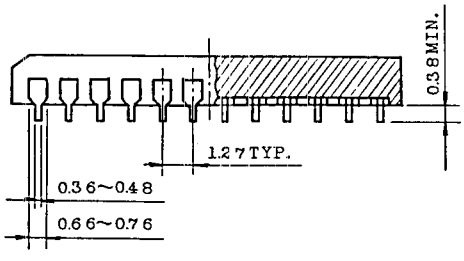
OUTLINE DRAWINGS

- Plastic SOJ

Unit in mm







Note: Each lead pitch is 1.27mm.
All leads are located within 0.12mm of the true longitudinal position with respect to No.1 and No.24 leads.