

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5561P/J-45, TC5561P/J-55
TC5561P/J-70

DESCRIPTION

The TC5561P/J is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and Operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45/55/70ns and maximum operating current of 100mA at minimum cycle time.

The TC5561P/J also features an automatic stand-by mode. When deselected by Chip Enable (CE), the operating current is reduced from 100mA to 100 μ A.

FEATURES

- Fast access time : TC5561P/J-45 45ns (MAX.)
TC5561P/J-55 55ns (MAX.)
TC5561P/J-70 70ns (MAX.)
- Low power dissipation : Operation 100mA (MAX.)
Standby 100 μ A (MAX.)
- 5V single power supply

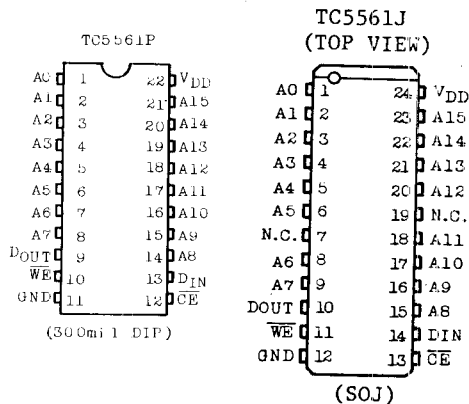
The TC5561P/J is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required.

The TC5561P is moulded in a 22 pin standard plastic SOJ with 300 mil width for high density surface assembly.

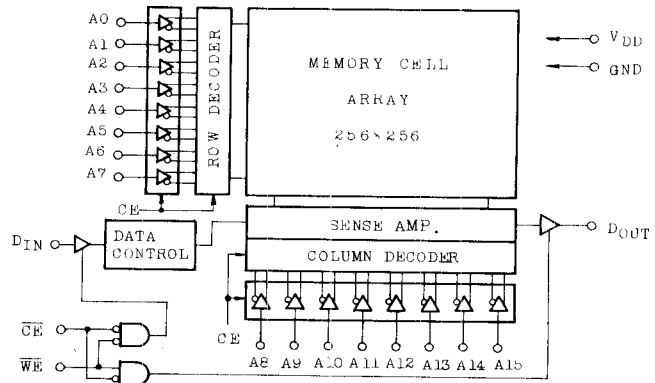
The TC5561P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

- Fully static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width: TC5561P
24 pin plastic 300 mil SOJ : TC5561J

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A ₀ ~A ₁₅	Address Inputs
D _{IN}	Data Input
D _{OUT}	Data Output
CE	Chip Enable Input
WE	Write Enable Input
V _{DD}	Power (+5V)
GND	Ground

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MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3~7.0	V
V _{IN}	Input Voltage	-2.0~7.0	V
V _{OUT}	Output Voltage	-0.5~V _{DD} +0.5	V
P _D	Power Dissipation	650	mW
T _{SOLDER}	Soldering Temperature	260·10	°C·sec
T _{STG}	Storage Temperature	-65~150	°C
T _{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	--	V _{DD} +0.3	V
V _{IL}	Input Low Voltage	-0.3	--	0.8	V
V _{DH}	Data Retention Supply Voltage	2.0	--	5.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} =0~V _{DD}	--	--	±1.0	μA
I _{OH}	Output High Current	V _{OH} =2.4V	-8	--	--	mA
I _{OL}	Output Low Current	V _{OL} =0.4V	8	--	--	mA
I _{LO}	Output Leakage Current	CE=V _{IH} or WE=V _{IL} V _{OUT} =0~V _{DD}	--	--	±1.0	μA
I _{DD0}	Operating Current	V _{DD} =5.5V, t _{cycle} =Min cycle, CE=V _{IL} Other Input=V _{IH} /V _{IL}	--	--	100	mA
I _{DD1}	Standby Current	CE=V _{IH}	--	--	2	mA
I _{DD2}		CE=V _{DD} -0.2V	--	--	100	μA

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} =GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

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A. C. CHARACTERISTICS (T_a=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5561P/J-45		TC5561P/J-55		TC5561P/J-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t _{ACC}	Address Access Time	—	45	—	55	—	70	
t _{CO}	Chip Enable Access Time	—	45	—	55	—	70	
t _{COE}	Chip Enable to Output in Low-Z	10	—	10	—	10	—	
t _{COD}	Chip Disable to Output in High-Z	—	15	—	15	—	15	
t _{OH}	Output Data Hold Time	5	—	5	—	5	—	

Write Cycle

SYMBOL	PARAMETER	TC5561P/J-45		TC5561P/J-55		TC5561P/J-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t _{WP}	Write Pulse Width	30	—	35	—	35	—	
t _{CW}	Chip Enable to End of Write	30	—	35	—	35	—	
t _{AS}	Address Set up Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{OE_W}	WE to Output Low-Z	0	—	0	—	0	—	
t _{OD_W}	WE to Output High-Z	—	15	—	15	—	15	
t _{DS}	Data Set up Time	25	—	25	—	30	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

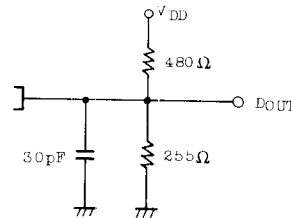
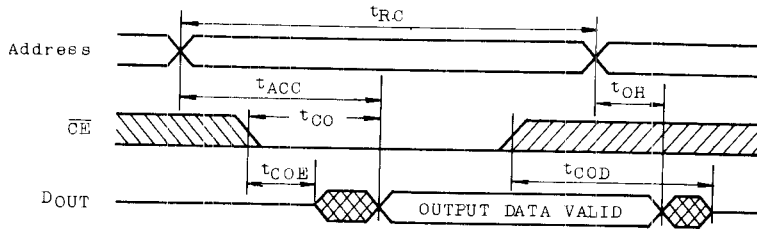


Fig.1 Output Load

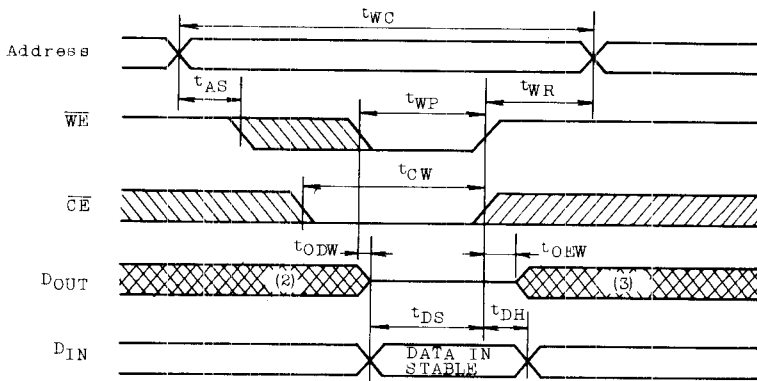
TC5561P/J-45, TC5561P/J-55 TC5561P/J-70

TIMING WAVEFORMS

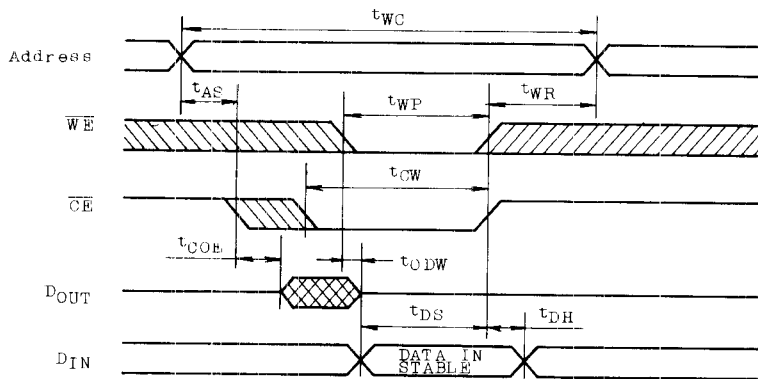
● READ CYCLE (1)



● WRITE CYCLE 1 (\overline{WE} Controlled Write)



● WRITE CYCLE 2 (\overline{CE} Controlled Write)



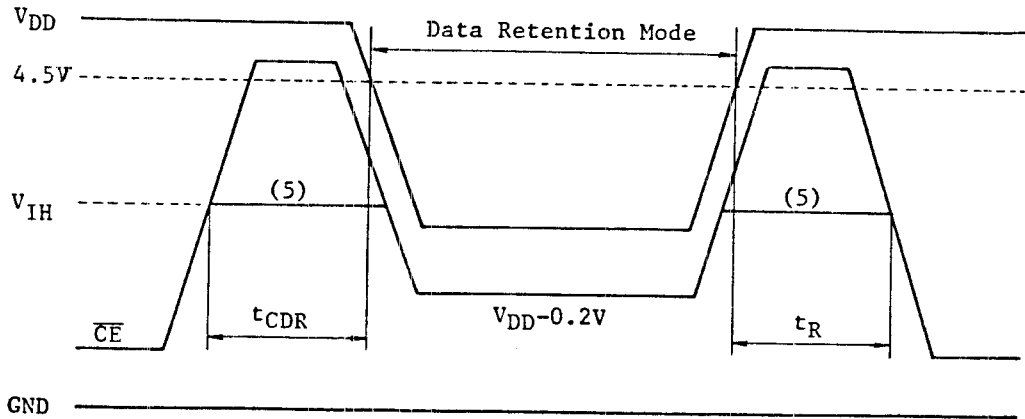
Note :

1. \overline{WE} is High for Read Cycle.
2. Assuming that \overline{CE} Low transit on occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
3. Assuming that \overline{CE} High transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
4. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

DATA RETENTION CHARACTERISTICS

(Ta = -40 ~ 50°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DR}	Data Retention Supply Voltage	2.0	—	5.5	V
I _{DRS2}	Standby Supply Current	V _{DD} = 3.0V	—	50	μA
		V _{DD} = 5.5V	—	100	μA
t _{CDH}	Chip Deselection to Data Retention Mode	0	—	—	μs
t _R	Recovery Time	t _{rc} (1)	—	—	μs

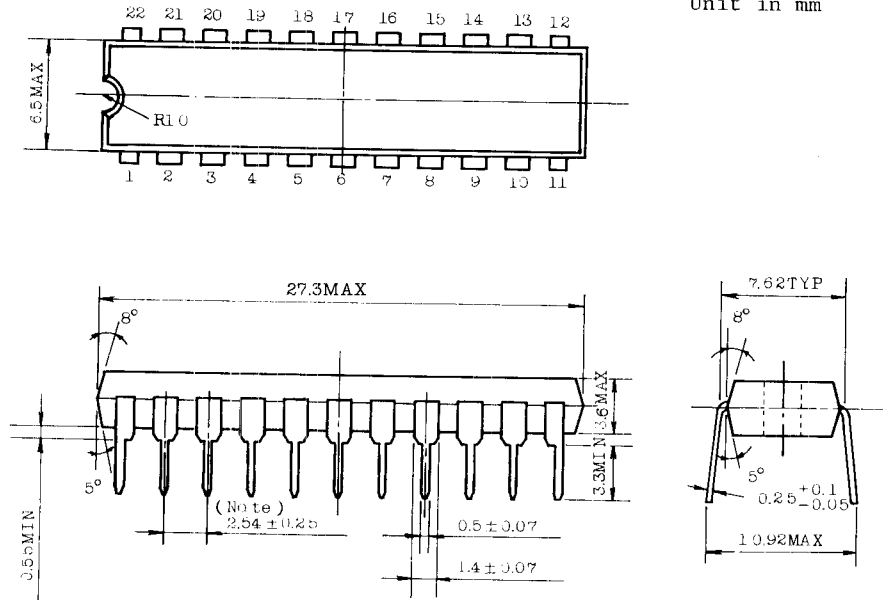


5. If the V_{IH} of \overline{CE}_1 is 2.2V in operation, I_{DRS1} current flows the period that V_{DD} voltage is going down from 4.5V to 2.5V.

**TC5561P/J-45, TC5561P/J-55
TC5561P/J-70**

OUTLINE DRAWINGS

Unit in mm

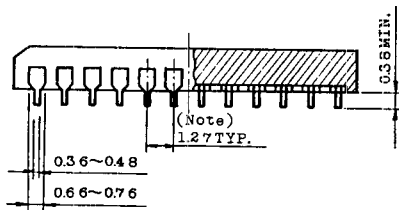
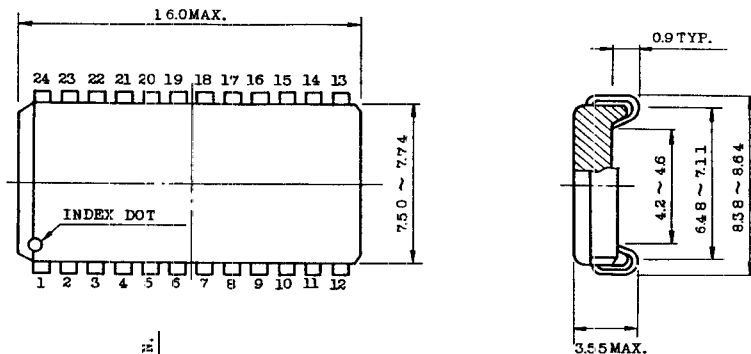


Note : Each lead pitch is 2.54 mm.

All leads are located within 0.25mm of the true longitudinal position with respect to No. 1 and No. 22 leads.

• Plastic SOJ

Unit in mm



Note: Each lead pitch is 1.27mm.

All leads are located within 0.12mm of the true longitudinal position with respect to No.1 and No.24 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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