

# TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD  $\times$  1 BIT CMOS STATIC RAM  
SILICON GATE CMOS

TC5562P/J-35, TC5562P/J-45  
TC5562P/J-55

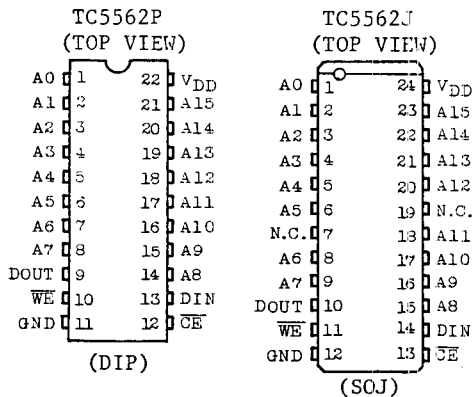
## DESCRIPTION

The TC5562P/J is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 100mA at minimum cycle time. The TC5562P/J also features and automatic standby mode. When deselected by chip Enable (CE), the operating current is reduced from 100mA to 20mA. The TC5562P/J is suitable for use in main memory of high speed computer and pattern memory, where high speed/high density are required. The TC5562P is moulded in a 22 pin plastic DIP with 300 mil width for high density surface assembly and the TC5562J is moulded in a 24 pin plastic SOJ with 300 mil width for high density surface assembly. The TC5562P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

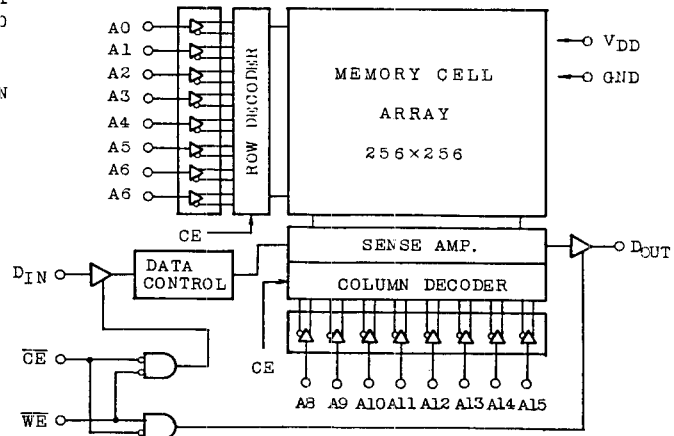
## FEATURES

- Fast access time: TC5562P/J-35 35ns(MAX.)  
TC5562P/J-45 45ns(MAX.)  
TC5562P/J-55 55ns(MAX.)
- Low power dissipation:  
Operation 100mA (MAX.)  
Standby 20mA (MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- I/O separate
- Package: 22 Pin Plastic 300 mil DIP : TC5562P  
24 Pin Plastic 300 mil SOJ : TC5562J

## PIN CONNECTION



## BLOCK DIAGRAM



## PIN NAMES

A0 ~ A15	Address Inputs
DIN	Data Input
DOUT	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V <sub>DD</sub>	Power (+5V)
GND	Ground
N.C.	No Connection

**MAXIMUM RATINGS**

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	V
V <sub>IN</sub>	Input Voltage	-2.0~7.0	V
V <sub>OUT</sub>	Output Voltage	-0.5~V <sub>DD</sub> +0.5	V
P <sub>D</sub>	Power Dissipator	650	mW
T <sub>SOLDER</sub>	Soldering Temperature	260 · 10	°C·sec
T <sub>STG</sub>	Storage Temperature	-65~150	°C
T <sub>OPR</sub>	Operating Temperature	0~70	°C

**D. C. RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-3.0	—	0.8	V

**D. C and OPERATING CHARACTERISTICS** (T<sub>a</sub>=0~70°C, V<sub>DD</sub>=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> =2.4V	-8	—	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> =0.4V	8	—	—	mA
I <sub>LO</sub>	Output Leakage Current	CE=V <sub>IH</sub> or WE=V <sub>IL</sub> V <sub>OUT</sub> =0~V <sub>DD</sub>	—	—	±1.0	μA
I <sub>DDO</sub>	Operating Current	V <sub>DD</sub> =5.5V, t <sub>cycle</sub> =Min cycle, CE=V <sub>IL</sub> Other Input=V <sub>IH</sub> /V <sub>IL</sub>	—	—	100	mA
I <sub>DDs1</sub>	Standby Current	CE=V <sub>IH</sub>	—	—	20	mA
I <sub>DDs2</sub>		CE=V <sub>DD</sub> -0.2V Other Input=V <sub>DD</sub> -0.2V or 0.2V	—	—	2	

**CAPACITANCE** (T<sub>a</sub>=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> =GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

# TC5562P/J-35, TC5562P/J-45 TC5562P/J-55

## A. C. CHARACTERISTICS (Ta=0~70°C, VDD=5V±10%)

### Read Cycle

SYMBOL	PARAMETER	TC5562P/J-35		TC5562P/J-45		TC5562P/J-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	35	—	45	—	55	—	ns
t <sub>ACC</sub>	Address Access Time	—	35	—	45	—	55	
t <sub>CO</sub>	Chip Enable Access Time	—	35	—	45	—	55	
t <sub>COE</sub>	Chip Enable to Output in Low-Z	5	—	5	—	5	—	
t <sub>COD</sub>	Chip Disable to Output in High-Z	—	15	—	15	—	15	
t <sub>OH</sub>	Output Data Hold Time	5	—	5	—	5	—	

### Write Cycle

SYMBOL	PARAMETER	TC5562P/J-35		TC5562P/J-45		TC5562P/J-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	35	—	45	—	55	—	ns
t <sub>WP</sub>	Write Pulse Width	25	—	30	—	35	—	
t <sub>CW</sub>	Chip Enable to End of Write	25	—	30	—	35	—	
t <sub>AS</sub>	Address Set up Time	0	—	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	
t <sub>OE<sub>W</sub></sub>	WE to Output Low-Z	0	—	0	—	0	—	
t <sub>OD<sub>W</sub></sub>	WE to Output High-Z	—	15	—	15	—	15	
t <sub>DS</sub>	Data Set up Time	20	—	25	—	25	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	

## A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

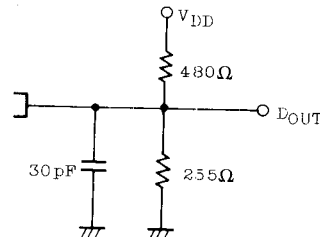
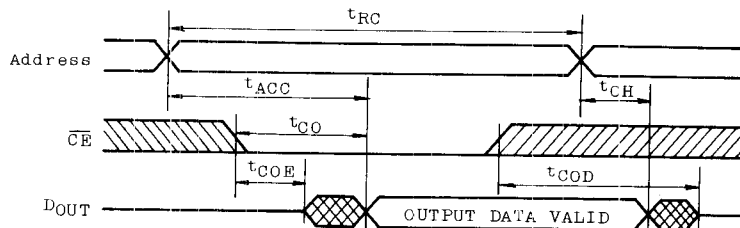


Fig.1 Output Load

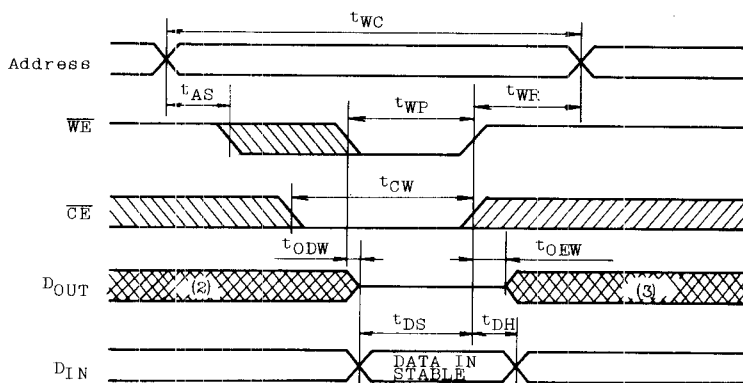
# TC5562P/J-35, TC5562P/J-45 TC5562P/J-55

## TIMING WAVEFORMS

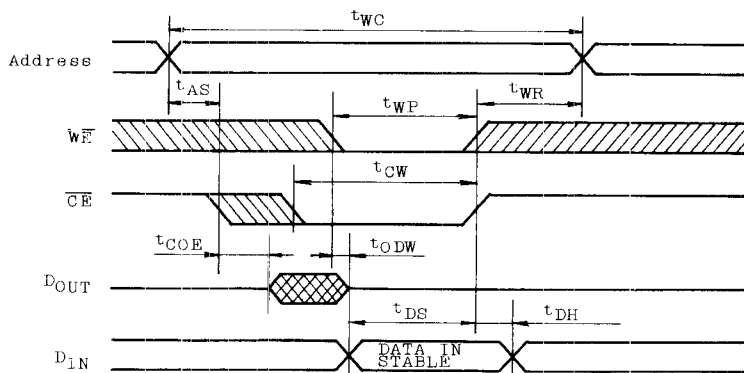
### ● READ CYCLE (1)



### ● WRITE CYCLE 1 ( $\overline{WE}$ Controlled Write)



### ● WRITE CYCLE 2 ( $\overline{CE}$ Controlled Write)

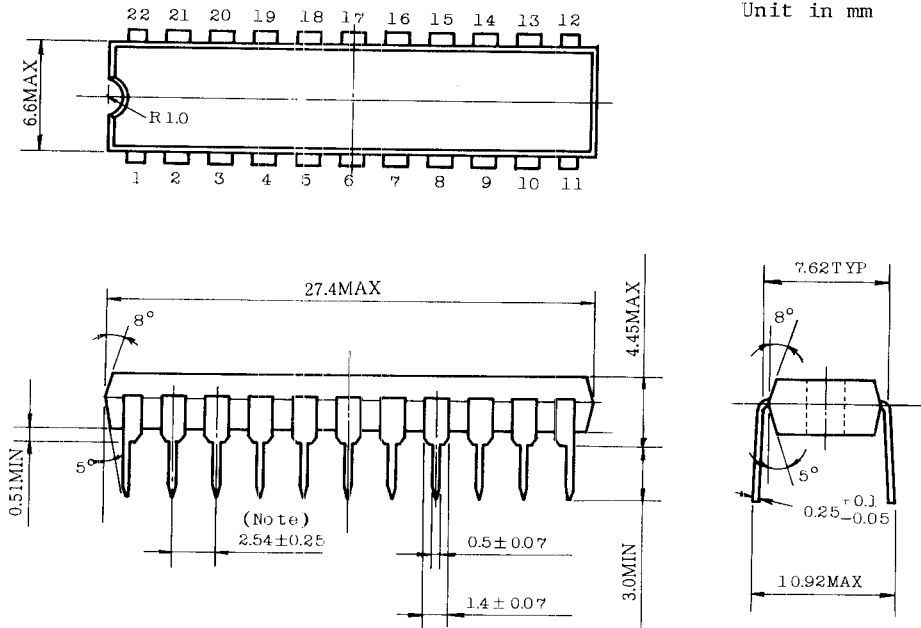


Note :

1.  $\overline{WE}$  is High for Read Cycle.
2. Assuming that  $\overline{CE}$  Low transition occurs coincident with or after  $\overline{WE}$  Low transition, Outputs remain in a high impedance state.
3. Assuming that  $\overline{CE}$  High transition occurs coincident with or prior  $\overline{WE}$  High transition, Outputs remain in a high impedance state.
4. The operating temperature ( $T_a$ ) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

# TC5562P/J-35, TC5562P/J-45 TC5562P/J-55

## OUTLINE DRAWINGS



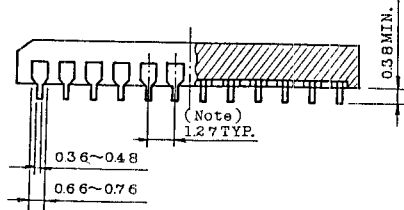
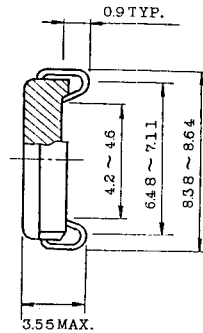
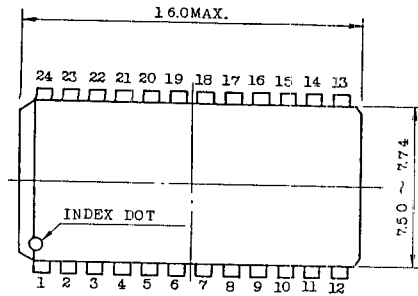
Note : Each lead pitch is 2.54mm.

All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

# TC5562P/J-35, TC5562P/J-45 TC5562P/J-55

• Plastic SOJ

Unit in mm



Note: Each lead pitch is 1.27mm.

All leads are located within 0.12mm of the true longitudinal position with respect to No. 1 and No. 24 leads.

Note: Toshiba does not assume any responsibility for use of any circuit described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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