65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5562P/J-35, TC5562P/J-45
TC5562P/J-55

DESCRIPTION

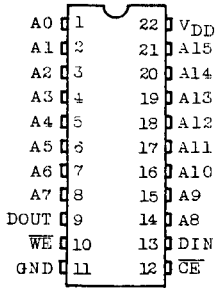
The TC5562P/J is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 100mA at minimum cycle time. The TC5562P/J also features and automatic standby mode. When deselected by chip Enable (CE), the operating current is reduced from 100mA to 20mA. The TC5562P/J is suitable for use in main memory of high speed computer and pattern memory, where high speed/high density are required. The TC5562P is moulded in a 22 pin plastic DIP with 300 mil width for high density surface assembly and the TC5562J is moulded in a 24 pin plastic SOJ with 300 mil width for high density surface assembly. The TC5562P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time: TC5562P/J-35 35ns(MAX.)
  TC5562P/J-45 45ns(MAX.)
  TC5562P/J-55 55ns(MAX.)
- Low power dissipation:
  Operation 100mA (MAX.)
  Standby 20mA (MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- I/O separate
- Package: 22 Pin Plastic 300 mil DIP : TC5562P
  24 Pin Plastic 300 mil SOJ : TC5562J

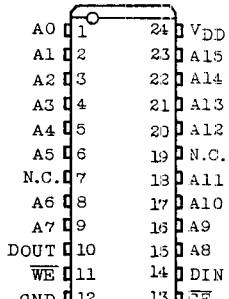
PIN CONNECTION

TC5562P
(TOP VIEW)



(DIP)

TC5562J
(TOP VIEW)

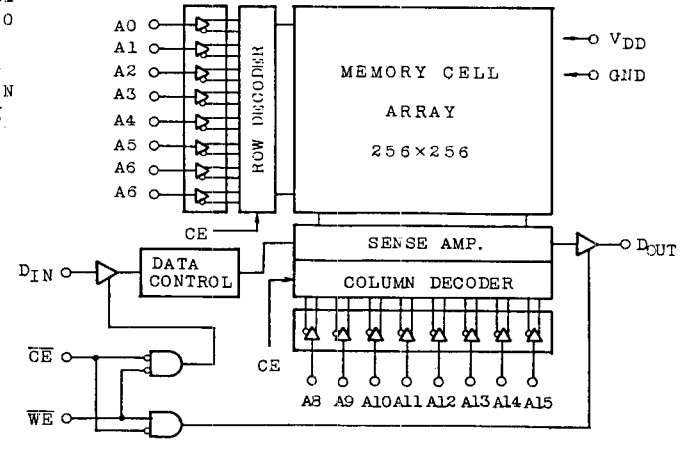


(SOJ)

PIN NAMES

A0 ∿ A15	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V

D. C and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$	--	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	−8	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0\sim V_{DD}$	—	—	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, tcycle=Min cycle, $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	—	—	20	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input=$V_{DD}-0.2V$ or $0.2V$	—	—	2	

CAPACITANCE

($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC5562P/J-35		TC5562P/J-45		TC5562P/J-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	–	45	–	55	–	ns
t_{ACC}	Address Access Time	–	35	–	45	–	55	
t_{CO}	Chip Enable Access Time	–	35	–	45	–	55	
t_{COE}	Chip Enable to Output in Low-Z	5	–	5	–	5	–	
t_{COD}	Chip Disable to Output in High-Z	–	15	–	15	–	15	
t_{OH}	Output Data Hold Time	5	–	5	–	5	–	

Write Cycle

SYMBOL	PARAMETER	TC5562P/J-35		TC5562P/J-45		TC5562P/J-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	–	45	–	55	–	ns
t_{WP}	Write Pulse Width	25	–	30	–	35	–	
t_{CW}	Chip Enable to End of Write	25	–	30	–	35	–	
t_{AS}	Address Set up Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{OEW}	WE to Output Low-Z	0	–	0	–	0	–	
t_{ODW}	WE to Output High-Z	–	15	–	15	–	15	
t_{DS}	Data Set up Time	20	–	25	–	25	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

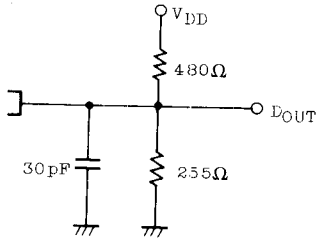
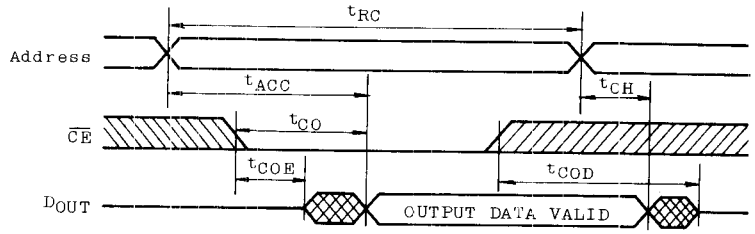


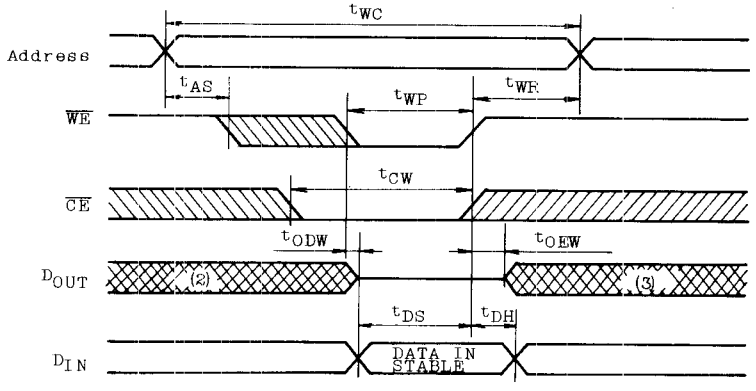
Fig.1 Output Load

TIMING WAVEFORMS

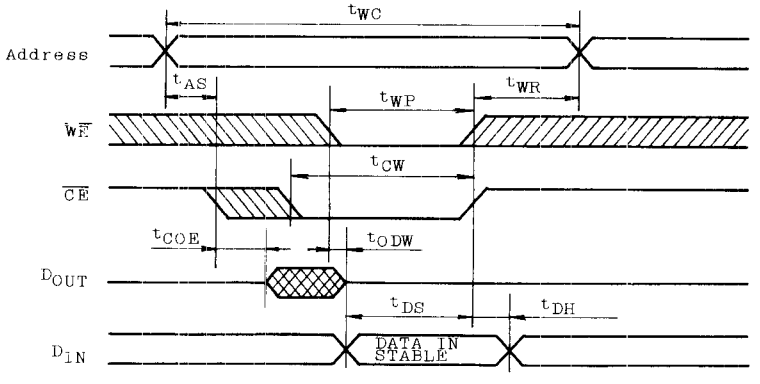
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

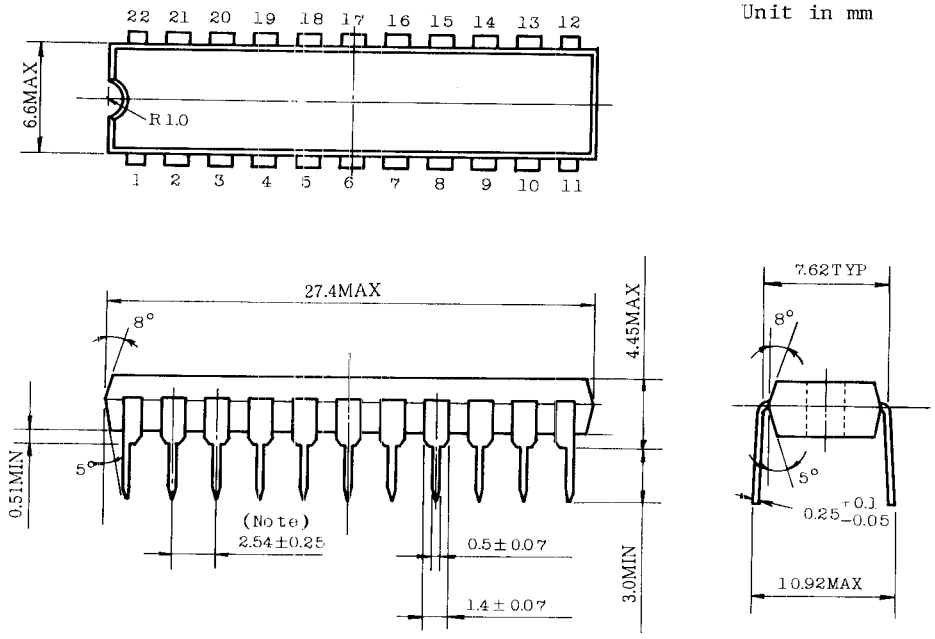


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) ir guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

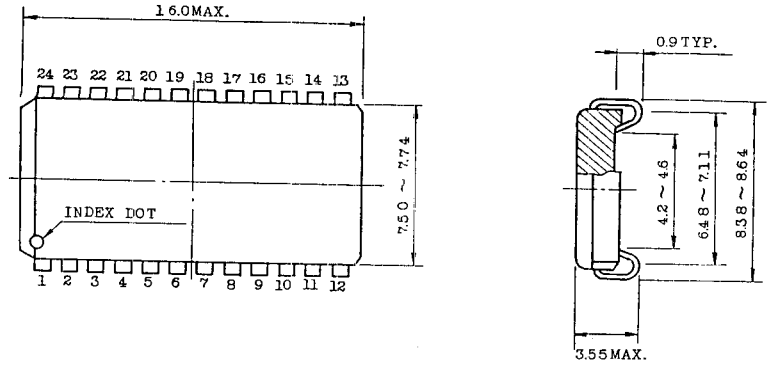
Unit in mm

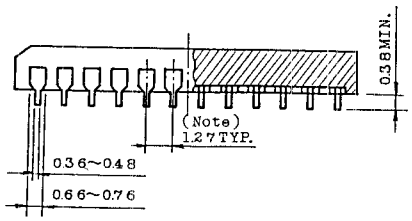


Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

• Plastic SOJ

Unit in mm





Note: Each lead pitch is 1.27mm.
All leads are located within 0.12mm of the ture longitudinal position with respect to No. 1 and No. 24 leads.