





### E32D1 H E C 2 K -156.250M

Series — RoHS Compliant (Pb-free) 3.3V 6 Pad 5mm x 7mm Ceramic SMD LVPECL VCXO

#50ppm Maximum over -40°C to +85°C

Frequency Deviation ±75ppm Minimum

> Linearity —— 10% Maximum

Nominal Frequency 156.250MHz

Logic Control / Additional Output Tri-State (Enable Low) / Complementary Output

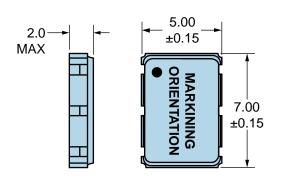
- Duty Cycle 50% ±5%

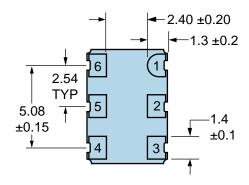
#50ppm Maximum over -40°C to +85°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change 1st Year Aging at 25°C, Shock, and Vibration.)  **Supply Voltage**  3.3Vdc ±5%*  Input Current**  100mA Maximum (with Load)  Output Voltage Logic High (Voh)  Vcc-1.025Vdc Minimum  Output Voltage Logic Low (Vol)  Vcc-1.620Vdc Maximum  Rise/Fall Time**  1.5nSec Maximum (Measured over 20% to 80% of waveform)  Duty Cycle  50% ±5% (Measured at 50% of waveform)  Duty Cycle  50% ±5% (Measured at 50% of waveform)  Output Voltage Logic Low (Vol)  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range  0.0Vdc to Vcc +0.5Vdc  Frequency Deviation  #75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity  10% Maximum  Transfer Function  Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  50kOhms Typical  Phase Noise  55dBc/Hz at 10Hz offset, -90dBc/Hz at 10Hz offset, -120dBc/Hz at 11kHz offset, -140dBc/Hz at 10kHz offset, -146dBc/Hz at 11kHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State Input Voltage (Vih and Vil)  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tri)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tris)  4pSec Typical, 5pSec Maximum Deterministic Jitter  Period Jitter (tpp)  27pSec Typical, 4pSec Maximum Deterministic Jitter  Period Jitter (tpp)  47pSec Typical, 4pSec Maximum Deterministic Jitter  10mSec Maximum	ELECTRICAL SPECIFICAT	TIONS
Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change 1st Year Aging at 25°C, Shock, and Vibration.)  Supply Voltage Input Current  100mA Maximum (with Load)  Output Voltage Logic High (Voh)  Voc-1.025Vdc Minimum  Output Voltage Logic Low (Vol)  Voc-1.026Vdc Maximum  Rise/Fall Time  1.5nSec Maximum (Measured over 20% to 80% of waveform)  Duty Cycle  50% ±5% (Measured at 50% of waveform)  Load Drive Capability  50 Ohms into Voc-2.0Vdc  Output Logic Type  LVPECL  Control Voltage Range  0.0Vdc to Voc +0.5Vdc  Frequency Deviation  ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity  10% Maximum  Transfer Function  Modulation Bandwidth  10kHz Minimum (Measured at 3dB with a control voltage of +1.65Vdc)  Input Impedance  Phase Noise  56dBcHz at 10Hz offset, -90dBcHz at 100Hz offset, -120dBcHz at 1kHz offset, -140dBc/Hz at 10kHz offset, -148dBc/Hz at 10kHz (Typical Values, Fc=155.520MHz)  Logic Control / Additional Output  Tri-State Input Voltage (Vih and Vil)  Vin of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Cutputs  Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trr)  9pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trp)  27pSec Typical, 5pSec Maximum Deterministic Jitter  Period Jitter (tp-)  Start Up Time	Nominal Frequency	156.250MHz
Input Current  100mA Maximum (with Load)  Output Voltage Logic High (Voh)  Vcc-1.025Vdc Minimum  Output Voltage Logic Low (Vol)  Vcc-1.620Vdc Maximum  Rise/Fall Time  1.5nSec Maximum (Measured over 20% to 80% of waveform)  Duty Cycle  50% ±5% (Measured at 50% of waveform)  Load Drive Capability  50 Ohms into Vcc-2.0Vdc  Output Logic Type  LVPECL  Control Voltage  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range  0.0Vdc to Vcc +0.5Vdc  Frequency Deviation  Linearity  10% Maximum  Transfer Function  Positive Transfer Characteristic  Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  Phase Noise  55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 11kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 110kHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State Input Voltage (Vih and Vil)  Tri-State Input Voltage (Vih and Vil)  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (ttr)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (ttp)  27pSec Typical, 40pSec Maximum Deterministic Jitter  Period Jitter (ttp)  27pSec Typical, 40pSec Maximum Deterministic Jitter  Period Jitter (ttp)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution	Frequency Tolerance/Stability	Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change,
Output Voltage Logic High (Voh)  Output Voltage Logic Low (Vol)  Rise/Fall Time  1.5nSec Maximum (Measured over 20% to 80% of waveform)  Duty Cycle  50% ±5% (Measured at 50% of waveform)  Load Drive Capability  50 Ohms into Voc-2.0Vdc  Output Logic Type  LVPECL  Control Voltage  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range  0.0Vdc to Vcc +0.5Vdc  Frequency Deviation  ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity  10% Maximum  Transfer Function  Positive Transfer Characteristic  Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  50kChms Typical  -55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 11kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 10wHz offset, -15dBc/Hz at 10wHz offset, -145dBc/Hz at 10wHz offset, -145dBc/Hz a	Supply Voltage	3.3Vdc ±5%
Output Voltage Logic Low (Vol)         Vcc-1.620Vdc Maximum           Rise/Fall Time         1.5nSec Maximum (Measured over 20% to 80% of waveform)           Duty Cycle         50% ±5% (Measured at 50% of waveform)           Load Drive Capability         50 Ohms into Vcc-2.0Vdc           Output Logic Type         LVPECL           Control Voltage         1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)           Control Voltage Range         0.0Vdc to Vcc +0.5Vdc           Frequency Deviation         ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)           Linearity         10% Maximum           Transfer Function         Positive Transfer Characteristic           Modulation Bandwidth         10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)           Input Impedance         50kOhms Typical           Phase Noise         -55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 11kHz offset, -140dBc/Hz at 10kHz offset, -146dBc/Hz at 100kHz offset, -148dBc/Hz at 10kHz (Typical Values, Fo=155.520MHz)           Logic Control / Additional Output         Tri-State (Inable Low) / Complementary Output           Tri-State Input Voltage (Vin and Vil)         Vin of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs           RMS Phase Jitter         0.4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution	Input Current	100mA Maximum (with Load)
Rise/Fall Time 1.5nSec Maximum (Measured over 20% to 80% of waveform)  Duty Cycle 50% ±5% (Measured at 50% of waveform)  Load Drive Capability 50 Ohms into Vcc-2.0Vdc  Output Logic Type LVPECL  Control Voltage 1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range 0.0Vdc to Vcc +0.5Vdc  Frequency Deviation ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity 10% Maximum  Transfer Function Positive Transfer Characteristic  Modulation Bandwidth 10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance 50kOhms Typical  Phase Noise 55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -148dBc/Hz at 10OkHz offset, -148dBc/Hz at 10OkHz offset, 20thz at 10kHz offset, -148dBc/Hz at 10OkHz offset, at 14kHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vil) Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter 0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc) 4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms) 3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms) 4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p) 27pSec Typical, 40pSec Maximum Deterministic Jitter  Period Jitter (tp-p) 27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution	Output Voltage Logic High (Voh)	Vcc-1.025Vdc Minimum
Duty Cycle 50% ±5% (Measured at 50% of waveform)  Load Drive Capability 50 Ohms into Vcc-2.0Vdc  Output Logic Type LVPECL  Control Voltage 1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range 0.0Vdc to Vcc +0.5Vdc  Frequency Deviation ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity 10% Maximum  Transfer Function Positive Transfer Characteristic  Modulation Bandwidth 10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance 50kOhms Typical  Phase Noise 55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 14kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 10kHz offset, -120dBc/Hz at 10kHz offset, -145dBc/Hz at 10kHz offset, -145dBc/Hz at 10kHz offset, -120dBc/Hz at 10kHz offset, -120dBc	Output Voltage Logic Low (Vol)	Vcc-1.620Vdc Maximum
Load Drive Capability  50 Ohms into Vcc-2.0Vdc  Output Logic Type  LVPECL  Control Voltage  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range  0.0Vdc to Vcc +0.5Vdc  Frequency Deviation  ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity  10% Maximum  Transfer Function  Positive Transfer Characteristic  Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  Phase Noise  50kOhms Typical  55dBc/Hz at 10Hz offset, -90dBc/Hz at 10Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 10kHz offset, -146dBc/Hz at 10kHz offset, -120dBc/Hz at 10kHz offset, -140dBc/Hz at 10kHz offset, -146dBc/Hz at 10kHz offset, -120dBc/Hz at 10kHz offset, -146dBc/Hz at 10kHz offset, -146dBc/Hz at 10kHz offset, -146dBc/Hz at 10kHz offset, -120dBc/Hz at 10kHz offset, -146dBc/Hz at 10kHz	Rise/Fall Time	1.5nSec Maximum (Measured over 20% to 80% of waveform)
Output Logic Type  LVPECL  Control Voltage  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range  0.0Vdc to Vcc +0.5Vdc  Frequency Deviation  ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity  10% Maximum  Transfer Function  Positive Transfer Characteristic  Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  Phase Noise  50kOhms Typical  Phase Noise  55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State Input Voltage (Vih and Vii)  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  4pSec Typical, 1pSec Maximum Deterministic Jitter  Period Jitter (tdj)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution	Duty Cycle	50% ±5% (Measured at 50% of waveform)
Control Voltage  1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)  Control Voltage Range  0.0Vdc to Vcc +0.5Vdc  Frequency Deviation  ±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity  10% Maximum  Transfer Function  Positive Transfer Characteristic  Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  50kOhms Typical  Phase Noise  -55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1KHz offset, -140dBc/Hz at 10kHz offset, -148dBc/Hz at 100kHz offset, -148dBc/Hz at 10kHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vil)  Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (ttms)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tdj)  4pSec Typical, 40pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution	Load Drive Capability	50 Ohms into Vcc-2.0Vdc
Control Voltage Range  0.0Vdc to Vcc +0.5Vdc  Frequency Deviation  10% Maximum  Transfer Function  Positive Transfer Characteristic  Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  50kOhms Typical  Phase Noise  -55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 1	Output Logic Type	LVPECL
#75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)  Linearity 10% Maximum  Transfer Function Positive Transfer Characteristic  Modulation Bandwidth 10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance 50kOhms Typical  Phase Noise -55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vil) Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter 0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc) 4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trrj) 3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms) 3pSec Typical, 1pSec Maximum Deterministic Jitter  Period Jitter (tdj) 4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tpp) 27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time 10mSec Maximum	Control Voltage	1.65Vdc ±1.65Vdc (Test Conditions for Frequency Deviation)
Linearity 10% Maximum  Transfer Function Positive Transfer Characteristic  Modulation Bandwidth 10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance 50kOhms Typical  Phase Noise -55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vii) Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter 0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc) 4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trij) 3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj) 4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p) 27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time 10mSec Maximum	Control Voltage Range	0.0Vdc to Vcc +0.5Vdc
Transfer Function Positive Transfer Characteristic  Modulation Bandwidth 10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc) Input Impedance 50kOhms Typical  Phase Noise -55dBc/Hz at 10Hz offset, -90dBc/Hz at 10Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vil) Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter 0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc) 4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms) 3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj) 4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p) 27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time 10mSec Maximum	Frequency Deviation	±75ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)
Modulation Bandwidth  10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)  Input Impedance  50kOhms Typical  -55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vil)  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trj)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time	Linearity	10% Maximum
Input Impedance  50kOhms Typical  Phase Noise  -55dBc/Hz at 10Hz offset, -90dBc/Hz at 10Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vil)  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time  50kOhms Typical 50kOhms Typic	Transfer Function	Positive Transfer Characteristic
Phase Noise  -55dBc/Hz at 10Hz offset, -90dBc/Hz at 10Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State (Enable Low) / Complementary Output  Tri-State Input Voltage (Vih and Vil)  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trij)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time	Modulation Bandwidth	10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)
offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)  Logic Control / Additional Output  Tri-State (Enable Low) / Complementary Output  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trj)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time  10mSec Maximum	Input Impedance	50kOhms Typical
Tri-State Input Voltage (Vih and Vil)  Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs  RMS Phase Jitter  0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trj)  3pSec Typical, 5pSec Maximum Sigma of Random Jitter  Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time  10mSec Maximum	Phase Noise	
Connect to Enable Outputs  RMS Phase Jitter 0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)  Accumulated Period Jitter (tacc) 4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trj) 3pSec Typical, 5pSec Maximum Sigma of Random Jitter  Period Jitter (trms) 3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj) 4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p) 27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time 10mSec Maximum	Logic Control / Additional Output	Tri-State (Enable Low) / Complementary Output
Accumulated Period Jitter (tacc)  4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (trj)  3pSec Typical, 5pSec Maximum Sigma of Random Jitter  Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time  10mSec Maximum	Tri-State Input Voltage (Vih and Vil)	
Period Jitter (trj)       3pSec Typical, 5pSec Maximum Sigma of Random Jitter         Period Jitter (trms)       3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution         Period Jitter (tdj)       4pSec Typical, 10pSec Maximum Deterministic Jitter         Period Jitter (tp-p)       27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution         Start Up Time       10mSec Maximum	RMS Phase Jitter	0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)
Period Jitter (trms)  3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution  Period Jitter (tdj)  4pSec Typical, 10pSec Maximum Deterministic Jitter  Period Jitter (tp-p)  27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time  10mSec Maximum	Accumulated Period Jitter (tacc)	4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution
Period Jitter (tdj) 4pSec Typical, 10pSec Maximum Deterministic Jitter Period Jitter (tp-p) 27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution Start Up Time 10mSec Maximum	Period Jitter (trj)	3pSec Typical, 5pSec Maximum Sigma of Random Jitter
Period Jitter (tp-p) 27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution  Start Up Time 10mSec Maximum	Period Jitter (trms)	3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution
Start Up Time 10mSec Maximum	Period Jitter (tdj)	4pSec Typical, 10pSec Maximum Deterministic Jitter
· · · · · · · · · · · · · · · · · · ·	Period Jitter (tp-p)	27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution
Storage Temperature Range -55°C to +125°C	Start Up Time	10mSec Maximum
otorago remperaturo rungo	Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS		
Fine Leak Test	MIL-STD-883, Method 1014 Condition A	
Gross Leak Test	MIL-STD-883, Method 1014 Condition C	
Mechanical Shock	MIL-STD-202, Method 213 Condition C	
Resistance to Soldering Heat	MIL-STD-202, Method 210	
Resistance to Solvents	MIL-STD-202, Method 215	
Solderability	MIL-STD-883, Method 2003	
Temperature Cycling	MIL-STD-883, Method 1010	
Vibration	MIL-STD-883, Method 2007 Condition A	



### **MECHANICAL DIMENSIONS (all dimensions in millimeters)**



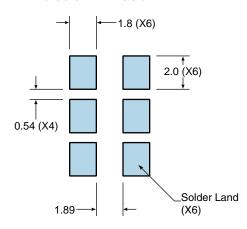


PIN	CONNECTION
1	Voltage Control
2	Tri-State
3	Case/Ground
4	Output
5	Complementary Output
6	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	156.25M
3	XXYZZ XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year

#### **Suggested Solder Pad Layout**

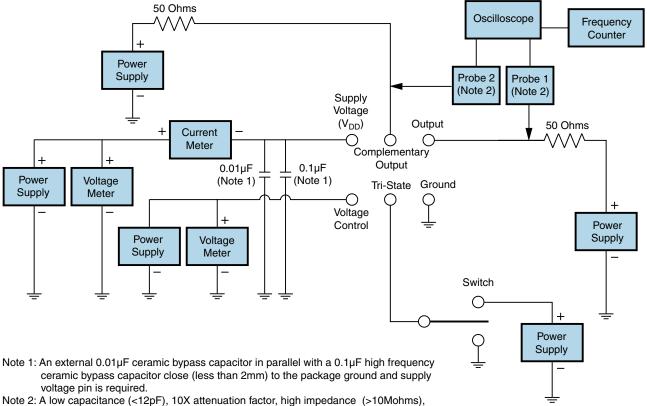
All Dimensions in Millimeters



All Tolerances are ±0.1



#### **Test Circuit for Tri-State and Complementary Output**



and high bandwidth (>500MHz) passive probe is recommended.

Note 3: Test circuit PCB traces need to be designed for a characteristic line impedance of 50 ohms.



### **Recommended Solder Reflow Methods**



### **High Temperature Infrared/Convection**

T <sub>s</sub> MAX to T <sub>∟</sub> (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (T <sub>s</sub> MIN)	150°C
- Temperature Typical (T <sub>s</sub> TYP)	175°C
- Temperature Maximum (T <sub>S</sub> MAX)	200°C
- Time (t <sub>s</sub> MIN)	60 - 180 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T <sub>P</sub> )	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T <sub>P</sub> Target)	250°C +0/-5°C
Time within 5°C of actual peak (t <sub>p</sub> )	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1



### **Recommended Solder Reflow Methods**



#### Low Temperature Infrared/Convection 240°C

T <sub>S</sub> MAX to T <sub>L</sub> (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T <sub>s</sub> MIN)	N/A
- Temperature Typical (T <sub>s</sub> TYP)	150°C
- Temperature Maximum (T <sub>s</sub> MAX)	N/A
- Time (t <sub>s</sub> MIN)	60 - 120 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T <sub>P</sub> )	240°C Maximum
Target Peak Temperature (T <sub>P</sub> Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (tp)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

#### **Low Temperature Manual Soldering**

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

#### **High Temperature Manual Soldering**

260°C Maximum for 5 seconds Maximum, 2 times Maximum.