

# 10A+ Switch-Mode Power Supply with LDO Regulator

The 34703 integrated power supply IC is designed to support the PowerQUICC™ family of MCUs as well as other MCUs and DSPs requiring a high current core supply. The 34703 incorporates a high-performance switching regulator for the microprocessor's core supply, and a low-dropout (LDO) linear regulator control circuit to provide I/O and bus voltage.

The switching regulator is an efficient synchronous buck converter with integrated low  $R_{DS(ON)}$  high side and low side FETs. Temperature and current sensing is built in and provides protection for the IC as well as the external circuitry.

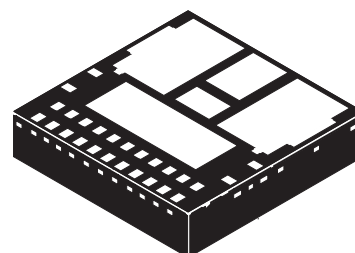
The 34703 incorporates specific advanced protection features for use with high power processors and controllers, including power-up and power-down sequencing of the I/O and core supply voltages in relation to each other.

## Features

- Wide input Operating Voltage Range: 2.8 V to 13.5 V
- Adjustable Output Voltages
- Continuous Core Voltage Supply Currents up to 10 A (with infrequent excursions to 12 A permitted)
- Undervoltage Lockout
- Selectable Power Sequencing
- Programmable Watchdog Timer
- Voltage Margining via I<sup>2</sup>C Bus
- Overcurrent Protection
- Reset with Programmable Power-ON Delay

**34703**

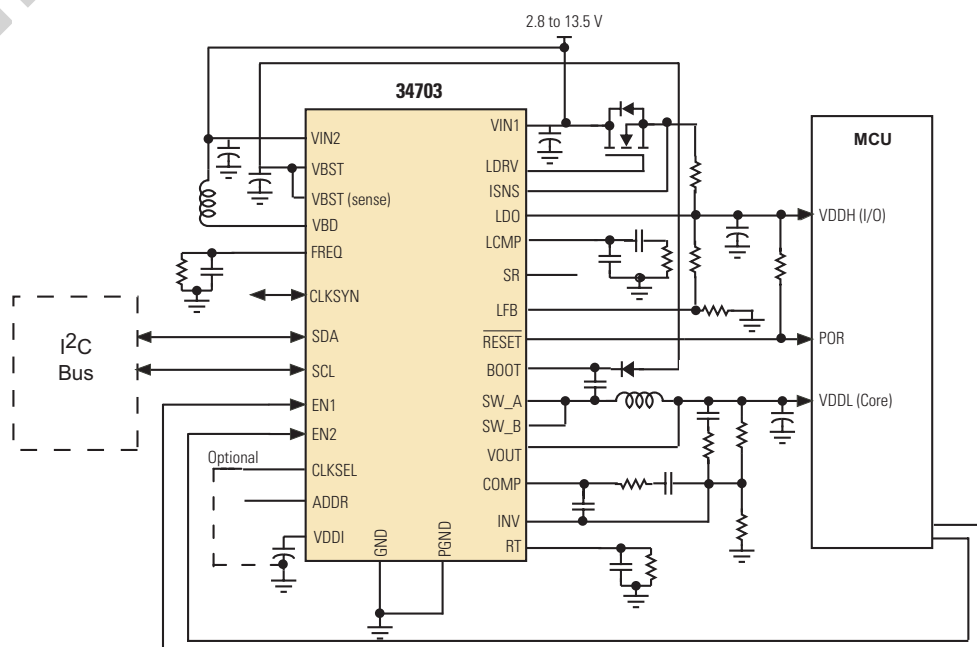
**\* INTEGRATED POWER SUPPLY IC**



**PNB SUFFIX  
98ASA10705D  
33-PIN PQFN**

## ORDERING INFORMATION

Device	Temperature Range (T <sub>A</sub> )	Package
MC34703PNB/R2	-40 to 85°C	33 PQFN



**Figure 1. MC34703 Simplified Application Diagram**

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

## INTERNAL BLOCK DIAGRAM

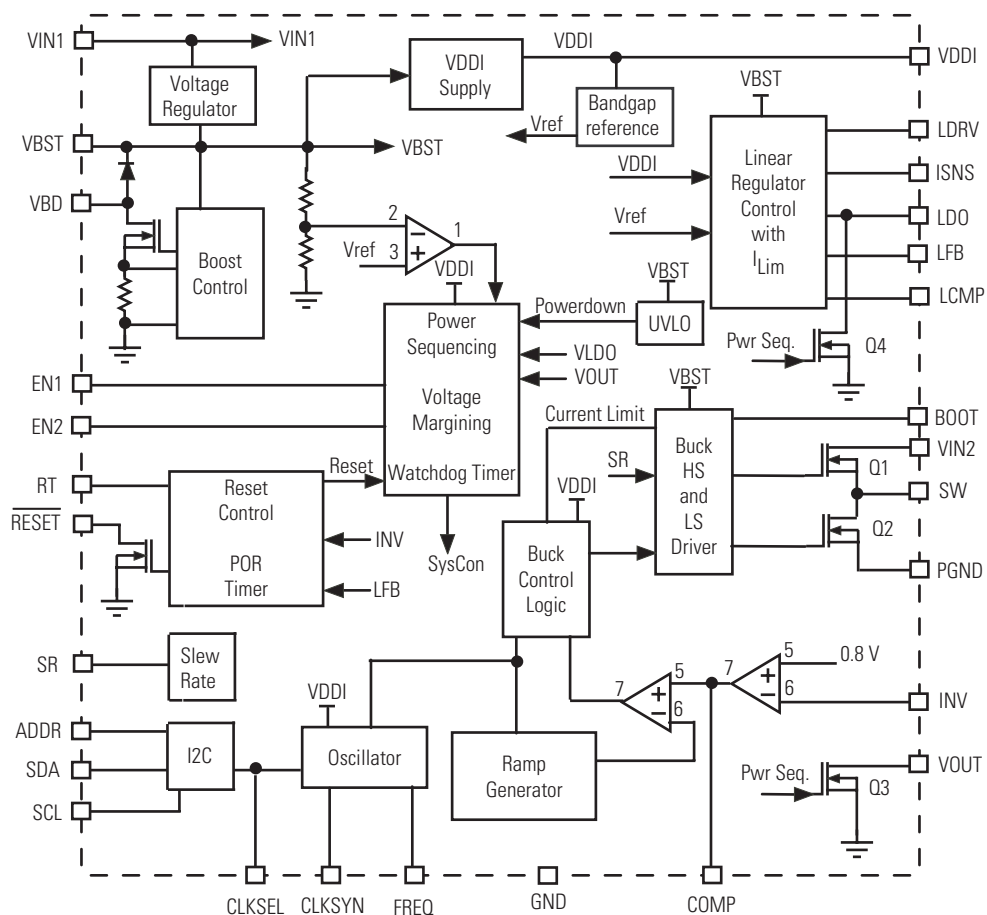


Figure 2. 34703 Simplified Internal Block Diagram

## PIN CONNECTIONS

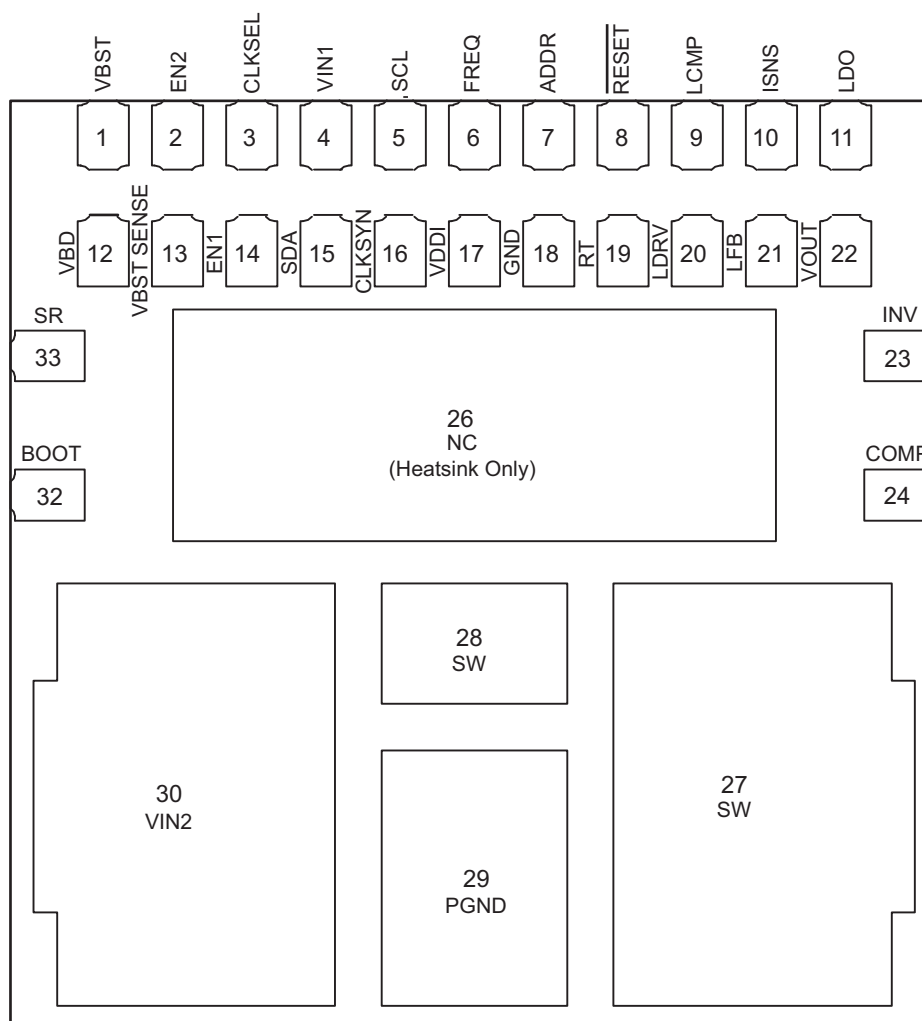


Figure 3. 34703 Pin Connections Bottom View

Table 1. 34703 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 15](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	VBST	Input	Boost Voltage	Input for internal boost regulator. The internal boost regulator provides 8 V (at up to 45 mA current) to supply the gate drive circuits for the integrated power MOSFETs and the external N-channel power MOSFET of the linear regulator.
2	EN2	Input	Enable Pin 2	Enable 2 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determine operation mode and type of power sequencing of the IC.
3	CLKSEL	Input/Output	Clock Selection	This pin sets the CLKSYN pin either as an oscillator output or synchronization input pin. The CLKSEL pin is also used for the I <sup>2</sup> C address selection.

**Table 1. 34703 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 15](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
4	VIN1	Input	Input Voltage 1	The input supply pin for the integrated circuit. The internal circuits of the IC are supplied through this pin.
5	SCL	Input	Serial Clock	I <sup>2</sup> C bus pin. Serial clock.
6	FREQ	Input	Oscillator Frequency	The switcher oscillator frequency can be adjusted by connecting an external resistor $R_F$ to the FREQ pin. The default switching frequency (FREQ pin left open or tied to $V_{DDI}$ ) is ~300 kHz.
7	ADDR	Input	Address	I <sup>2</sup> C address selection. This pin can be either left open, tied to $V_{DDI}$ , or grounded through a 10 k $\Omega$ resistor.
8	RESET	Output	Reset	The Reset pin indicates to the external circuitry when one of the regulators protection features has been activated. Note, since it is an open drain output it has to be pulled up to some supply voltage (e.g., the output of the LDO) by an external resistor.
9	LCMP	Input	Linear Compensation	Linear regulator compensation pin.
10	ISNS	Input	Current Sense	Current sense pin of the LDO to provide overcurrent protection of the linear regulator's external power MOSFET. The voltage drop over the LDO current sense resistor $R_S$ is sensed between the ISNS and the LDO pins. The LDO current limit can be adjusted by selecting the proper value of the current sense resistor $R_S$ .
11	LDO	Input	Linear Regulator	Input pin of the linear regulator power sequence and current limit control circuits.
12	VBD	Output	Boost Voltage Drain	Drain of the internal boost regulator's switching power MOSFET.
13	VBST SENSE	Input	Boost Voltage Sense	Note, this pin must be connected to VBST (pin 1) and is not intended to provide power to external circuitry.
14	EN1	Input	Enable Pin 1	Enable 1 Input. The combination of the logic state of the Enable 1 and Enable 2 inputs determine operation mode and type of power sequencing of the IC.
15	SDA	Input/Output	Serial Data	I <sup>2</sup> C bus pin. Serial data.
16	CLKSYN	Input/Output	Clock Sync Input/ Oscillator Output	Oscillator synchronization input pin or oscillator output pin. The CLKSYN pin can be configured either as an oscillator output when the CLKSEL pin is left open or it can be used as a synchronization input when the CLKSEL pin is grounded.
17	VDDI	Passive	Vdd Filter	Internal supply voltage capacitor pin. A ceramic low ESR 1.0 $\mu$ F capacitor in parallel with a ceramic 100nF capacitor should be connected from this pin to ground. The VDDI power supply voltage is for internal use only; do not use externally.
18	GND	Signal	Ground	Analog ground of the IC.
19	RT	Passive	Reset Timer	This pin allows programming the Power-ON Reset delay by means of an external RC network.
20	LDRV	Output	LDO Gate Drive	LDO gate drive of the external pass N-channel MOSFET.
21	LFB	Input	LDO Feedback	Linear regulator feedback pin.
22	VOOUT	Output	Output Voltage Power Sequencing Control	This pin must be directly connected to the output voltage of the buck converter. This pin controls the buck regulators output voltage (Vout) in accordance with the power sequencing control mode set by EN1 and EN2.
23	INV	Input	Error Amp	Buck Controller Error Amplifier inverting input.
24	COMP	Input	Switcher Compensation	Buck converter compensation pin.

**Table 1. 34703 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 15](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
25, 31				These pins are not present in package.
26	NC	Heatsink		No electrical connection, thermal heatsinking only.
27, 28	SW	Output	Switch	Buck regulator switching node. This pin is connected to the high power inductor.
29	PGND	Power	Power Ground	Buck regulator and power sequencing shunt FETs Power Ground.
30	VIN2	Input	Input Voltage 2	Buck regulator power input. Drain of the high-side power MOSFET.
32	BOOT	Input	Bootstrap	Bootstrap capacitor input.
33	SR	Passive	Slew Rate	Buck converter Slew Rate control pin.

## ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
<b>ELECTRICAL RATINGS</b>			
Supply Voltage	$V_{IN1}, V_{IN2}$	-0.3 to 14	V
Switching Node	SW	-1.0 to 14	V
Buck Regulator Bootstrap Input (BOOT - SW)	BOOT	-0.3 to 8.5	V
Differential Voltage (SR - SW)	$V_{SR}$	-0.3 to 8.5	V
Boost Regulator Output <sup>(1)</sup>	$V_{BST}$	-0.3 to 8.5	V
Boost Regulator Drain	$V_{BD}$	-0.3 to 9.5	V
$\overline{\text{RESET}}$ Drain Voltage	$\overline{\text{RESET}}$	-0.3 to 7.0	V
Enable Pins (EN1, EN2)	$V_{\text{ENABLE}}$	-0.3 to 14	V
Logic Pins (SDA, SCL, CLKSYN)	$V_{\text{LOGIC}}$	-0.3 to 7.0	V
Analog Pins (INV, $V_{\text{OUT}}$ )	$V_{\text{ANALOG1}}$	-0.3 to 7.0	V
Analog Pins (LDRV, LFB, LDO, LCMP, ISNS)	$V_{\text{ANALOG2}}$	-0.3 to 8.5	V
Analog Pins (CLKSEL, ADDR, RT, FREQ, $V_{\text{DDI}}$ )	$V_{\text{ANALOG3}}$	-0.3 to 3.6	V
ESD Voltage			V
Human Body Model <sup>(2)</sup>	$V_{\text{ESD1}}$	±2000	
Machine Model <sup>(3)</sup>	$V_{\text{ESD2}}$	±200	
<b>THERMAL RATINGS</b>			
Storage Temperature	$T_{\text{STG}}$	-65 to 150	°C
Power Dissipation ( $T_A = 85^\circ\text{C}$ ) <sup>(4)</sup>	$P_D$	2.0	W
Lead Soldering Temperature <sup>(5)</sup>	$T_{\text{SOLDER}}$	245	°C
Maximum Operating Junction Temperature	$T_{\text{JMAX}}$	125	°C
Package Operating Temperature Range (Ambient Temperature)	$T_A$	-40 to 85	°C
<b>THERMAL RESISTANCE</b>			
Thermal Resistance, Junction to Ambient <sup>(6)</sup>	$R_{\theta\text{JA}}$	38	°C/W
Thermal Resistance, Junction to Base <sup>(7)</sup>	$R_{\theta\text{JB}}$	~1.0	°C/W

## Notes

- Maximum recommended filter capacitor: 10  $\mu\text{F}$ . (Note, VBST pin is not short-circuit protected.)
- ESD1 testing is performed in accordance with the Human Body Model ( $C_{\text{ZAP}}=100\text{ pF}$ ,  $R_{\text{ZAP}}=1500\ \Omega$ ).
- ESD2 testing is performed in accordance with the Machine Model ( $C_{\text{ZAP}}=200\text{ pF}$ ,  $R_{\text{ZAP}}=0\ \Omega$ ).
- Maximum still-air power dissipation at indicated ambient temperature; higher power dissipations may be possible with additional heat-sinking and forced-air cooling.
- Lead soldering temperature limit is for 10 seconds maximum duration. Contact Freescale Sales Office for immersion soldering time/temperature limits.
- Thermal resistance measured in accordance with EIA/JESD51-2.
- Theoretical thermal resistance from the die junction to the exposed heat-sinking pins.

## STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $2.8\text{ V} \leq V_{\text{IN}} \leq 13.5\text{ V}$ . Typical values noted reflect the approximate parameter means at  $T_A = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>GENERAL (VIN1, VIN2, VBST, VDDI) <sup>(9)</sup></b>					
Operating Voltage Range (VIN1, VIN2)	$V_{\text{IN}}$	2.8	–	13.5	V
Start-Up Voltage Threshold (Boost Switching)	$V_{\text{ST}}$	–	1.6	1.8	V
$V_{\text{BST}}$ Undervoltage Lockout (Internal use only)	$V_{\text{BSTUVLO}}$	5.5	6.0	6.5	V
Input DC Supply Current (Normal Operation Mode, Enabled) <sup>(8)</sup>	$I_{\text{IN}}$	–	60	–	mA
$V_{\text{IN1}}$ Pin Input Supply Current ( $\text{EN1} = \text{EN2} = 0$ ) <sup>(8)</sup>	$I_{\text{IN1}}$	–	13	–	mA
$V_{\text{IN2}}$ Pin Input Leakage Current ( $\text{EN1} = \text{EN2} = 0$ ) <sup>(8)</sup>	$I_{\text{IN2}}$	–	100	–	$\mu\text{A}$
Output Voltage <sup>(11)</sup>	$V_{\text{OUT}}$	10% $V_{\text{IN}}$	–	5.0	V
Output DC Current <sup>(10) (11)</sup>	$I_{\text{OUT}}$	0.1	–	12	A
<b>BUCK CONVERTER (INV, VOUT)</b>					
Buck Converter Feedback Voltage $I_{\text{VOUT}} = 100\text{ mA}$ to $10\text{ A}$ , $V_{\text{IN1}} = V_{\text{IN2}} = 2.8\text{ V}$ to $13.5\text{ V}$ . No $R_{\text{B}}$ Resistor. Includes Load Regulation Error	$V_{\text{INV}}$	0.784	0.8	0.816	V
Buck Converter Voltage Margining Step	$V_{\text{MVO}}$	–	1.0	–	%
Buck Converter Line Regulation <sup>(12)</sup> $V_{\text{IN1}} = V_{\text{IN2}} = 2.8\text{ V}$ to $13.5\text{ V}$ , $I_{\text{VOUT}} = 10\text{ A}$	$\text{REG}_{\text{LNVO}}$	-1.0	–	1.0	%
Buck Converter Load Regulation <sup>(12)</sup> $I_{\text{VOUT}} = 100\text{ mA}$ to $10\text{ A}$	$\text{REG}_{\text{LDVO}}$	-2.0	–	2.0	%
$V_{\text{OUT}}$ Input Leakage Current $V_{\text{OUT}} = 5.0\text{ V}$	$I_{\text{VOUTLK}}$	1.7	4.6	7.5	mA
High-Side Power MOSFET Q1 $R_{\text{DS(ON)}}$ <sup>(10)</sup> $I_{\text{D}} = 1.0\text{ A}$ , $T_A = 25^{\circ}\text{C}$ , $V_{\text{BST}} = 8.0\text{ V}$	$R_{\text{DS(ON)}}$	–	–	25	$\text{m}\Omega$
Low-Side Power MOSFET Q2 $R_{\text{DS(ON)}}$ <sup>(10)</sup> $I_{\text{D}} = 1.0\text{ A}$ , $T_A = 25^{\circ}\text{C}$ , $V_{\text{BST}} = 8.0\text{ V}$	$R_{\text{DS(ON)}}$	–	–	10	$\text{m}\Omega$
Buck Converter Peak Current Limit (High Level)	$I_{\text{HLIM}}$	12	15	19	A
Buck Converter Valley Current Limit (Low Level)	$I_{\text{LLIM}}$	6.0	7.5	9.0	A
$V_{\text{OUT}}$ Internal Pull-Down MOSFET Current Limit $T_A = 25^{\circ}\text{C}$ , $V_{\text{BST}} = 8.0\text{ V}$	$I_{\text{Q3LIM}}$	0.75	1.7	2.0	A
$V_{\text{OUT}}$ Internal Pull-Down MOSFET $R_{\text{DS(ON)}}$ $I_{\text{D}} = 1.0\text{ A}$ , $T_A = 25^{\circ}\text{C}$ , $V_{\text{BST}} = 8.0\text{ V}$	$\text{Q3R}_{\text{DS(ON)}}$	–	–	3.0	$\Omega$
Thermal Shutdown <sup>(12)</sup>	$T_{\text{SD}}$	150	170	190	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis <sup>(12)</sup>	$T_{\text{SDHys}}$	–	15	–	$^{\circ}\text{C}$

## Notes

8. Not production tested; typical values for reference only.
9.  $V_{\text{DDI}}$  is an internal supply voltage. It should not be used for any external purpose.
10. Design information only; not production tested.
11. Minimum output voltage can be adjusted to  $0.8\text{ V}$  when  $V_{\text{IN}} < 8\text{ V}$ . Maximum currents subject to sufficient heat-sinking.
12. Guaranteed by design.

**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $2.8\text{ V} \leq V_{\text{IN}} \leq 13.5\text{ V}$ . Typical values noted reflect the approximate parameter means at  $T_A = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>BUCK ERROR AMPLIFIER (INV, COMP)</b>					
Input Impedance <sup>(13)</sup>	$R_{\text{IN}}$	–	14	–	$\text{M}\Omega$
Output Impedance <sup>(13)</sup>	$R_{\text{OUT}}$	–	1.4	–	$\text{k}\Omega$
DC Open Loop Gain <sup>(13)</sup>	$A_{\text{VOL}}$	–	80	–	dB
Gain Bandwidth Product <sup>(13)</sup>	GBW	–	4.0	–	MHz
Slew Rate <sup>(13)</sup>	SR	–	2.0	–	$\text{V}/\mu\text{s}$
Output Voltage Swing – High Level $V_{\text{IN1}} \geq 3.3\text{ V}$ , $I_{\text{OEA}} = -400\text{ mA}$ <sup>(13)</sup>	$V_{\text{EAOH}}$	–	2.0	–	V
Output Voltage Swing – Low Level $I_{\text{OEA}} = 400\text{ mA}$ <sup>(13)</sup>	$V_{\text{EAOL}}$	–	0.4	–	V
Slope Compensation Ramp <sup>(13)</sup>	$V_{\text{SCRAMP}}$	–	0.6	–	V
<b>OSCILLATOR (FREQ)</b>					
Oscillator Low-Level Output Voltage (CLKSYN Pin), CLKSEL Open	$V_{\text{OSCOL}}$	–	0.1	0.4	V
Oscillator High-Level Output Voltage (CLKSYN Pin), CLKSEL Open <sup>(14)</sup>	$V_{\text{OSCOH}}$	2.7	–	3.3	V
Oscillator Input Voltage Threshold (CLKSYN Pin), CLKSEL Grounded	$V_{\text{OSCIH}}$	1.2	1.6	2.0	V
Oscillator Frequency Adjusting Reference Voltage (FREQ) <sup>(16)</sup>	$V_{\text{FREQ}}$	1.15	1.27	1.35	V
Oscillator Frequency Adjusting Resistor Range <sup>(16)</sup>	$R_{\text{FREQ}}$	5.0	–	20	$\text{k}\Omega$
<b>BOOST REGULATOR (VBST, VIN)</b>					
Boost Regulator Output Voltage $I_{\text{BST}} = 20\text{ mA}$ , $V_{\text{IN1}} = V_{\text{IN2}} = 2.8\text{ V}$ to $8.0\text{ V}$	$V_{\text{BST}}$	7.5	8.0	8.5	V
Boost Regulator Output Voltage <sup>(15)</sup> $I_{\text{BST}} = 20\text{ mA}$ , $V_{\text{IN1}} = V_{\text{IN2}} > 8.0\text{ V}$	$V_{\text{BST(VGREG)}}$	7.5	8.0	8.8	V
Boost Regulator Start-Up Voltage	$V_{\text{INBSU}}$	–	1.6	1.8	V
Boost Regulator Peak Current Limit (Power FET Peak Current)	$I_{\text{PBD}}$	0.75	1.0	1.5	A
Boost Regulator Power FET Valley Current Limit (Low Level)	$I_{\text{LBD}}$	550	600	900	mA
Boost Power FET $R_{\text{DS(ON)}}$ <sup>(16)</sup> $I_{\text{BST}} = 500\text{ mA}$ , $V_{\text{IN1}} = V_{\text{IN2}} = 13.5\text{ V}$	$R_{\text{DS(ON)}}$	–	900	–	$\text{m}\Omega$
Boost Regulator Recommended Output Capacitor	$C_{\text{BST}}$	–	10	–	$\mu\text{F}$
Boost Regulator Recommended Output Capacitor Maximum ESR	$\text{ESR}_{\text{CBST}}$	–	–	100	$\text{m}\Omega$

Notes

13. Design information only. It is not production tested.
14. All internal high level voltages are reference to the VDDI voltage.
15. When the input is above 8 V an integrated linear regulator will provide  $V_{\text{BST}}$ ; under this configuration the external inductor must be removed and the VBD pin left open (floating).
16. Guaranteed by design.



**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $2.8\text{ V} \leq V_{\text{IN}} \leq 13.5\text{ V}$ . Typical values noted reflect the approximate parameter means at  $T_A = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>LINEAR REGULATOR (LDO, ISNS, LDRV, LFB) <sup>(17)</sup></b>					
LDO Output Voltage Range <sup>(17)</sup> $V_{\text{IN}1} = V_{\text{IN}2} = 2.8\text{ V to } 13.5\text{ V}$ , $I_{\text{LDO}} = 100\text{ mA to } 2000\text{ mA}$	$V_{\text{LDO}}$	0.8	–	4.5	V
LDO Feedback Voltage, LFB Pin Connected to LDO Pin $V_{\text{IN}1} = V_{\text{IN}2} = 2.8\text{ V to } 13.5\text{ V}$ , $I_{\text{LDO}} = 100\text{ mA to } 2000\text{ mA}$ . Includes Load Regulation Error	$V_{\text{LDO}}$	0.784	0.8	0.816	V
LDO Voltage Margining Step Size	$V_{\text{MLDO}}$	–	1.0	–	%
LDO Line Regulation $V_{\text{IN}1} = V_{\text{IN}2} = 2.8\text{ V to } 13.5\text{ V}$ , $I_{\text{LDO}} = 1000\text{ mA}$	$\text{REG}_{\text{LNVLDO}}$	-1.0	–	1.0	%
LDO Load Regulation $I_{\text{LDO}} = 100\text{ mA to } 2000\text{ mA}$	$\text{REG}_{\text{LDVLDO}}$	-1.0	–	1.0	%
LDO Ripple Rejection, Dropout Voltage $V_{\text{DO}} = 1.0\text{ V}$ , $V_{\text{RIPPLE}} = +1.0\text{ V p-p}$ <sup>(18)</sup> Sinusoidal, $f = 300\text{ kHz}$ , $I_{\text{LDO}} = 500\text{ mA}$	$V_{\text{LDORR}}$	–	26	–	dB
LDO Maximum Dropout Voltage ( $V_{\text{IN}} - V_{\text{LDO}}$ ) <sup>(18)</sup> $V_{\text{LDO}} = 2.5\text{ V}$ , $I_{\text{LDO}} = 2000\text{ mA}$	$V_{\text{DO}}$	–	50	–	mV
LDO Current Sense Comparator Threshold Voltage ( $V_{\text{CS}} - V_{\text{LDO}}$ )	$V_{\text{CSTH}}$	35	45	65	mV
LDO Pin Input Current	$I_{\text{LDO}}$	1.0	2.0	4.0	mA
LDO Feedback Input Current (LFB Pin)	$I_{\text{LFB}}$	-1.0	0.04	1.0	$\mu\text{A}$
LDO Drive Output Current (LDRV Pin)	$I_{\text{LDRV}}$	2.0	4.0	5.0	mA
LDO Drive Current Limit (LDRV Pin) <sup>(18)</sup>	$I_{\text{DRLIM}}$	–	3.6	–	mA
ISNS Pin Input Leakage Current $V_{\text{ISNS}} = 5.0\text{ V}$	$I_{\text{SNSLK}}$	50	125.0	200	$\mu\text{A}$
LDO Error Amplifier Input Impedance (LFB Pin) <sup>(18)</sup>	$R_{\text{IN}}$	–	10	–	$\text{M}\Omega$
LDO Error Amplifier Output Impedance (LCMP Pin) <sup>(18)</sup>	$R_{\text{OUT}}$	–	60	–	$\Omega$
LDO Internal Pull-Down MOSFET Current Limit $T_A = 25^{\circ}\text{C}$ , $V_{\text{BST}} = 8.0\text{ V}$ (LDO Pin)	$I_{\text{Q4LIM}}$	0.75	1.7	2.0	A
LDO Internal Pull-Down MOSFET $R_{\text{DS(ON)}}$ $I_{\text{D}} = 1.0\text{ A}$ , $T_A = 25^{\circ}\text{C}$ , $V_{\text{BST}} = 8.0\text{ V}$	$\text{Q4R}_{\text{DS(ON)}}$	–	–	3.2	$\Omega$
LDO Recommended Output Capacitance	$C_{\text{LDO}}$	–	10	–	$\mu\text{F}$
LDO Recommended Output Capacitor ESR	$\text{ESR}_{\text{CLDO}}$	–	100	–	$\text{m}\Omega$
Thermal Shutdown (LDO Pull-Down FET Q4) <sup>(19)</sup>	$T_{\text{SD}}$	150	170	190	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis <sup>(19)</sup>	$T_{\text{SDHYS}}$	–	15	–	$^{\circ}\text{C}$
Soft Start Duration (Power Sequencing Disabled, $\text{EN}1 = 1$ , $\text{EN}2 = 1$ ) <sup>(18)</sup>	$t_{\text{SS}}$	–	800	–	$\mu\text{s}$

**Notes**

17. The LDO output range is given for the MOSFET as depicted on [Figure 33](#). Should the customer select another MOSFET, it is the customer's responsibility to properly select the MOSFET given the expected power dissipation, voltage drop across it and any other constraint that could impact the MOSFET reliability and range of work.
18. Not production tested for typical values specified.
19. Guaranteed by design.

**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$  unless otherwise noted. Input voltages  $2.8\text{ V} \leq V_{\text{IN}} \leq 13.5\text{ V}$ . Typical values noted reflect the approximate parameter means at  $T_A = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>CONTROL AND SUPERVISORY CIRCUITS (EN1, EN2, RESET, CLKSEL, ADDR, RT)</b>					
Enable (EN1, EN2) Input Voltage Threshold	$V_{\text{THEN}}$	1.2	1.6	2.0	V
Enable (EN1, EN2) Input Voltage Threshold Hysteresis <sup>(21)</sup>	$V_{\text{IHYS}}$	–	0.1	–	V
Enable (EN1, EN2) Pull-Down Resistance	$R_{\text{PU}}$	30	60	90	k $\Omega$
RESET Low-Level Output Voltage, $I_{\text{OL}} = 5.0\text{ mA}$	$V_{\text{OL}}$	–	0.1	0.4	V
RESET Leakage Current, OFF State, Pulled Up to 5.0 V	$I_{\text{LKGRST}}$	–	–	10	$\mu\text{A}$
RESET Undervoltage Threshold on $V_{\text{OUT}}$ ( $\Delta V_{\text{OUT}}/V_{\text{OUT}}$ ) <sup>(20)</sup>	$V_{\text{OUTITH}}$	-12	-7.5	-4.0	%
RESET Overvoltage Threshold on $V_{\text{OUT}}$ ( $\Delta V_{\text{OUT}}/V_{\text{OUT}}$ ) <sup>(20)</sup>	$V_{\text{OUTTTH}}$	4.0	7.5	12	%
RESET Undervoltage Threshold on $V_{\text{LDO}}$ ( $\Delta V_{\text{LDO}}/V_{\text{LDO}}$ ) <sup>(20)</sup>	$V_{\text{LDOITH}}$	-12	-7.5	-4.0	%
RESET Overvoltage Threshold on $V_{\text{LDO}}$ ( $\Delta V_{\text{LDO}}/V_{\text{LDO}}$ ) <sup>(20)</sup>	$V_{\text{LDOTTH}}$	4.0	7.5	12	%
RT Voltage Threshold	$V_{\text{THRT}}$	0.8	1.2	1.5	V
RT current source	$I_{\text{SRT}}$	17	25	34	mA
RT Saturation Voltage, Reset Timer Current = 300 $\mu\text{A}$	$V_{\text{SATRT}}$	–	45	100	mV
Maximum Value of the RT Capacitor	$C_{\text{T}}$	–	–	33	$\mu\text{F}$
CLKSEL Threshold Voltage	$V_{\text{THCLKS}}$	1.2	1.6	2.0	V
CLKSEL Pull-Up Resistance	$R_{\text{PUCLKS}}$	60	120	240	k $\Omega$
ADDR Threshold Voltage	$V_{\text{THADDR}}$	1.2	1.6	2.0	V
ADDR Pull-Up Resistance	$R_{\text{PUADDR}}$	60	120	240	k $\Omega$
<b>I<sup>2</sup>C Bus (SDA, SCL)</b>					
Input Threshold Voltage	$V_{\text{ITH}}$	1.3	–	1.7	V
Input Voltage Threshold Hysteresis <sup>(21)</sup>	$V_{\text{IHYS}}$	–	0.2	–	V
SDA, SCL Input Current, Input Voltage = 0.4 V to 5.5 V	$I_{\text{I}}$	–	–	10	$\mu\text{A}$
SDA Low-Level Output Voltage, 3.0 mA Sink Current	$V_{\text{OL}}$	–	–	0.4	V
SDA, SCL Capacitance	$C_{\text{I}}$	–	–	10	pF

Notes

20. This parameter does not include the tolerance of the external resistor divider.

21. Not production tested for typical values specified.

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 4. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figure 27](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>BUCK CONVERTER (SW, SR)</b>					
Duty Cycle Range (Normal Operation) <sup>(22)</sup>	D	10	–	90	%
Switching Node SW Rise Time <sup>(22)</sup> $I_{LOAD} = 10\text{ A}$ , SR = OPEN, $V_{IN1} = V_{IN2} = 3.3\text{ V}$	$t_{ROPEN}$	–	10	–	ns
Switching Node SW Fall Time <sup>(22)</sup> $I_{LOAD} = 10\text{ A}$ , SR = OPEN, $V_{IN1} = V_{IN2} = 3.3\text{ V}$	$t_{FOPEN}$	–	10	–	ns
Switching Node SW Rise Time <sup>(22)</sup> $I_{LOAD} = 10\text{ A}$ , SR = SW, $V_{IN1} = V_{IN2} = 3.3\text{ V}$	$t_{RSW}$	–	14	–	ns
Switching Node SW Fall Time <sup>(22)</sup> $I_{LOAD} = 10\text{ A}$ , SR = SW, $V_{IN1} = V_{IN2} = 3.3\text{ V}$	$t_{FSW}$	–	14	–	ns
Switching Node SW Rise Time <sup>(22)</sup> $I_{LOAD} = 10\text{ A}$ , SR = BOOT, $V_{IN1} = V_{IN2} = 3.3\text{ V}$	$t_{RBOOT}$	–	6.0	–	ns
Switching Node SW Fall Time <sup>(22)</sup> $I_{LOAD} = 10\text{ A}$ , SR = BOOT, $V_{IN1} = V_{IN2} = 3.3\text{ V}$	$t_{FBOOT}$	–	6.0	–	ns
Maximum Deadtime <sup>(22)</sup>	$t_D$	–	150	–	ns
Buck Control Loop Propagation Delay <sup>(22)</sup> $V_{INV} < 0.8\text{ V}$ to $V_{SW} > 90\%$ of High Level or $V_{INV} > 0.8\text{ V}$ to $V_{SW} < 10\%$ of Low Level	$t_{PD}$	–	50	–	ns
Soft Start Duration (Power Sequencing Disabled, EN1 = 1, EN2 = 1) <sup>(22)</sup>	$t_{SS}$		800		$\mu\text{s}$
Fault Condition Timeout <sup>(22)</sup>	$t_{FAULT}$	–	10	–	ms
Retry Timer Cycle <sup>(22)</sup>	$t_{RET}$	–	100	–	ms
<b>OSCILLATOR (FREQ)</b>					
Oscillator Default Frequency (Switching Frequency), FREQ Pin Open	$f_{OSC}$	250	300	350	kHz
Oscillator Frequency Range	$f_{OSC}$	200		400	kHz
Oscillator Output Signal Duty Cycle (Square Wave, 180° Out-of-Phase with the Internal Suitable Oscillator) <sup>(23)</sup>	$D_{OSC}$	–	50	–	%
Synchronization Pulse Minimum Duration <sup>(22)</sup>	$t_{SYNC}$	300	–	–	ns
<b>BOOST REGULATOR (VBST, VBST (sense), VBD)</b>					
Boost Regulator FET Maximum ON Time <sup>(23)</sup>	$t_{ON}$	–	24	–	$\mu\text{s}$
Boost Regulator Control Loop Propagation Delay <sup>(22)</sup>	$t_{BSTPD}$	–	50	–	ns
Boost Switching Node V <sub>BD</sub> Rise Time <sup>(22)</sup> $I_{BST} = 45\text{ mA}$	$t_{BR}$	–	35	–	ns
Boost Switching Node V <sub>BD</sub> Fall Time <sup>(22)</sup> $I_{BST} = 45\text{ mA}$	$t_{BF}$	–	5.0	–	ns

## Notes

22. Design Information only. Not production tested.  
23. Not production tested for typical values specified.

**Table 4. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  unless otherwise noted. Input voltages  $V_{IN1} = V_{IN2} = 3.3\text{ V}$  using the typical application circuit (see [Figure 27](#)) unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>LINEAR REGULATOR (LDO)</b>					
Output Current Slew Rate <sup>(24)</sup>	$I_{SR}$	–	2.5	–	A/ $\mu\text{s}$
Fault Condition Timeout <sup>(24)</sup>	$t_{FAULT}$	–	10	–	ms
Retry Timer Cycle <sup>(24)</sup>	$t_{RET}$	–	100	–	ms
<b>PIN, I<sup>2</sup>C BUS (SDA, SCL)</b>					
SCL Clock Frequency <sup>(25)</sup>	$f_{SCL}$	–	–	100	kHz
Bus Free Time Between a STOP and a START Condition <sup>(25)</sup>	$t_{BUF}$	4.7	–	–	$\mu\text{s}$
Hold Time (Repeated) START Condition (After this period, the first clock pulse is generated.) <sup>(25)</sup>	$t_{HDSTA}$	4.0	–	–	$\mu\text{s}$
Low Period of the SCL Clock <sup>(25)</sup>	$t_{LOW}$	4.7	–	–	$\mu\text{s}$
High Period of the SCL Clock <sup>(25)</sup>	$t_{HIGH}$	4.0	–	–	$\mu\text{s}$
SDA Fall Time from $V_{IH\_MAX}$ to $V_{IL\_MIN}$ , Bus Capacitance 10 pF to 400 pF, 3.0 mA Sink Current <sup>(25)</sup>	$t_F$	–	–	250	ns
Setup Time for a Repeated START Condition <sup>(25)</sup>	$t_{SUSTA}$	4.7	–	–	$\mu\text{s}$
Data Hold Time for I <sup>2</sup> C bus devices <sup>(25), (26)</sup>	$t_{HDDAT}$	0.0	–	–	$\mu\text{s}$
Data Setup Time <sup>(25)</sup>	$t_{SUDAT}$	250	–	–	ns
Setup Time for STOP Condition <sup>(25)</sup>	$t_{SUSTO}$	4.0	–	–	$\mu\text{s}$
Capacitive Load for Each Bus Line <sup>(25)</sup>	$C_B$	–	–	400	pF

Notes

24. Not production tested for typical values specified.
25. Design Information only. Not production tested.
26. The device provides an internal hold time of at least 300 ns for the SDA signal (refer to the  $V_{IH\_MIN}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

## TIMING DIAGRAMS

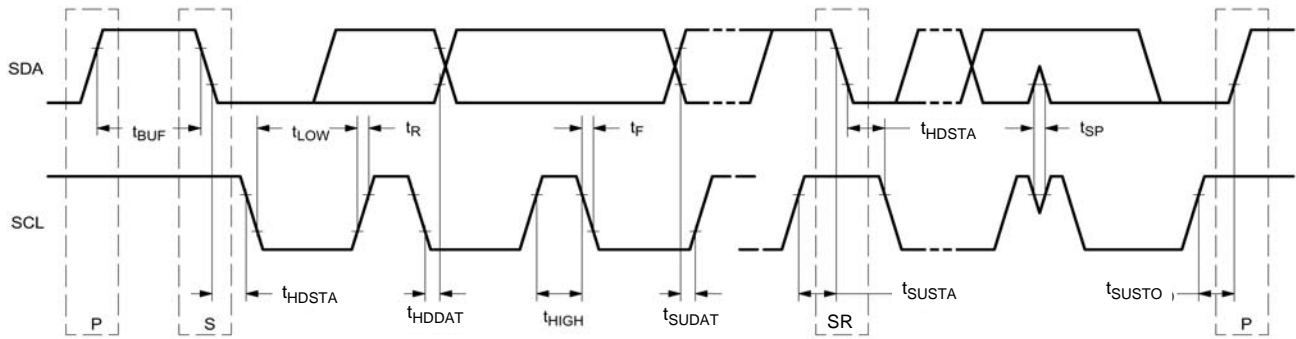


Figure 4. Definition of Time on the I<sup>2</sup>C Bus

## ELECTRICAL PERFORMANCE CURVES

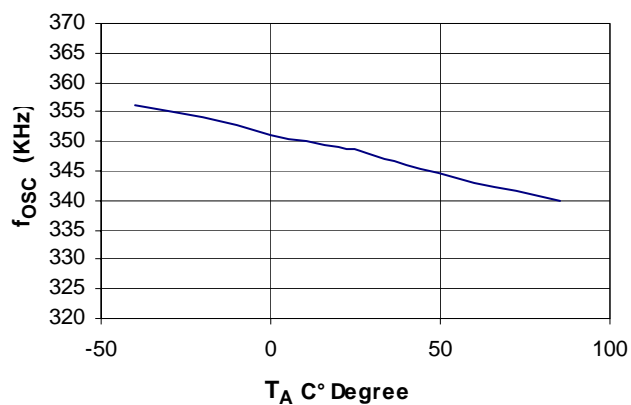


Figure 5. f<sub>OSC</sub> vs Ambient Temperature

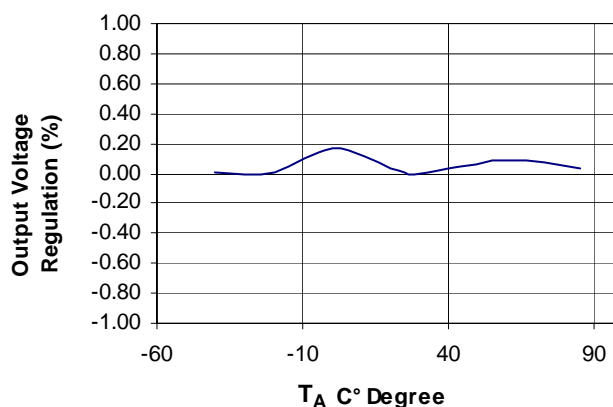


Figure 8. Buck Converter Voltage Regulation vs Ambient Temperature

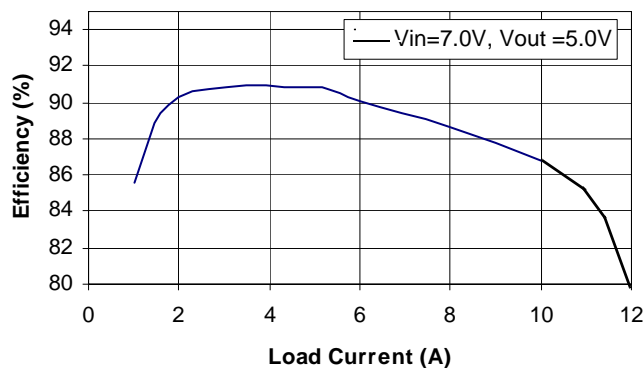


Figure 6. Efficiency vs Load Current

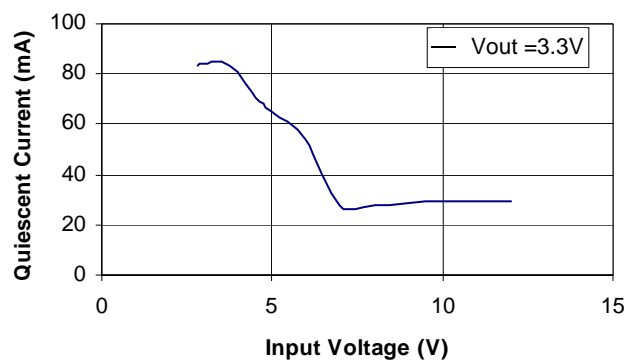


Figure 9. Quiescent Current vs Input Voltage

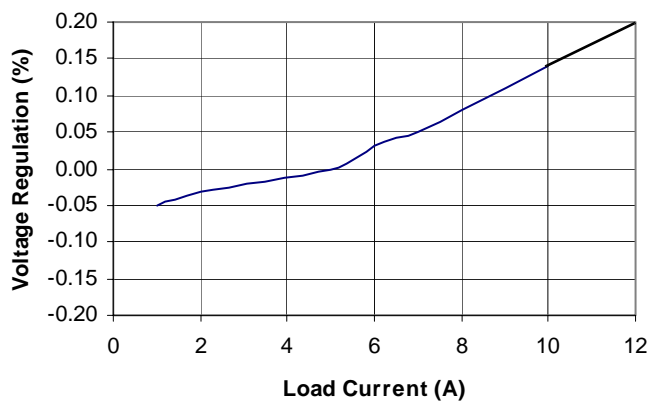


Figure 7. Buck Converter Voltage Regulation vs Load Current

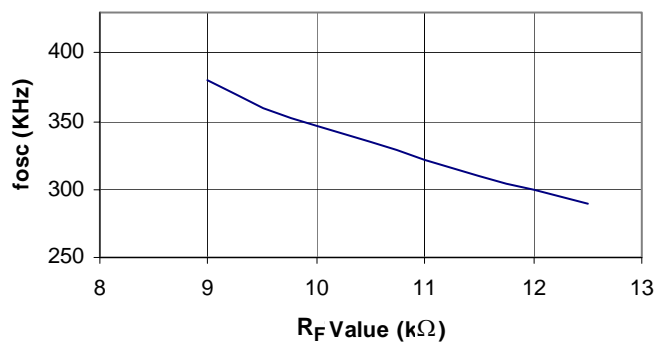


Figure 10. R<sub>F</sub> vs Frequency  
(R<sub>F</sub> is R1 in the application schematic on page [34](#))

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 34703 power supply integrated circuit is an efficient means to supply the PowerQUICC and other families of Freescale microprocessors. It incorporates a high-performance synchronous buck regulator, supplying the microprocessor's core, and a low dropout (LDO) linear regulator providing the microprocessor I/O and bus voltages.

This device incorporates many advanced features including up/down power sequencing, undervoltage lock-out, current shut-down limit, and temperature shut-down limit, to ensure proper operation and protection of the CPU and power system. The device can be configured to support different voltages and modes of operation, permitting the functions to be tailored to the specific application.

### FUNCTIONAL PIN DESCRIPTION

#### BOOST VOLTAGE PIN (VBST)

Internal boost regulator output voltage. The internal boost regulator provides a 45 mA output current to supply the drive circuits for the integrated power MOSFETs and the external N-channel power MOSFET of the linear regulator. The voltage at the VBST pin is 8.0 V nominal.

#### ENABLE 1 AND 2 PINS (EN1 AND EN2)

These two pins permit positive logic control of the Enable function and selection of the Power Sequencing mode concurrently. [Table 5](#) depicts the EN1 and EN2 function and Power Sequencing mode selection.

Both EN1 and EN2 pins have internal pulldown resistors and both can withstand a short circuit to the supply voltage, 13.5 V.

**Table 5. Operating Mode Selection**

EN1	EN2	Operating Mode
0	0	Regulators Disabled
0	1	Standard Power Sequencing
1	0	Inverted Power Sequencing
1	1	No Power Sequencing, Regulators Enabled

#### CLOCK SELECTION PIN (CLKSEL)

This pin sets the CLKSYN pin as either an oscillator output or a synchronization input pin. The CLKSEL pin is also used for the I<sup>2</sup>C address selection.

#### INPUT VOLTAGE 1 PIN (VIN1)

The input supply pin for the integrated circuit. The internal circuits of the IC are supplied through this pin.

#### SERIAL CLOCK PIN (SCL)

I<sup>2</sup>C bus pin. Serial clock.

#### OSCILLATOR FREQUENCY PIN (FREQ)

This switcher frequency selection pin can be adjusted by connecting external resistor RF to the FREQ pin. The default switching frequency (FREQ pin left open or tied to VDDI) is ~300 kHz.

#### ADDRESS PIN (ADDR)

The ADDR pin is used to set the address of the device when used in an I<sup>2</sup>C communication. This pin can either be tied to VDDI or grounded through a 10 kΩ resistor. Refer to [I<sup>2</sup>C Bus Operation on page 25](#) for more information on this pin.

#### RESET OUTPUT PIN ( $\overline{\text{RESET}}$ )

The Reset Control circuit monitors both the switching regulator and the LDO feedback voltages. It is an open drain output and has to be pulled up to the logic supply voltage (e.g., the output of the LDO) by an external resistor.

The Reset Control circuit supervises both output voltages—the linear regulator output VLDO and the switching regulator output VOUT. When either of these two regulators is out of regulation (high or low), the  $\overline{\text{RST}}$  pin is pulled low. There is a 20 μs internal delay filter preventing erroneous resets. During power-up sequencing,  $\overline{\text{RST}}$  is held low until the Reset Timer times out.

#### LINEAR COMPENSATION PIN (LCMP)

Linear regulator compensation pin.

#### CURRENT SENSE PIN (ISNS)

Current sense pin of the LDO. Overcurrent protection of the linear regulator external power MOSFET. The voltage drop over the LDO current sense resistor RS is sensed between the ISNS and LDO pins. The LDO current limit can be adjusted by selecting the proper value of the current sensing resistor RS.

## LINEAR REGULATOR PIN (LDO)

Input pin of the linear regulator power sequence control circuit.

## BOOST DRAIN PIN (VBD)

Drain of the internal boost regulator power MOSFET.

## VBST (SENSE)

Sense pin of the internal boost regulator output voltage.

## SERIAL DATA PIN (SDA)

I<sup>2</sup>C bus pin. Serial data.

## CLOCK SYNCHRONIZATION PIN (CLKSYN)

Oscillator output/synchronization input pin.

## VDD FILTER PIN (VDDI)

Internal Logic Supply Voltage Pin: a low-ESR 1.0  $\mu$ F 6.0 V capacitor must be connected between this pin and signal ground.

## RESET TIMER PIN (RT)

The Reset Timer power-up delay (RT) pin is used to set the delay between the time when the LDO and switcher outputs are active and stable and the  $\overline{\text{RST}}$  output is released. An external resistor and capacitor are used to program the timer. The power-up delay can be obtained by using the following formula:

$$t_D \sim 10 \text{ ms} + R_t C_t$$

Where  $R_t$  is the Reset Timer programming resistor and  $C_t$  is the Reset Timer programming capacitor, both connected in parallel from RT to ground.

## LINEAR DRIVE PIN (LDRV)

LDO gate drive of the external pass N-channel MOSFET.

## LINEAR FEEDBACK PIN (LFB)

Linear regulator feedback pin.

## OUTPUT VOLTAGE PIN (VOUT)

Output voltage of the buck converter. Input pin of the switching regulator power sequence control circuit.

## ERROR AMP INVERTING INPUT PIN (INV)

Buck Controller Error Amplifier inverting input.

## BUCK SWITCHER COMPENSATION (COMP)

Output voltage of the buck converter error amplifier. Compensation pin.

## SWITCH PINS (SW)

Buck regulator switching node. This pin is connected to the inductor.

## POWER GROUND PINS (PGND)

Buck regulator power ground.

## INPUT VOLTAGE 2 PINS (VIN2)

Buck regulator power input. Drain of the high-side power MOSFET.

## BOOTSTRAP PIN (BOOT)

Bootstrap capacitor input.

## SWITCHER SLEW RATE CONTROL (SR)

Buck slew rate control pin. For faster Slew Rates, connect the pin to the boot pin (Boot). For medium speeds, the pin should be left open. For slowest options, connect the pin to the Switch Pin (SW).



## FUNCTIONAL INTERNAL BLOCK DESCRIPTION

### INTRODUCTION

The paragraphs below describe the functional sub-circuits of the 34703 integrated power supply IC.

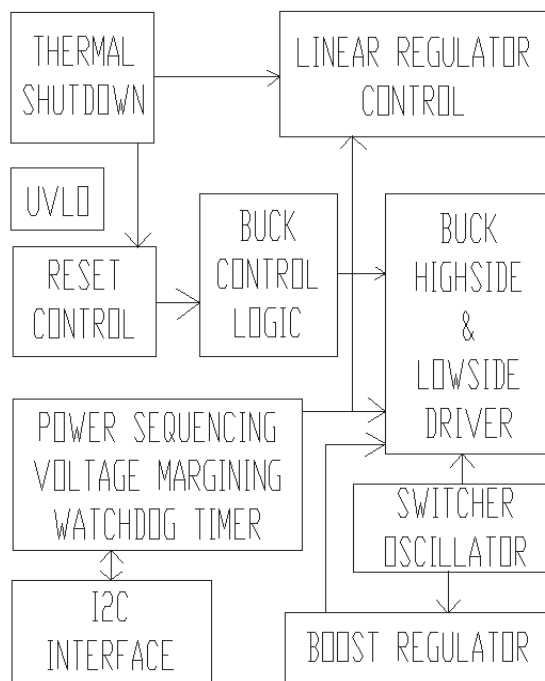


Figure 11. 34703 Functional Internal Block Diagram

### BOOST REGULATOR

A boost regulator provides a high voltage necessary to properly drive the buck regulator power MOSFETs, especially during the low input voltage condition. The LDO regulator external N-channel MOSFET gate is also powered from the boost regulator. In order to properly enhance the high-side MOSFETs when only a +3.3 V supply rail powers the integrated circuit, the boost regulator provides an output voltage of 8.0 V nominal value.

The 34703 boost regulator uses a simple hysteretic current control technique, which allows fast power-up and does not require any compensation. When the boost regulator main power switch (low side) is turned on, the current in the inductor starts to ramp up. After the inductor

current reaches the upper current limit (nominally set at 1.0 A), the low-side switch is turned off and the current charges the output capacitor through the internal rectifier. When the inductor current falls below the valley current limit value (nominally 600 mA), the low-side switch is turned on again, starting the next switching cycle. After the boost regulator output capacitor reaches its regulation limit, the low-side switch is turned off until the output voltage falls below the regulation limit again.

**NOTE:** Should the input voltage be higher than 8.0 V, an internal linear regulator provides the required boost voltage. **In this configuration the external boost inductor must be removed and the VBD pin left floating!**

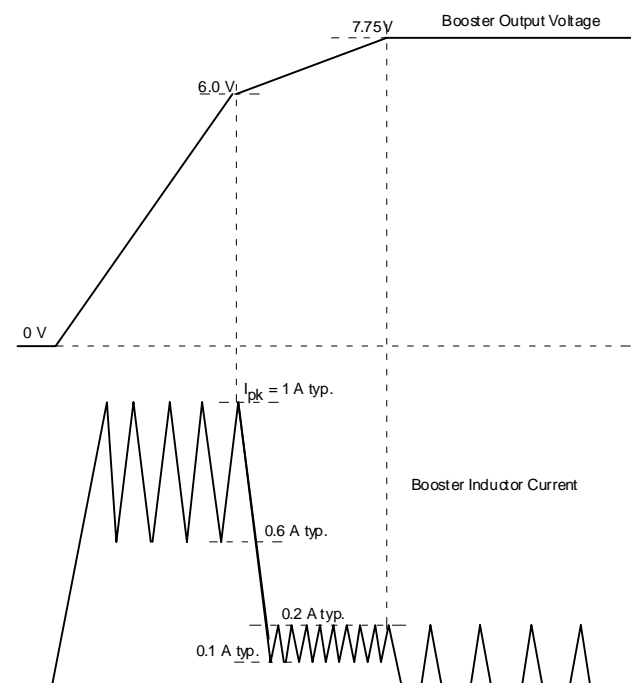


Figure 12. Boost Regulator Startup (Not To Scale)

## BUCK REGULATOR

The buck regulator is a high-frequency (300 kHz default, adjustable in the range from 200 kHz to 400 kHz), synchronous buck converter driving integrated high-side and low-side N-channel power MOSFETs. The buck regulator output voltage is adjustable by means of an external resistor divider to provide the required output voltage. Its high current output is well suited for directly powering the core of the microprocessor.

A typical bootstrap technique is used to provide the voltage necessary to properly enhance the high-side MOSFET gate. However, when the regulator is supplied from a low-input voltage (e.g., a +3.3 V supply rail), the bootstrap capacitor is charged from the internal boost regulator output  $V_{BST}$  through an external diode. This arrangement allows the 34703 to operate efficiently even from a very low input voltage source.

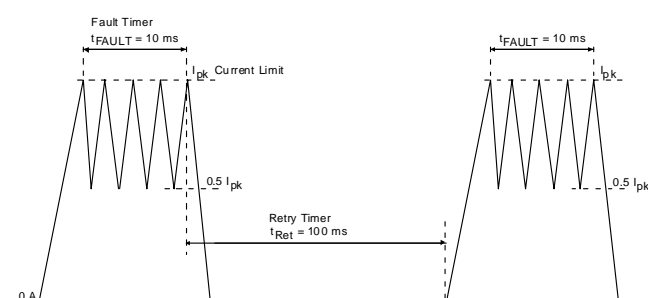


Figure 13. Switching Regulator Current Limit (Not To Scale)

In order to avoid destruction of the supplied circuits, a current limit with retry capability was implemented in the buck regulator. When an overcurrent condition occurs and the switch current reaches the peak current limit value, the main (high-side) switch is turned off until the inductor current decays to the valley value, which is one-half of the peak current limit. If an overcurrent condition exists for 10 ms, the buck regulator control circuit shuts the switcher OFF and the switcher retry timer starts to time out. When the timer expires after 100 ms, the switcher engages the start-up sequence and runs for 10 ms, repeatedly checking for the overcurrent condition. During the current limited operation (e.g., in case of short circuit on the buck regulator output), the buck regulator operation is not synchronized to the oscillator frequency.

The buck regulator output voltage can be adjusted from 0.8 V to 5.0 V. Power-up, power-down, and fault management are coordinated with the linear regulator.

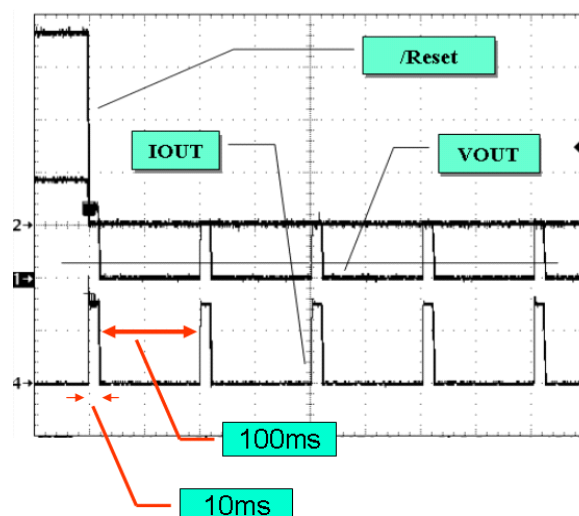


Figure 14. Buck Converter Overcurrent Protection

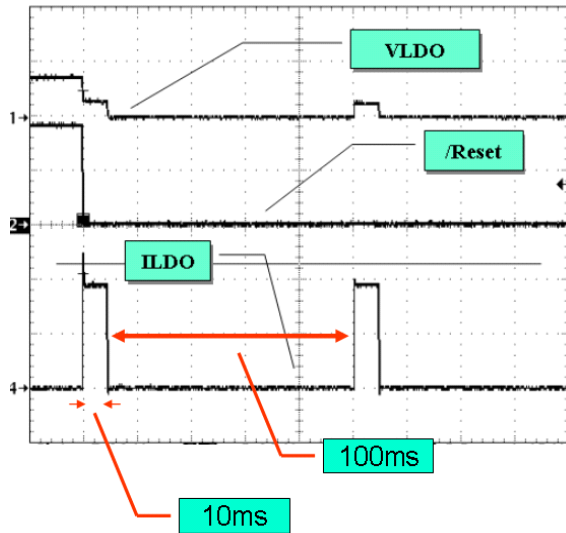


Figure 15. LDO Converter Overcurrent Protection

## SWITCHING OSCILLATOR

A 300 kHz (default) oscillator sets the switching frequency of the buck regulator. The frequency of the oscillator can be adjusted between 200 kHz and 400 kHz by an optional external resistor  $R_F$  connected from the FREQ pin of the integrated circuit to ground. See Figure 10 for frequency resistor selection.

The CLKSYN pin can be configured either as an oscillator output when the CLKSEL pin is left open or it can be used as a synchronization input when the CLKSEL pin is grounded. The oscillator output signal is a square wave logic signal with 50 percent duty cycle, 180 degrees out-of-phase with the internal clock signal. This allows opposite phase synchronization of two 3370x devices.

When the CLKSYN pin is used as synchronization input (CLKSEL pin grounded), the external resistor  $R_F$  chosen from the chart in Figure 10 should be used to synchronize the internal ramp generator to the external clock. Operation is only recommended between 200 kHz and 400 kHz. The supplied synchronization signal does not need to be 50 percent duty cycle. Minimum pulse width is 300 ns.

## LOW DROPOUT LINEAR REGULATOR (LDO)

The adjustable low dropout linear regulator (LDO) is capable of supplying up to a 2.0 A output current. It has a current limit feature with retry capability.

Current limiting is implemented via a sense resistor that feeds back a small voltage to the ISNS pin. When the sense resistor is used, the control circuit limits the current for 10 ms when the voltage measured across the current sense resistor reaches a 45 mV threshold. If the overcurrent condition still exists after the 10ms time period, the linear regulator is turned off. At the same time the overcurrent condition is detected, the Retry Timer starts to count down. When the

timer expires after 100 ms, the LDO tries to power up again for 10 ms, repeatedly checking for the overcurrent condition.

The current limit of the LDO is determined by the following formula:

$$I_{LIM} = 45 \text{ mV}/R_S$$

Where  $R_S$  is the LDO current sense resistor, connected between the ISNS pin and the LDO pin output (see Figure 27).

The output voltage of the LDO can be adjusted by means of an external resistor divider connected to the feedback control pin LFB. The linear regulator output voltage can be adjusted in the range of 0.8 V to 5.0 V, but the LDO output voltage is always lower than the input voltage to the regulator. Power-up, power-down, and fault management are coordinated with the switching regulator.

## THERMAL SHUTDOWN

In order to increase the overall safety of the system designed with the 34703, an internal thermal shutdown function has been incorporated into the switching regulator circuit. The 34703 senses the temperature of the buck regulator main switching FET (high-side FET Q1; see Figure 2), the low-side (synchronous FET Q2), and control circuit. If the temperature of any of the monitored components exceeds the limit of safe operation (thermal shutdown), the switching regulator will be shut down. After the temperature falls below the value given by the thermal shutdown hysteresis window, the switcher will retry to operate again.

The  $V_{OUT}/LDO$  pull-down FETs Q3/Q4 have an independent thermal shutdown control. When the Q3/Q4 temperature exceeds the thermal shutdown limit, Q3/Q4 will be turned off without affecting the switcher operation.

The maximum junction temperature is 125°C and thermal shutdown is 170°C. It is not recommended to operate this IC beyond these thresholds.

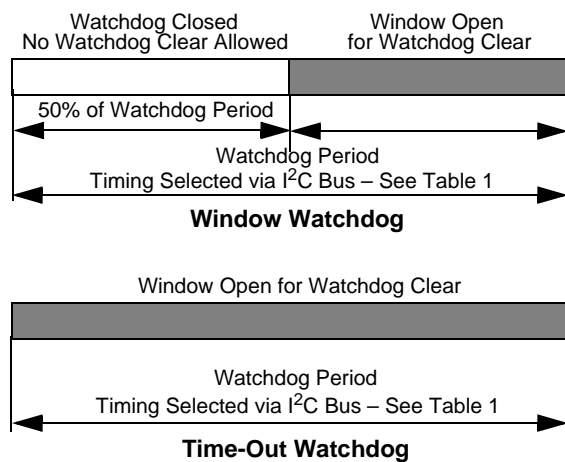
## WATCHDOG TIMER

A watchdog function is available via I<sup>2</sup>C bus communication. It is possible to select either window watchdog or time-out watchdog operation, as illustrated in Figure 16.

Watchdog time-out starts when the watchdog function is activated via I<sup>2</sup>C bus sending a Watchdog Programming command byte, thus determining watchdog operation (window or time-out) and period duration (refer to Table 6). If the watchdog is cleared by receiving a new Watchdog Programming command through the I<sup>2</sup>C bus, the watchdog timer is reset and the new time-out period begins. If the watchdog time expires, the RESET will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms. After a watchdog time-out, the function is no longer active.

When the Window Watchdog function is selected, the timer cannot be cleared during the Closed Window time, which is 50% of the total watchdog period. When the watchdog is cleared, the timer is reset and starts a new time-

out period. If the watchdog is not cleared during the Open Window time, the  $\overline{\text{RESET}}$  will become active (LOW) for a time determined by the RC components of the RT timer plus 10 ms.



**Figure 16. Watchdog Operation**

**Table 6. Watchdog Programming Command Byte  
(as a 2nd Command Byte)**

Address			Value					Action
0	1	1	0	0	0	0	0	1st Command
0	1	1	0	0	0	0	0	WD OFF <sup>(27)</sup>
0	1	1	0	1	0	0	0	WD 1280 ms WinOFF
0	1	1	0	1	0	0	1	WD 320 ms WinOFF
0	1	1	0	1	0	1	0	WD 80 ms WinOFF
0	1	1	0	1	0	1	1	WD 20 ms WinOFF
0	1	1	0	1	1	0	0	WD 1280 ms WinON
0	1	1	0	1	1	0	1	WD 320 ms WinON
0	1	1	0	1	1	1	0	WD 80 ms WinON
0	1	1	0	1	1	1	1	WD 20 ms WinON

**Notes**

27. The Watchdog feature will be turned ON automatically after receiving any other valid command byte changing watchdog time.

## FUNCTIONAL DEVICE OPERATION

### OPERATIONAL MODES

#### SOFT START

A switching regulator and LDO soft start feature is incorporated in the 34703. The soft start is active each time the IC is enabled,  $V_{IN}$  is reapplied, or after a fault retry. Other transient events do not activate the soft start.

#### VOLTAGE MARGINING

The 34703 includes a voltage margining feature accessed through the I<sup>2</sup>C bus. Voltage margining allows for independent adjustment of the Switcher  $V_{OUT}$  voltage and the linear output  $V_{LDO}$ . Each can be adjusted up and down in 1% steps to a range of  $\pm 7\%$ . This feature allows for worst case system validation; i.e., determining the design margin. Margining details are described in the section entitled [I<sup>2</sup>C Bus Operation](#), beginning on page 25 of this datasheet.

#### POWER SEQUENCING MODES

The power sequencing of the two outputs of this power supply IC is in compliance with the **Freescale Power QUICC** and other 32-bit microprocessor requirements. When the input voltage is applied, the switcher and linear regulator outputs follow the supply rail voltage during powering up and down in the limits given by the microcontroller power sequencing specification, illustrated in [Figures 17](#) through [19](#). There are two possible power sequencing modes, Standard and Inverted, as explained below. The third mode of operation is Power Sequencing Disabled.

#### STANDARD POWER SEQUENCING

When the power supply IC operates in the Standard Power Sequencing mode, the switcher output provides the core voltage for the microprocessor. This situation and operating conditions are illustrated in [Figure 17](#) and [Figure 18](#). [Table 5](#), page 15, shows the Power Sequencing mode selection.

#### INVERTED POWER SEQUENCING

When the power supply IC is operating in the Inverted Power Sequencing mode, the linear regulator (LDO) output provides the core voltage for the microprocessor, as illustrated in [Figure 19](#). [Table 5](#), page 15, shows the Power Sequencing mode selection.

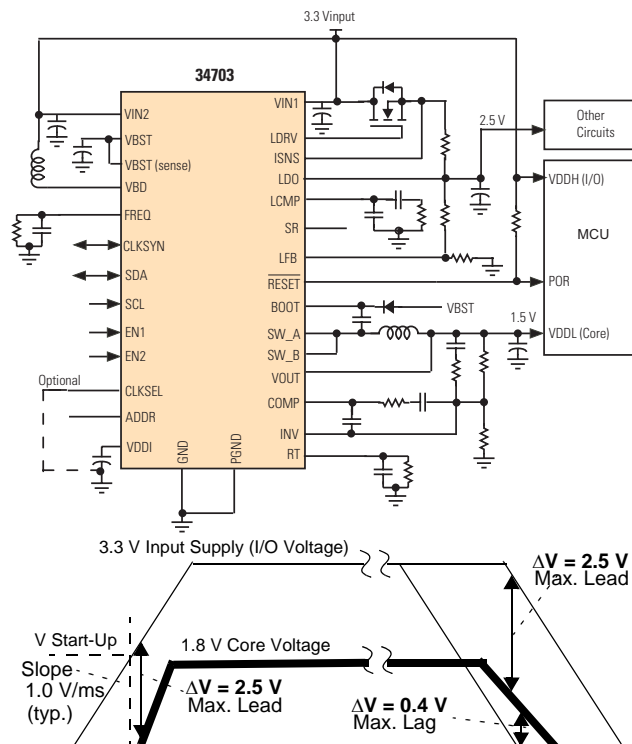


Figure 17. Standard Power Up/Down Sequence in +3.3 V Supply System

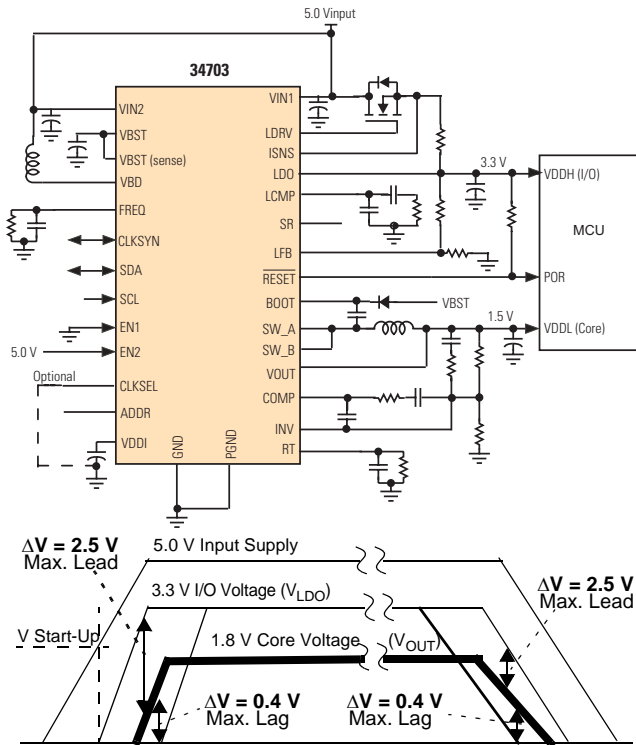


Figure 18. Standard Power Up/Down Sequence in +5.0 V Supply System

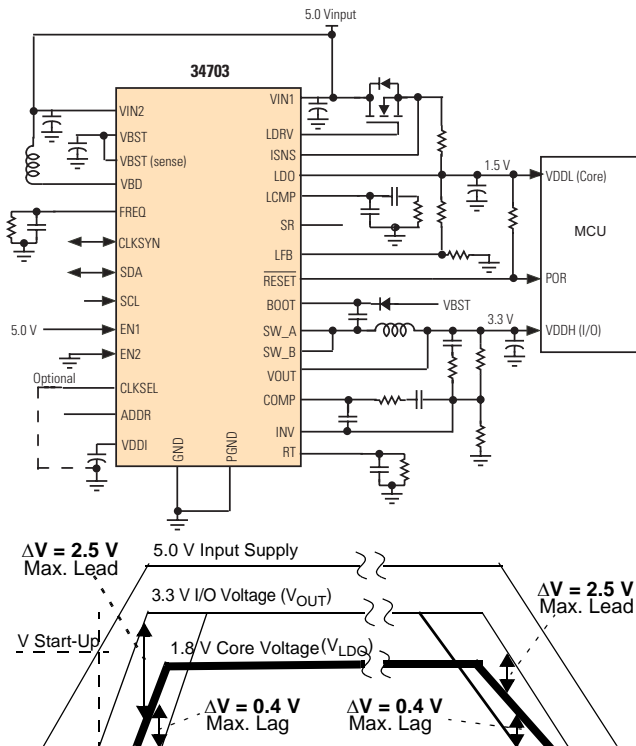


Figure 19. Inverted Power Up/Down Sequence in +5.0 V Supply System

## POWER SEQUENCING

### Requirements

1. I/O supply voltage not to exceed core voltage by more than 2.5 V.
2. Core supply voltage not to exceed I/O voltage by more than 0.4 V.

### Methods of Control

The 34703 has several methods of monitoring and controlling the regulator output voltages, as described in the paragraphs below. Power sequencing control is also achieved through the intrinsic operation of the regulators. The EN1 and EN2 pins can be used to disable the power sequencing (refer to [Table 5](#), page 15).

### Intrinsic Operation

For both the LDO and switcher, whenever the output voltage is below the regulation point, the LDO external Pass FET will be on or the Buck High-Side FET will be on at a duty cycle controlled by the switcher. Because these devices are FETs, current can flow in either direction, balancing the voltages via the common supply pin. The ability to maintain the FETs on will depend on the available gate voltage, and thus the size of the boost regulator storage capacitor.

### Standard Power Sequencing Control

Comparators monitor voltage differences between the LDO (LDO pin) and the switcher ( $V_{OUT}$  pin) outputs as follows:

1.  $LDO > V_{OUT} + 2.3 \text{ V}$ , turn off LDO. The LDO can be forced off. This occurs whenever the LDO output voltage exceeds the switcher output voltage by more than 2.3 V.
2.  $LDO > V_{OUT} + 2.4 \text{ V}$ , shunt LDO to ground. If turning off the LDO is insufficient and the LDO output voltage exceeds the switcher output voltage by more than 2.4 V, a  $1.0 \Omega$  shunt FET is turned on that discharges the LDO load capacitor to ground. The shunt FET is used for switcher output shorts to ground and for power down in case of  $V_{IN1} \neq V_{IN2}$  with the switcher output falling faster than the LDO.
3.  $LDO < V_{OUT} + 2.2 \text{ V}$ , cancel (1) and (2) above, re-enable LDO. Normal operation resumes when the LDO output voltage is less than 2.2 V above the switcher output voltage.
4.  $LDO < V_{OUT} - 0.1 \text{ V}$ , turn off switcher. The switcher can be forced off. This occurs whenever the LDO is less than  $V_{OUT} - 0.1 \text{ V}$ .
5.  $LDO < V_{OUT} - 0.3 \text{ V}$ , turn on Sync (LS) FET and  $1.0 \Omega$   $V_{OUT}$  sink FET. The Buck High-Side FET is forced off and the Sync FET is forced on. This occurs when the switcher output voltage exceeds the LDO output by more than 300 mV.



6.  $LDO > V_{OUT}$ , reset (4) and (5) above. Normal operation resumes when  $LDO > V_{OUT}$ .

### Inverted Power Sequencing Control

Comparators monitor voltage differences between the switcher ( $V_{OUT}$  pin) and LDO (LDO pin) outputs as follows:

1.  $V_{OUT} > LDO + 2.2\text{ V}$ , turn off  $V_{OUT}$ . The switcher  $V_{OUT}$  can be forced off. This occurs whenever the  $V_{OUT}$  output voltage exceeds the LDO output voltage by more than 2.3 V.
2.  $V_{OUT} > LDO + 2.4\text{ V}$ , shunt  $V_{OUT}$  to ground. If turning off the switcher  $V_{OUT}$  is insufficient and the  $V_{OUT}$  output voltage exceeds the LDO output voltage by more than 2.4 V, a  $1.0\ \Omega$  shunt FET is turned on that discharges the  $V_{OUT}$  load capacitor to ground. The shunt FET is used for LDO output shorts to ground and for power-down in case of  $V_{IN1} \neq V_{IN2}$  with LDO output falling faster than the  $V_{OUT}$ .
3.  $V_{OUT} < LDO + 2.2\text{ V}$ , cancel (1) and (2) above, re-enable  $V_{OUT}$ . Normal operation resumes when the  $V_{OUT}$  output voltage is less than 2.2 V above the LDO output voltage.
4.  $V_{OUT} < LDO - 0.2\text{ V}$ , turn off LDO. The LDO can be forced off. This occurs whenever the  $V_{OUT}$  is less than  $V_{LDO} - 0.2\text{ V}$ .
5.  $V_{OUT} < LDO - 0.3\text{ V}$ , turn on the  $1.0\ \Omega$  LDO sink FET. This occurs when the LDO output voltage exceeds the  $V_{OUT}$  output by more than 300 mV.
6.  $V_{OUT} > LDO$ , reset (4) and (5) above. Normal operation resumes when  $V_{OUT} > LDO$ .

## STANDARD OPERATING MODE

### Single 3.3 V Supply, $V_{IN} = V_{IN1} = V_{IN2} = 3.3\text{ V}$

The 3.3 V supplies the microprocessor I/O voltage, the switcher supplies core voltage (e.g., 1.8 V nominal), and the LDO operates independently (see [Figure 17](#), page 21). Power sequencing depends only on the normal switcher intrinsic operation to control the Buck High-Side FET.

#### Power Up

When  $V_{IN}$  is rising, initially  $V_{OUT}$  will be below the regulation point and the Buck High-Side FET will be on. In order not to exceed the 2.5 V differential requirement between the I/O ( $V_{IN}$ ) and the core ( $V_{OUT}$ ), the switcher must start up at 2.5 V or less and be able to maintain the 2.5 V or less differential. The maximum slew rate for  $V_{IN}$  is 1.0 V/ms.

#### Power Down

When  $V_{IN}$  is falling,  $V_{OUT}$  will be below the regulation point; therefore the Buck High-Side FET will be on. In the case

where  $V_{OUT}$  is falling faster than  $V_{IN}$ , the Buck High-Side FET will attempt to maintain  $V_{OUT}$ . In the case where  $V_{IN}$  is falling faster than  $V_{OUT}$ , the Buck High-Side FET is also on, and the  $V_{OUT}$  load capacitor will be discharged through the Buck High-Side FET to  $V_{IN}$ . Thus, provided  $V_{IN}$  does not fall too fast, the core voltage ( $V_{OUT}$ ) will not exceed the I/O voltage ( $V_{IN}$ ) by more than a maximum of 0.4 V.

#### Shorted Load

1.  $V_{OUT}$  shorted to ground. This will cause the I/O voltage to exceed the core voltage by more than 2.5 V. The load is protected by a current limit.
2.  $V_{IN}$  shorted to ground. Until the switcher load capacitance is discharged, the core voltage will exceed the I/O voltage by more than 0.4 V. By the intrinsic operation of the switcher, the load capacitor will be discharged rapidly through the Buck High-Side FET to  $V_{IN}$ .
3.  $V_{OUT}$  shorted to supply. No load protection. 34703 protected by a thermal limit.

### Single 5.0 V Supply, $V_{IN1} = V_{IN2}$ , or Dual Supply $V_{IN1} \neq V_{IN2}$

The LDO supplies the microprocessor I/O voltage. The switcher supplies the core (e.g., 1.8 V nominal) (see [Figure 18](#), page 22).

#### Power Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the  $V_{IN1}$  and  $V_{IN2}$  supplies. There are 2 cases:

1.  $LDO$  rises faster than  $V_{OUT}$ . The LDO uses control methods (1) and (2) described in the [Methods of Control](#) section, page 22.
2.  $V_{OUT}$  rises faster than  $LDO$ . The switcher uses control methods (4) and (5) described in the [Methods of Control](#) section.

#### Power Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the  $V_{IN1}$  and  $V_{IN2}$  supplies. There are 2 cases:

1.  $V_{OUT}$  falls faster than  $LDO$ . The LDO uses control methods (1) and (2) described in the [Methods of Control](#) section, page 22.

In the case  $V_{IN1} = V_{IN2}$  the intrinsic operation will turn on both the Buck High-Side FET and the LDO external Pass FET, and will discharge the LDO load capacitor into the  $V_{IN}$  supply.

2.  $LDO$  falls faster than  $V_{OUT}$ . The switcher uses control methods (4) and (5) described in the [Methods of Control](#) section.

### Shorted Load

1.  $V_{OUT}$  shorted to ground. The LDO uses method (1) and (2) described in the Methods of Control section.
2. LDO shorted to ground. The switcher uses control methods (4) and (5) described in the [Methods of Control](#) section, page 22.
3.  $V_{IN1}$  shorted to ground. This is equivalent to the LDO output shorted to ground.
4.  $V_{IN2}$  shorted to ground. This is equivalent to the switcher output shorted to ground.
5.  $V_{OUT}$  shorted to supply. No load protection. 34703 protected by current limit and thermal limit.
6. LDO shorted to supply. No load protection. 34703 protected by current limit and thermal limit.

## INVERTED OPERATING MODE

### Single 3.3 V Supply, $V_{IN} = V_{IN1} = V_{IN2} = 3.3$ V

The 3.3 V supplies the microprocessor I/O voltage, the LDO supplies core voltage (e.g., 1.8 V nominal), and the switcher  $V_{OUT}$  operates independently. Power sequencing depends only on the normal LDO intrinsic operation to control the Pass FET.

#### Power Up

When  $V_{IN}$  is rising, initially LDO will be below the regulation point and the Pass FET will be on. In order not to exceed the 2.5 V differential requirement between the I/O ( $V_{IN}$ ) and the core (LDO), the LDO must start up at 2.5 V or less and be able to maintain the 2.5 V or less differential. The maximum slew rate for  $V_{IN}$  is 1.0 V/ms.

#### Power Down

When  $V_{IN}$  is falling, LDO will be below the regulation point; therefore the Pass FET will be on. In the case where LDO is falling faster than  $V_{IN}$ , the Pass FET will attempt to maintain LDO. In the case where  $V_{IN}$  is falling faster than LDO, the Pass FET is also on, and the LDO load capacitor will be discharged through the Pass FET to  $V_{IN}$ . Thus, provided  $V_{IN}$  does not fall too fast, the core voltage (LDO) will not exceed the I/O voltage ( $V_{IN}$ ) by more than maximum of 0.4 V.

### Shorted Load

1. LDO shorted to ground. This will cause the I/O voltage to exceed the core voltage by more than 2.5 V. The load is protected by a current limit.
2.  $V_{IN}$  shorted to ground. Until the LDO load capacitance is discharged, the core voltage will exceed the I/O voltage by more than 0.4 V. By the intrinsic operation of

the LDO, the load capacitor will be discharged rapidly through the Pass FET to  $V_{IN}$ .

3. LDO shorted to supply. No load protection.

### Single 5.0 V Supply, $V_{IN1} = V_{IN2}$ , or Dual Supply $V_{IN1} \neq V_{IN2}$

The switcher  $V_{OUT}$  supplies the microprocessor I/O voltage. The LDO supplies the core (e.g., 1.8 V nominal) (see [Figure 19](#), page 22).

#### Power Up

This condition depends upon the regulator current limit, load current and capacitance, and the relative rise times of the  $V_{IN1}$  and  $V_{IN2}$  supplies. There are 2 cases:

1.  $V_{OUT}$  rises faster than LDO. The switcher  $V_{OUT}$  uses control methods (1) and (2) described in the [Methods of Control](#) section, page 23.
2. LDO rises faster than  $V_{OUT}$ . The LDO uses control methods (4) and (5) described in the [Methods of Control](#) section.

#### Power Down

This condition depends upon the regulator load current and capacitance and the relative fall times of the  $V_{IN1}$  and  $V_{IN2}$  supplies. There are 2 cases:

1. LDO falls faster than  $V_{OUT}$ . The  $V_{OUT}$  uses control methods (1) and (2) described in the [Methods of Control](#) section, page 23.

In the case  $V_{IN1} = V_{IN2}$  the intrinsic operation will turn both the Buck High-Side FET and the LDO external Pass FET, and will discharge the  $V_{OUT}$  load capacitor into the  $V_{IN}$  supply.

2.  $V_{OUT}$  falls faster than LDO. The LDO uses control methods (4) and (5) described in the [Methods of Control](#) section.

### Shorted Load

1. LDO shorted to ground. The  $V_{OUT}$  uses methods (1) and (2) described in the [Methods of Control](#) section, page 23.
2.  $V_{OUT}$  shorted to ground. The LDO uses control methods (4) and (5) described in the Methods of Control section.
3.  $V_{IN1}$  shorted to ground. This is equivalent to the LDO output shorted to ground.
4.  $V_{IN2}$  shorted to ground. This is equivalent to the switcher  $V_{OUT}$  output shorted to ground.
5. LDO shorted to supply. No load protection.
6.  $V_{OUT}$  shorted to supply. No load protection. 34703 protected by a thermal limit.



## LOGIC COMMANDS AND REGISTERS

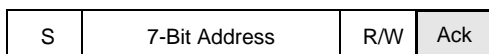
### I<sup>2</sup>C BUS OPERATION

The 34703 device is compatible with the I<sup>2</sup>C interface standard. SDA and SCL pins are the Serial Data and Serial Clock pins of the I<sup>2</sup>C bus.

### I<sup>2</sup>C COMMAND AND DATA FORMATS

#### Communication Start

Communication starts with a START condition, followed by the slave device unique address. [Figure 20](#) illustrates the data transfer beginning an I<sup>2</sup>C communication for a 7-bit slave address.



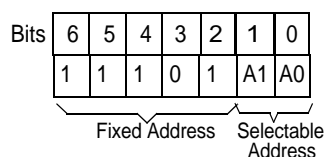
**Figure 20. Communication Using 7-Bit Address**

#### Slave Address Definition

The 34703 has the two LSB's address bits defined by the state of the CLKSEL pin and the ADDR pin.

**Note** The state of the CLKSEL pin also defines the configuration of the oscillator synchronization CLKSYN pin.

This feature allows up to four 34703 ICs to communicate in the same I<sup>2</sup>C bus, all of them sharing the same high-order address bits. A different combination of bits A1 and A0 is assigned to each individual part to assure its unique address. [Figure 21](#) illustrates the flexible addressing feature for a 7-bit address. [Table 7](#) provides the definition of the selectable portion of the device address.



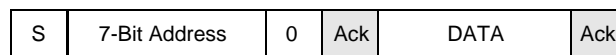
**Figure 21. Address Bit Definition for 7-Bit Address**

**Table 7. Definition of Selectable Portion of Device Address**

CLKSEL Pin	ADDR Pin	A1	A0
Low	Low	0	0
Low	Open	0	1
Open	Low	1	0
Open	Open	1	1

#### Writing Data Into the Slave Device

After the address acknowledgment by the slave, DATA can be written into the slave registers. The R/W bit must be set to 0 so DATA will be written. [Figure 22](#) shows the data write sequence. Actions performed by the slave device are grayed.



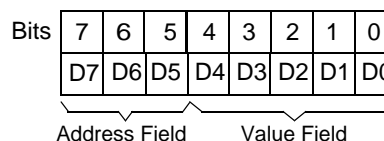
**Figure 22. Data Transfer for Write Operations**

#### Data Definition

For the sake of the 34703 acting as a slave device, the master writes a Command Byte and writes one Data Byte. The Command Byte identifies the kind of operation required by the master and has two fields, as illustrated in [Figure 23](#):

1. Address field
2. Value field

The address field is selected from the list in [Table 8](#).



**Figure 23. Command Byte**

**Table 8. Address Field Definitions**

Code	Operation	Write
001	Voltage Margining	W
010	Not Used	–
011	Watchdog	W

Refer to [Table 10](#), page 26, which summarizes the value field definitions for the entire set of operation options.

## Security in Writing Commands

All writing operations are critical and must not be inadvertently latched after a false command. To improve the security level, a so-called *first command* is defined to initiate each write communications.

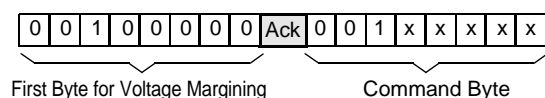
A first command has the Command Byte address field equal to the related operation one, followed by a null value field (all zeros). [Table 9](#) summarizes first command definitions. The master sends the first command before the Command Byte for the intended operation.

**Table 9. First Command Definitions**

First Command	Operation
001 00000	Voltage Margining
011 00000	Watchdog Programming

## Voltage Margining Operation

After starting the communication in Writing mode, the master sends the first command followed by the specific Command Byte to set the required voltage margining for either the LDO or the switcher (see [Figure 24](#)). To achieve a simultaneous set for both LDO and switcher, two specific commands must be issued in sequence after the first command, one for each supply.



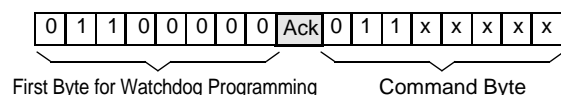
**Figure 24. Voltage Margining Programming (One Supply Only)**

**Note** x bits are defined in [Table 10](#), page 26.

## Watchdog Programming Operation

For watchdog operation control, the master periodically sends a watchdog first command followed by a command byte selecting, or confirming, the watchdog period according to the options listed in [Table 10](#), page 26. Also see [Figure 25](#).

The internal watchdog timer will be cleared each time a watchdog command is written into the device, provided it arrives during the window open time. The Command 01100000 sent twice will shut the time OFF, and the watchdog function will be disabled. Any other valid watchdog command turns on the timer again.



**Figure 25. Watchdog Timer Programming**

**Note** x bits are defined in [Table 10](#), page 26.

**Table 10. Command Byte Definitions**

Operation	Address	Value	Action
Voltage Margining (As a 2nd Command Byte)	0 0 1 0 0 0 0 0	0 0 0 0 0	1st Command
	0 0 1 x 0 0 0 0	0 0 0 0 0	Output Normal
	0 0 1 x 0 0 0 1	0 0 0 0 1	+ 1%
	0 0 1 x 0 0 1 0	0 0 0 1 0	+ 2%
	0 0 1 x 0 0 1 1	0 0 1 1 1	+ 3%
	0 0 1 x 0 1 0 0	0 1 0 0 0	+ 4%
	0 0 1 x 0 1 0 1	0 1 0 0 1	+ 5%
	0 0 1 x 0 1 1 0	0 1 1 0 0	+ 6%
	0 0 1 x 0 1 1 1	0 1 1 0 1	+ 7%
	0 0 1 x 1 0 0 0	1 0 0 0 0	- 1%
	0 0 1 x 1 0 0 1	1 0 0 0 1	- 2%
	0 0 1 x 1 0 1 0	1 0 1 0 0	- 3%
	0 0 1 x 1 0 1 1	1 0 1 0 1	- 4%
	0 0 1 x 1 1 0 0	1 1 0 0 0	- 5%
	0 0 1 x 1 1 0 1	1 1 0 0 1	- 6%
	0 0 1 x 1 1 1 0	1 1 1 0 0	- 7%
Watchdog Programming (As a 2nd Command Byte)	0 1 1 0 0 0 0 0	0 0 0 0 0	1st Command
	0 1 1 0 0 0 0 0	0 0 0 0 0	WD OFF (28)
	0 1 1 0 1 0 0 0	0 0 0 0 0	WD 1280 ms WinOFF
	0 1 1 0 1 0 0 1	0 0 0 0 1	WD 320 ms WinOFF
	0 1 1 0 1 0 1 0	0 0 1 0 0	WD 80 ms WinOFF
	0 1 1 0 1 0 1 1	0 0 1 0 1	WD 20 ms WinOFF
	0 1 1 0 1 1 0 0	0 1 0 0 0	WD 1280 ms WinON
	0 1 1 0 1 1 0 1	0 1 0 0 1	WD 320 ms WinON
	0 1 1 0 1 1 1 0	0 1 1 0 0	WD 80 ms WinON
	0 1 1 0 1 1 1 1	0 1 1 0 1	WD 20 ms WinON

Notes

28. The Watchdog feature will be turned ON automatically after receiving any other valid command byte changing watchdog time.

### Communication Stop

Only the master can terminate the data transfer by issuing a STOP condition. The slave waits for this condition to resume its initial state waiting for the next START condition (see [Figure 26](#)).

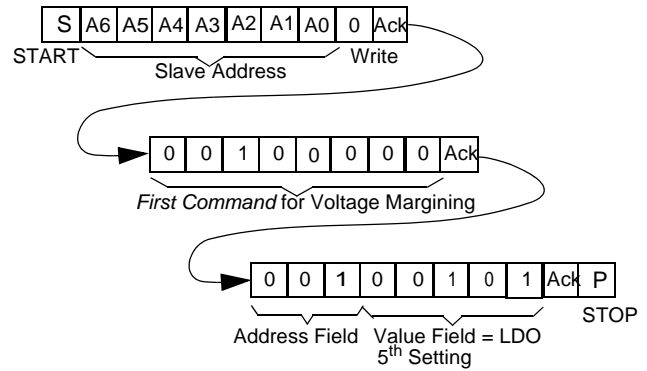
### Data Transfer Example

The master device controlling the I<sup>2</sup>C bus will always start addressing a 34703 slave IC in writing mode (R/W = 0) in order to be able to write a Command Byte just after the address acknowledge. I<sup>2</sup>C bus protocol defines this circumstance as a master-transmitter and slave-receiver configuration.

Eventually this Command Byte can again define a Write operation (e.g., Voltage Margining, see [Figure 26](#)), and the master will keep the data transfer direction.

[Figure 26](#) illustrates a communication beginning with the slave address, the *first command* for voltage margining, and a third byte containing the address field 001 and the value field 00101 corresponding with the LDO fifth setting (LDO output voltage = +5% above its nominal value). If a simultaneous setting for switcher is needed, a fourth byte

should be included before the STOP condition (P); for instance, 001 10010 to set switcher in its second setting (switcher output voltage = +2% above its nominal value).



**Figure 26. Complete Data Transfer Example**

## TYPICAL APPLICATIONS

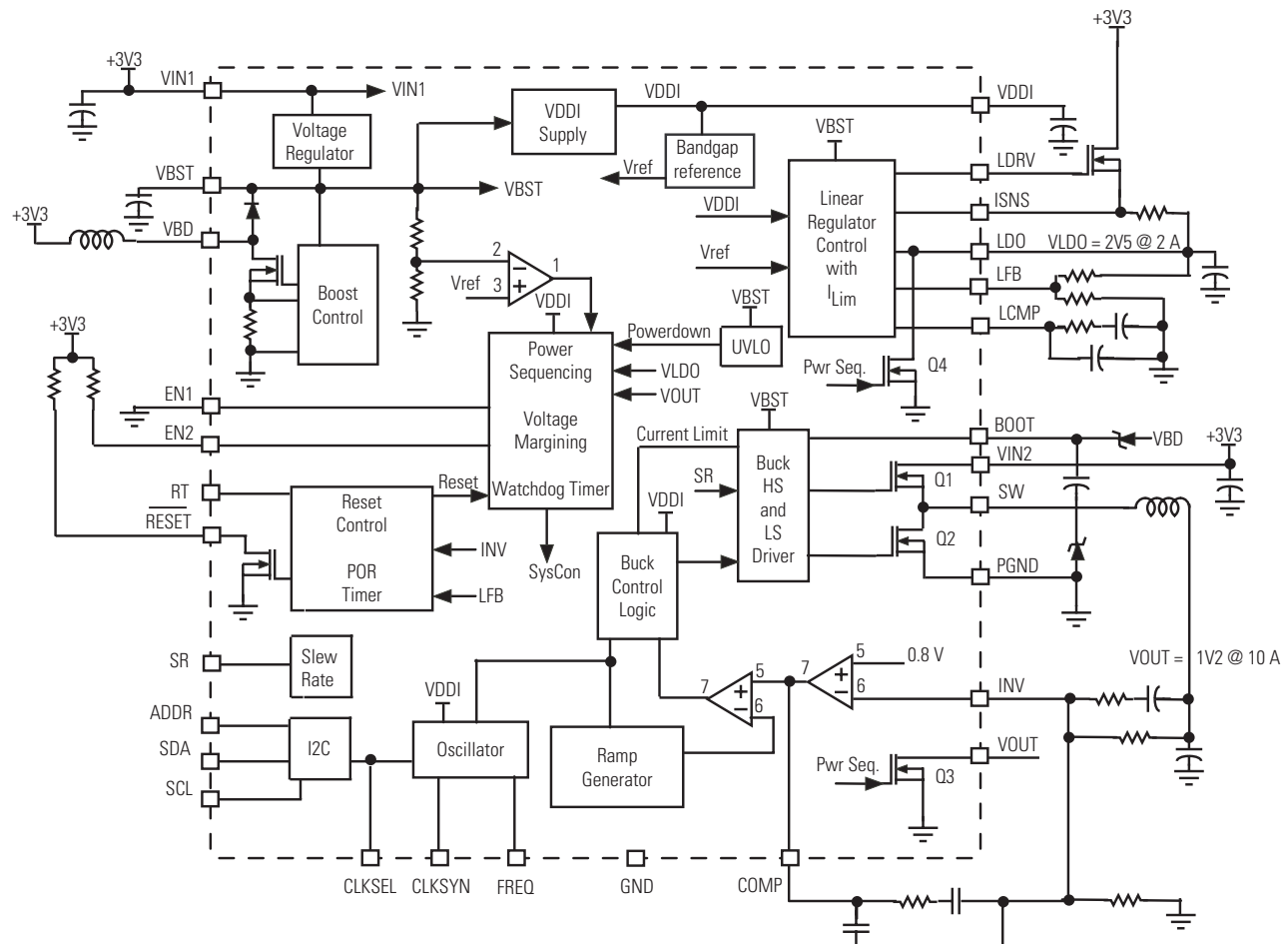


Figure 27. 34703 Typical Application

## BOOST REGULATOR

When the input voltage to be used is less than 8.0 V, the boost regulator should be used. The boost regulator is made active by adding a small external inductor, and provides an output voltage of 8.0 V nominal value for driving the gates of the buck regulator power MOSFETs, the linear regulator power MOSFET gate, and also for the internal  $V_{ddi}$  supply. The boost inductor value should be at least 10  $\mu$ H for the proper boost operation. NOTE: If the input voltage to be used is greater than 8 V, the boost regulator must not be implemented, and the boost inductor, if present, must be removed from the circuit. A 0.1  $\mu$ F capacitor is recommended to be added at Pin VBST for filtering high frequency noise in the system board.

## BUCK REGULATOR

## Output Voltage Setting

The buck output voltage is set by an external resistor network ( $R_9$  and  $R_{14}$ ) and an internal reference voltage. The external resistor network feeds back the dc output voltage, and an error amplifier compares it with an internal reference voltage  $V_{ref}$  (See Figure 28). The buck output voltage can be calculated from the following equation:

$$V_{\text{output}} = V_{\text{ref}} \times (1 + R_9/R_{14})$$

Where  $V_{\text{ref}}$  designed in MC34703 is 0.8 V typ.

If  $R_9$  is chosen as 5.1 k $\Omega$  (recommended),  $R_{14}$  will be calculated as 4.08 k $\Omega$  for the output voltage of 1.8 V; in a same manner,  $R_{14}$  is 1.63 k $\Omega$  for an output voltage of 3.3 V.

We recommend using 1% tolerance resistors ( $R_9$  and  $R_{14}$ ) for the precise output voltage.

The following table shows the recommendation values of  $R_9$  and  $R_{14}$  as referred to different buck output voltages:

**Table 11. Recommendation of  $R_9$  and  $R_{14}$  Value for Different Output Voltage**

V <sub>o</sub>	R <sub>9</sub> (K $\Omega$ )	R <sub>14</sub> (K $\Omega$ )
0.8	5.1	•
1.8	5.1	4.12
2.0	5.1	3.4
3.3	5.1	1.65
5.0	5.23	1.0

### Compensation Loop Determination

The MC34703 has a simple PWM voltage mode control loop to achieve an excellent line and load regulation. The goal for the compensation loop circuit design is to achieve as

high as possible unit gain crossover frequency with a gain slope of -1, and enough phase margin (at least 45°) for the closed loop transfer function. The bandwidth should be between 20 -30% of the switching frequency. In the power system, there is a double pole created by the output LC filter, and a zero generated by output capacitor ESR (equivalent series resistance).

The poles are located:

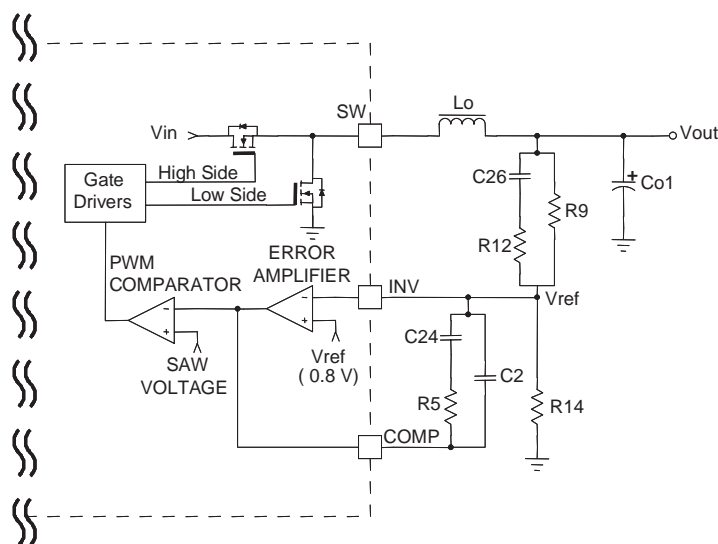
$$F_{p1, p2} = \frac{1}{2\pi\sqrt{L_O \times C_O}}$$

The zero is located:

$$F_{z1} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

Where  $C_O$  is the capacitance of the output capacitor,  $L_O$  is the inductance of the output filter inductor.  $R_{ESR}$  is the total equivalent series resistance of output capacitors.

Based on the typical system conditions, the type 3 compensation scheme has been chosen to use as shown in [Figure 28](#).



**Figure 28. Buck Regulator Compensation Circuit**

The location of the three poles and two zeros from the transfer function is shown by the following equations:

$$F_{s,p1} = 0$$

$$F_{s,p2} = \frac{C_2 + C_{24}}{2\pi \times R_5 \times C_2 \times C_{24}}$$

$$F_{s,p3} = \frac{1}{2\pi \times R_{12} \times C_{26}}$$

$$F_{s,z1} = \frac{1}{2\pi \times R_5 \times C_{24}}$$

$$F_{s,z2} = \frac{1}{2\pi \times (R_9 + R_{12}) \times C_{26}}$$

Figure 29 shows the asymptotic bode gain and phase plot for the type 3 compensation scheme. The poles and /or zeroes are adjusted in order to shape the gain profile and make sure the phase has sufficient margin (to meet the system stability criteria).

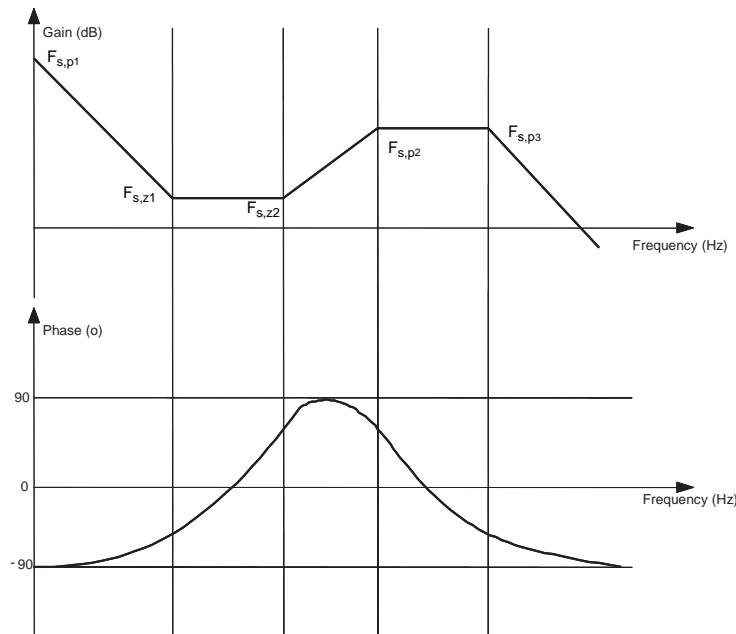


Figure 29. Bode and Phase plot for Type Compensation Scheme

### Output Inductor Calculation

If the output inductor is designed to guarantee the buck regulator will operate at critical mode or continuous mode within all load conditions, the following equation will be used to calculate the inductance of the output inductor:

$$L \geq \frac{V_{\text{output}} \times (V_{\text{in}} - V_{\text{output}})}{2 \times I_{\text{output}} \times V_{\text{in}} \times F_s}$$

Where L is the output inductor value in Henries,  $V_{\text{in}}$  is the input voltage in Volts,  $I_{\text{output}}$  is the minimum output current in Amps, and  $F_s$  is the switching frequency in Hertz. In this equation, the magnitude of the ripple current is assumed as 2 times minimum load current.

For example: Input voltage is 5.5 V, minimum output current is 0.2 A, output voltage is 1.8 V, the operating frequency is 300 kHz, the inductance of output inductor is calculated as 10  $\mu\text{H}$  for an initial value.

### Output Capacitor Calculating

The minimum capacitance of output capacitor could be calculated from the following equation:

$$C_{\text{Omin}} = \frac{V_{\text{output}}}{8 \times F_s^2 \times L \times \Delta V_{\text{pp}}} \times (1 - D)$$

Where  $D$  is minimum switching duty cycle,  $F_s$  is the operating frequency in Hertz,  $L$  is output inductance in Henries, and  $\Delta V_{pp}$  is output ripple voltage in Volts.

For example, if the output voltage is 1.8V, the minimum duty cycle is 33%, the operating frequency is 300 kHz, the inductance is 10H and  $\Delta V_{pp}$  is 50 mV, the minimum capacitance of output capacitor will be calculated as 3.3  $\mu$ F, as start value. However, this value is only concerned with the ripple voltage. In the system, one needs to consider load changes from overload to minimum load and keep the output voltage within spec, so that the actual output capacitor value varies with the system requirements.

The relationship between the ripple voltage and the ESR of output capacitor is shown as follows:

$$\Delta V_{pp} = \Delta I_{ripple} \times R_{ESR}$$

### Output Current Limit Setting

The default setting of the limit is 11 A. When the output current exceeds 11 A, the current limit timer starts to time out while the control circuit limits the output current. If the over current condition lasts for more than 10 ms, the buck regulator is shut off and tuned on again after 100 ms. This type of operation provides equivalent protection to the analog "current fold-back" operation. See [Figure 30](#).

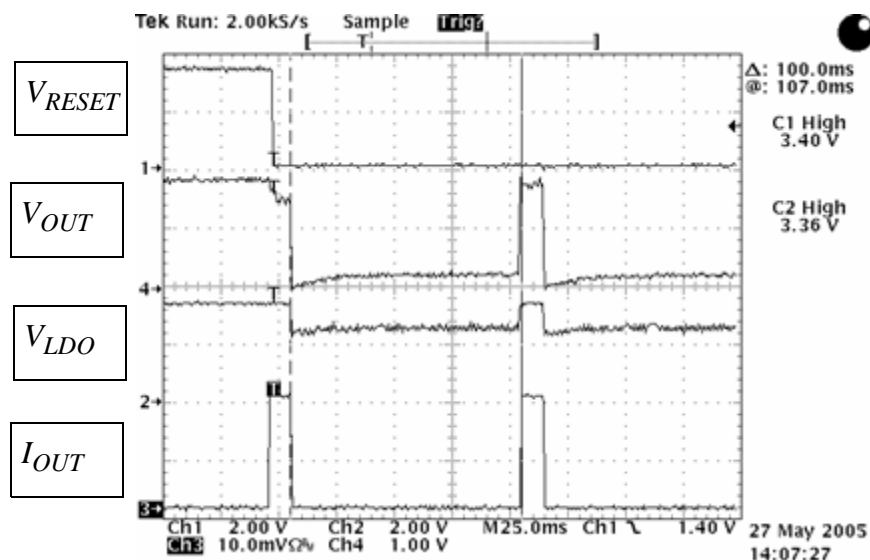


Figure 30. Buck is in the Over Current Condition

When the buck output current (Channel 3) reaches and exceeds limit, Reset Pin (Channel 1) is pulled down immediately. Channel 4 is Buck output voltage (1.8V); Channel 2 is LDO output voltage (3.3V).

## LINEAR REGULATOR

### Output Voltage Setting

The output voltage ( $V_{LDO}$ ) of the linear regulator (LDO) can be set by the following equation:

$$V_{ldo} = V_{ref} \times \left(1 + \frac{R_{11}}{R_{10}}\right)$$

Where  $V_{REF}$  is the linear regulator reference voltage, typically is 0.8V at the LFB Pin.

[Figure 31](#) shows the MC34703 linear regulator circuit with its compensation circuit.

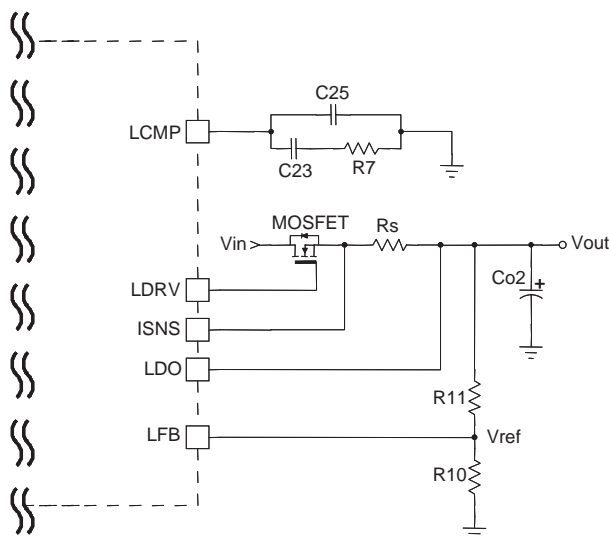
For example, if  $R_{10}$  is chosen as 15 k $\Omega$  (recommended),  $R_{11}$  will be calculated as 18.75 k $\Omega$  for the output voltage of 1.8 V; in a same manner,  $R_{11}$  is 46.87 k $\Omega$  for the output voltage of 3.3 V.

We recommend using 1% tolerance resistors ( $R_{10}$  and  $R_{11}$ ) for the precise output voltage.

The following table shows the recommended values of and referred to different buck output voltage:

Table 12. Recommendation of and Value for Different Voltage

$V_o$	$R_{10}$ (K $\Omega$ )	$R_{11}$ (K $\Omega$ )
0.8	15	•
1.8	15	18.7
2.0	15	22.6
3.3	15	47
5.0	15	78.7



### Figure 31. Linear Regulator Circuit

## Compensation Components Setting

The compensation component values have been determined by the design. The recommended values are the following:

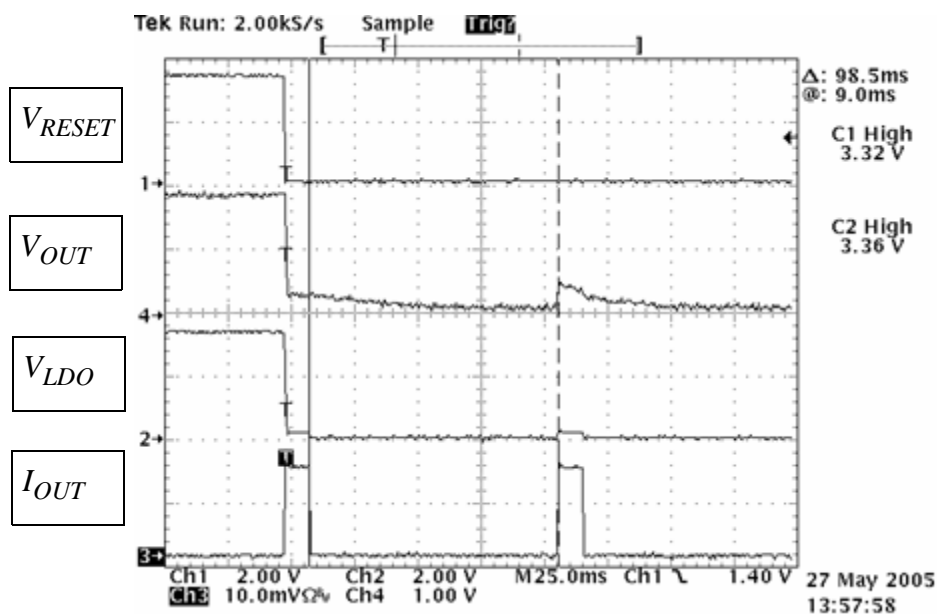
$$C_{25} = 10\text{nF}, C_{23} = 6.8\text{nF}, R_7 = 1.5\text{K}\Omega$$

Since the compensation component values designed are dependent on the output capacitor value, the capacitance of 10  $\mu$ F for the output capacitor  $C_o$  is recommended.

## Output Current Limit Setting

The current limit of the linear regulator can be adjusted by means of an external current sense resistor  $R_s$ , see

**Figure 31.** The voltage drop caused by the regulator output current flowing through the current sense resistor is sensed between the LDO and the ISNS pins. When the sensed voltage exceeds 45 mV (Design), the current limit timer starts to time out while the control circuit limits the output current. If the over current condition lasts for more than 10 ms, the linear regulator is shut off and tuned on again after 100 ms. This type of operation provides equivalent protection to the analog “current fold-back” operation. [Figure 32](#) shows a sample of the LDO in the Over current protection.



### Figure 32. LDO in the Over Current Condition



When the LDO output current (Channel 3) reaches and exceeds limit, Reset Pin (Channel 1) is pulled down immediately. Channel 2 is LDO output voltage (3.3 V); Channel 4 is Buck output voltage (1.8 V).

The current limit of the LDO can be set by using the following formula:

$$R_s = \frac{45\text{mV}}{I_{\text{LIMIT}}}$$

### Power MOSFET Selecting

To keep the LDO working under stable operation, low input capacitance is recommended for the external power MOSFET. However, if input capacitance is too small, it may lead the feedback loop into an unstable region. In this case, a suggested MOSFET for the LDO, is IRL2703S or NTD60N02R from On Semiconductor.

### Layout Guidelines

To achieve a working power supply (regulator) design, care must be taken in the PCB layout, not just the electrical design. The PCB layout plays a critical role in the power supply performance. A good PCB layout design will improve regulation parameters and electromagnetic compatibility (EMC) performance of switching power supply. In order to

avoid any inductive or capacitive coupling of the switching power supply noise into the sensitive analog control circuits, the noisy power ground and clean quiet signal ground should be well separated on the PCB board, and connected only at one point. The power routing should be made by heavy traces or area of copper. The power path and its return should be placed, if possible, on top of each other on different layers or opposite sides of the PCB board.

The switching power supply input and output capacitors should be physically placed very close to the power pins (Vin2, SW, and PGND) of the 34703. Their ground pins, together with the 34703 power ground pins (PGND), should be connected by a single island of the power ground copper to create the "single island" grounding.

The bootstrap capacitor should be tightly connected to the integrated circuit as well. The same guidelines as those for the layout of the main switching buck regulator should be applied to the layout of the low power auxiliary boost regulator and to some extent, the power path of the linear regulator.

A four layer PCB is recommended for this product. It is imperative to provide a  $V_{\text{OUT}} (-)$  pin at the ground side of the output capacitors, in order to ensure adequate load regulation. The same is also true for LDO.

It is also recommended that the vias on the PCB used to connect the second row of contacts (pins 13 to 21) on the IC, have a hole diameter no larger than 0.009".

## TYPICAL APPLICATION CIRCUIT

### PCB LAYOUTS AND BOM

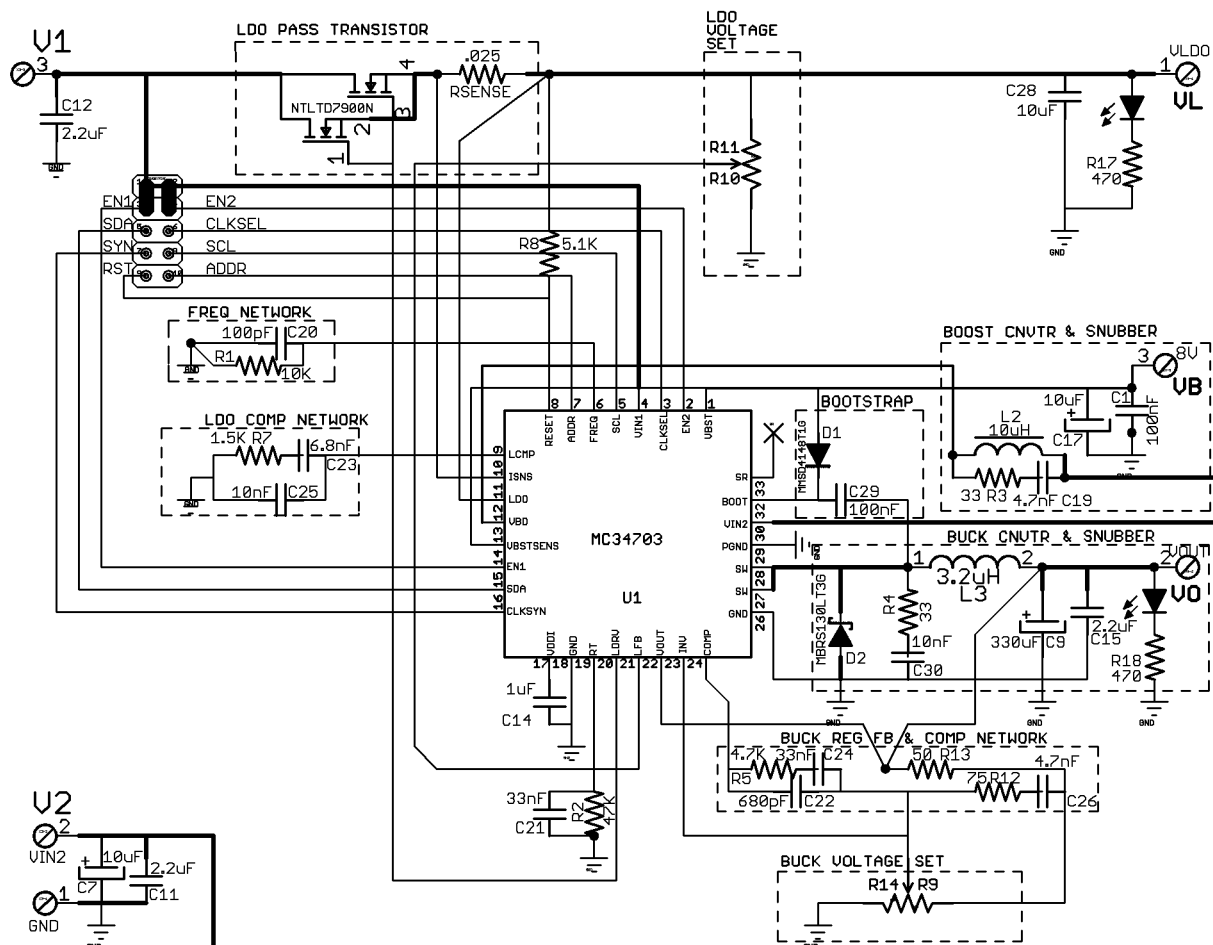


Figure 33. A Typical Application Circuit Schematic

**Table 13. Bill of Material of a Typical Application Circuit**

Application Bill of Material			
NOTE: ALL BOM COMPONENTS ARE RoHS COMPLIANT. 4-layer PCB TO BE SMONiG (soldermask over Nickel Gold Flash) with micro vias plated with Cu until filled nearly solid (9mil thru-holes plated until diameter < 5mil).			
Part-ID	Value	Device	Package & Description
U1	MC34703	MC34703	PQFN33 FREESCALE Power Management IC
Q1	NTLTD7900N	MOSFET	CHIPFET Protected Power MOSFET (ON Semi)
D1	MMSD4148T1G	diode	SOD123 Switching DIODE (ON Semi)
VO, VL	RED or YEL	CHIPLED	0603
C9	330 $\mu$ F	ALEL	UHN1C331MPD Nichicon Ultra Low Impedance
C7, C17	10 $\mu$ F	ALEL	ECEA1EKS100 (Panasonic KS series)
C11, 12, 15	2.2 $\mu$ F	CERAMIC	C1206 CAPACITOR
C1	100 nF	CERAMIC	C1206 CAPACITOR
C28	10 $\mu$ F	CERAMIC	C1206 ECJ-3YB1E106M (Panasonic X5R series, digikey# PCC2326TR-ND
C14	1 $\mu$ F	CERAMIC	C1206 CAPACITOR
C29	100 nF	CERAMIC	C1206 CAPACITOR
C21, C24	33 nF	CERAMIC	C1206 CAPACITOR
C25, C30	10 nF	CERAMIC	C0603 CAPACITOR
C23	6.8 nF	CERAMIC	C0603 CAPACITOR
C19	4.7 nF	CERAMIC	C0805 CAPACITOR
C26	4.7 nF	CERAMIC	C1206 CAPACITOR
C22	680 pF	CERAMIC	C0603 CAPACITOR
C20	100 pF	CERAMIC	C0603 CAPACITOR
L2	10 $\mu$ H	INDUCTOR	16T#30AWG WOUND ON T26-18 Micrometals.com CORE
L2-alt.	10 $\mu$ H	INDUCTOR	22T#30AWG WOUND ON T20=70 Micrometals.com CORE
L3	3.2 $\mu$ H	INDUCTOR	6T#18AWG WOUND ON T50-70D Micrometals.com CORE
L3-alt.	2.2 $\mu$ H	INDUCTOR	9T#18AWG WOUND ON T50-18B Micrometals.com CORE
RSENSE	.025	NONINDUCTIVE	WW RESISTOR WLAR025FE (Ohmite.com)
R1	10K	R-US_R0603	R0603 RESISTOR
R2	47K	R-US_R0603	R0603 RESISTOR
R3	33	R-US_R0603	R0603 RESISTOR
R4	33	R-US_M1206	M1206 RESISTOR
R5	4.7K	R-US_R0603	R0603 RESISTOR
R7	1.5K	R-US_R0603	R0603 RESISTOR
R8, R9	5.1K	R-US_R0603	R0603 RESISTOR
R10	22K	R-US_R0603	R0603 RESISTOR
R11	47K	R-US_R0603	R0603 RESISTOR
R12	75	R-US_R0603	R0603 RESISTOR
R13	50	R-US_R0603	R0603 RESISTOR
R14	10K	R-US_R0603	R0603 RESISTOR
R17, R18	470	R-US_R0603	R0603 RESISTOR
R15, R16	50K	10TURN TRIMPOT	3223-W-1-503-E BOURNS SMD Trimming Potentiometer

## Notes

29. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

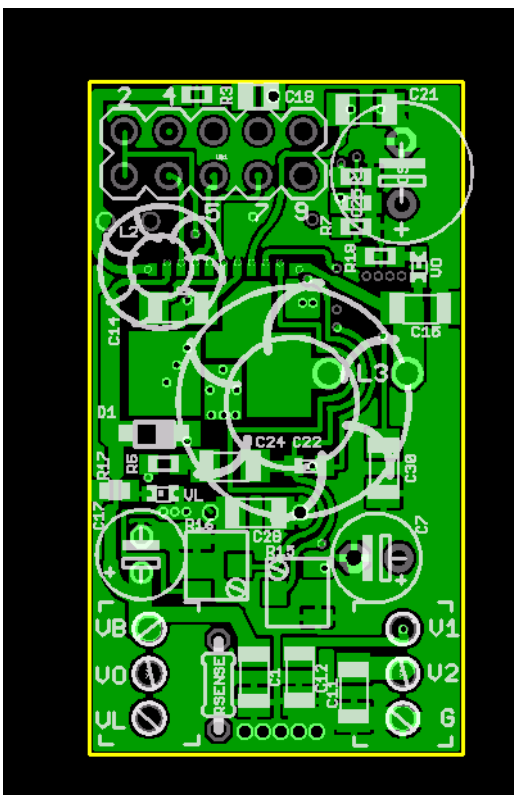


Figure 34. PCB Layer 1

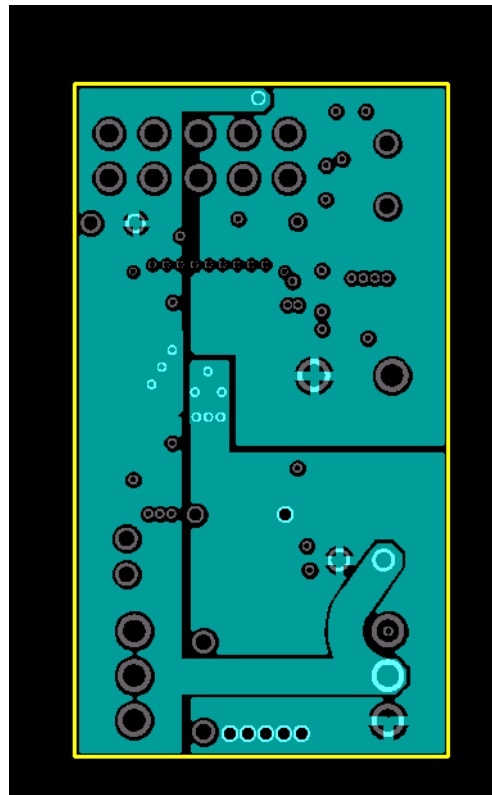


Figure 36. PCB Layer 3

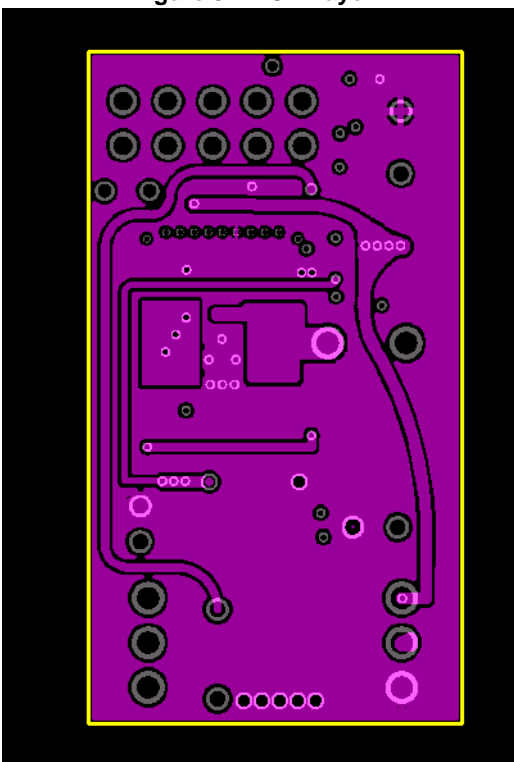


Figure 35. PCB Layer 2

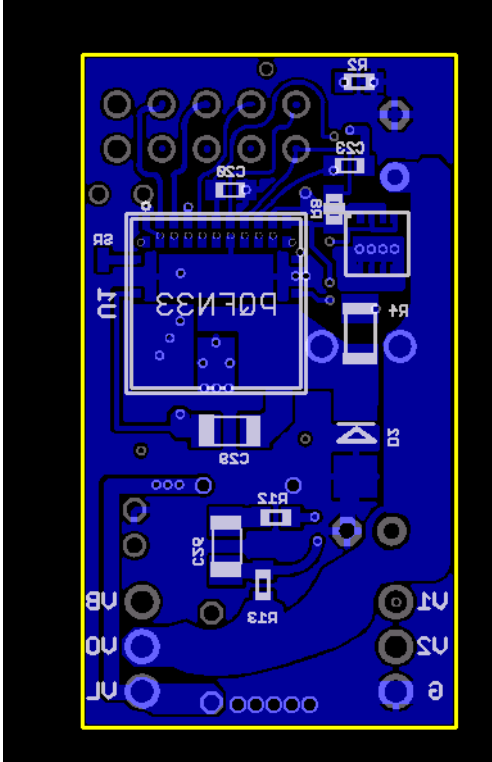


Figure 37. PCB Layer 4

## TYPICAL WAVEFORM CHARACTERISTICS OF THE EVB BOARD

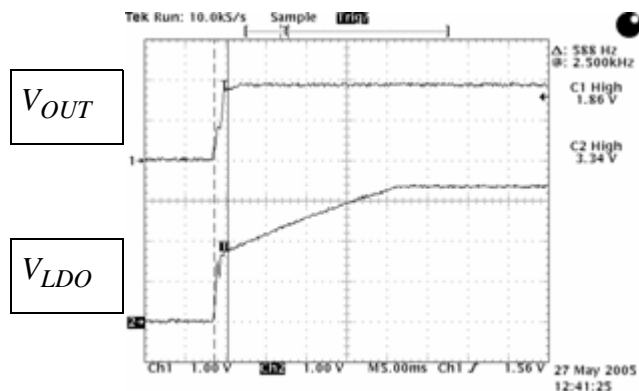


Figure 38. Power Up Sequences  
(Standard Mode,  $V_{in} = 5\text{ V}$ ,  $V_{output} = 1.8\text{ V}$ ,  $V_{LDO} = 3.3\text{ V}$ )

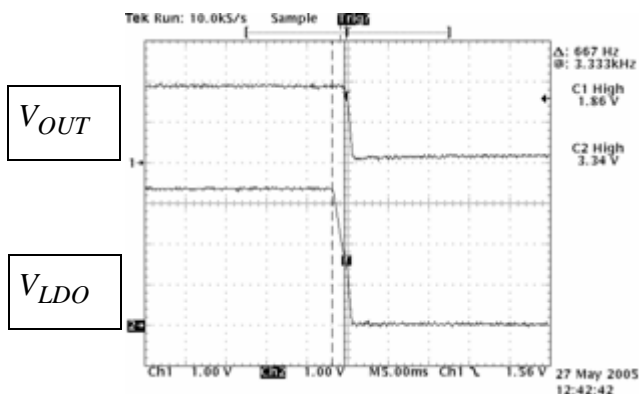


Figure 39. Power Down Sequences  
(Standard Mode,  $V_{in} = 5\text{ V}$ ,  $V_{output} = 1.8\text{ V}$ ,  $V_{LDO} = 3.3\text{ V}$ )

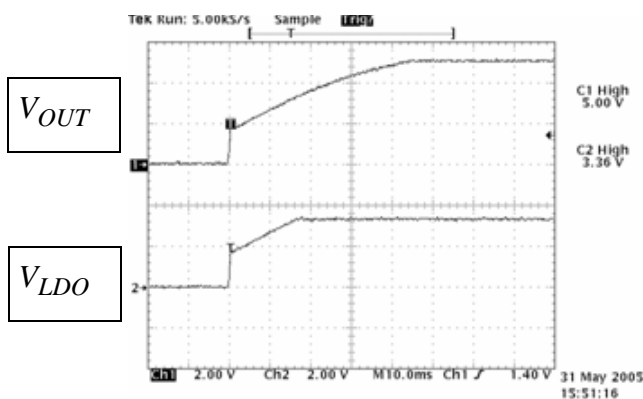


Figure 40. Power Up Sequences  
(Inverted Mode,  $V_{in} = 7\text{ V}$ ,  $V_{output} = 5\text{ V}$ ,  $V_{LDO} = 3.3\text{ V}$ )

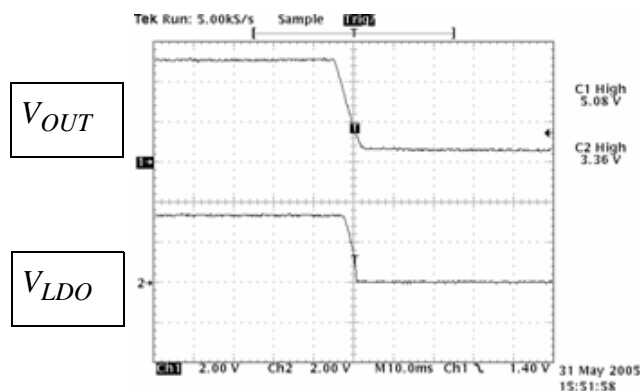


Figure 41. Power Down Sequences  
(Inverted Mode,  $V_{in} = 7\text{ V}$ ,  $V_{output} = 5\text{ V}$ ,  $V_{LDO} = 3.3\text{ V}$ )

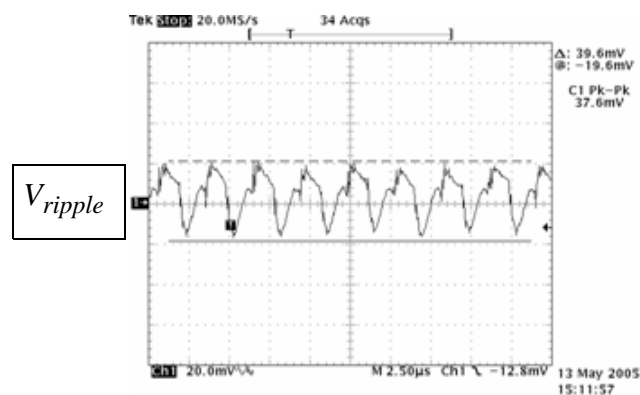


Figure 42. Output Ripple Voltage ( $V_{in} = 5\text{ V}$ ,  $I_o = 10\text{ A}$ )

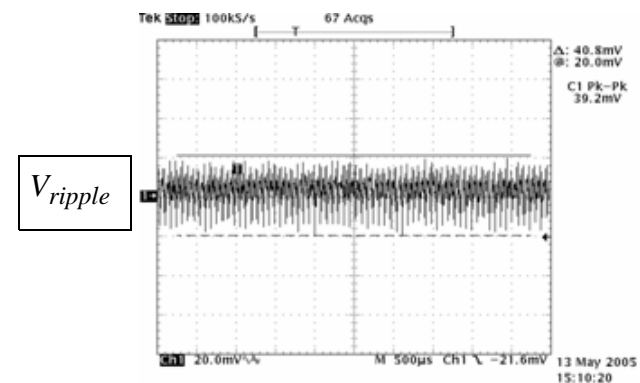


Figure 43. The Same Output Waveform as Figure 42

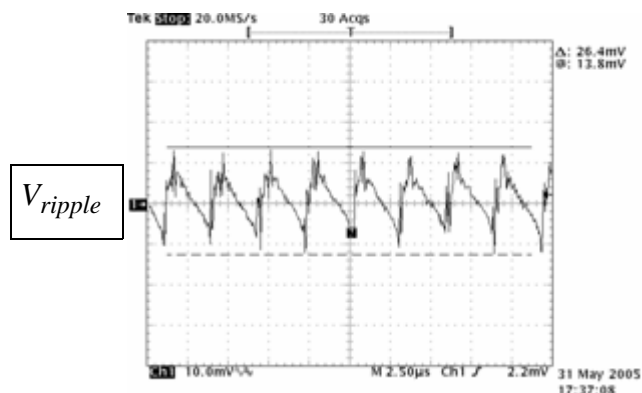


Figure 44. Output Ripple Voltage ( $V_{in} = 10\text{ V}$ ,  $I_o = 10\text{ A}$ )

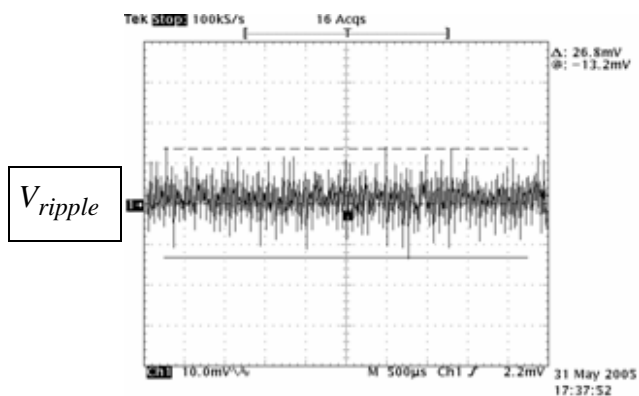


Figure 45. The Same Output Waveform as Figure 44

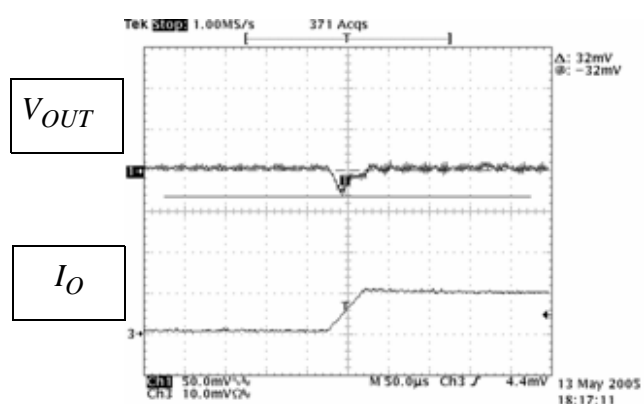


Figure 46. Load Transient Response  
(Step-Up  $I_o = 0.1\text{ A} - 5\text{ A}$ )

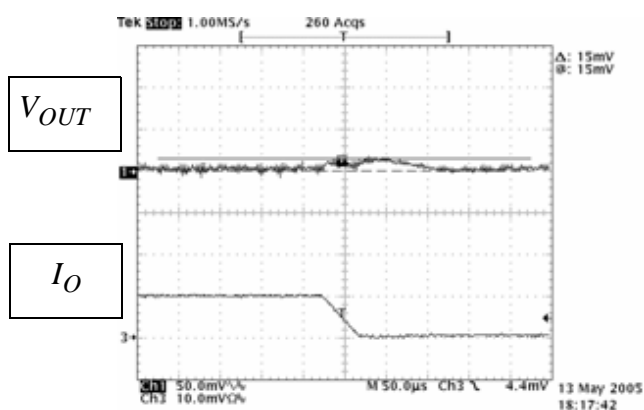
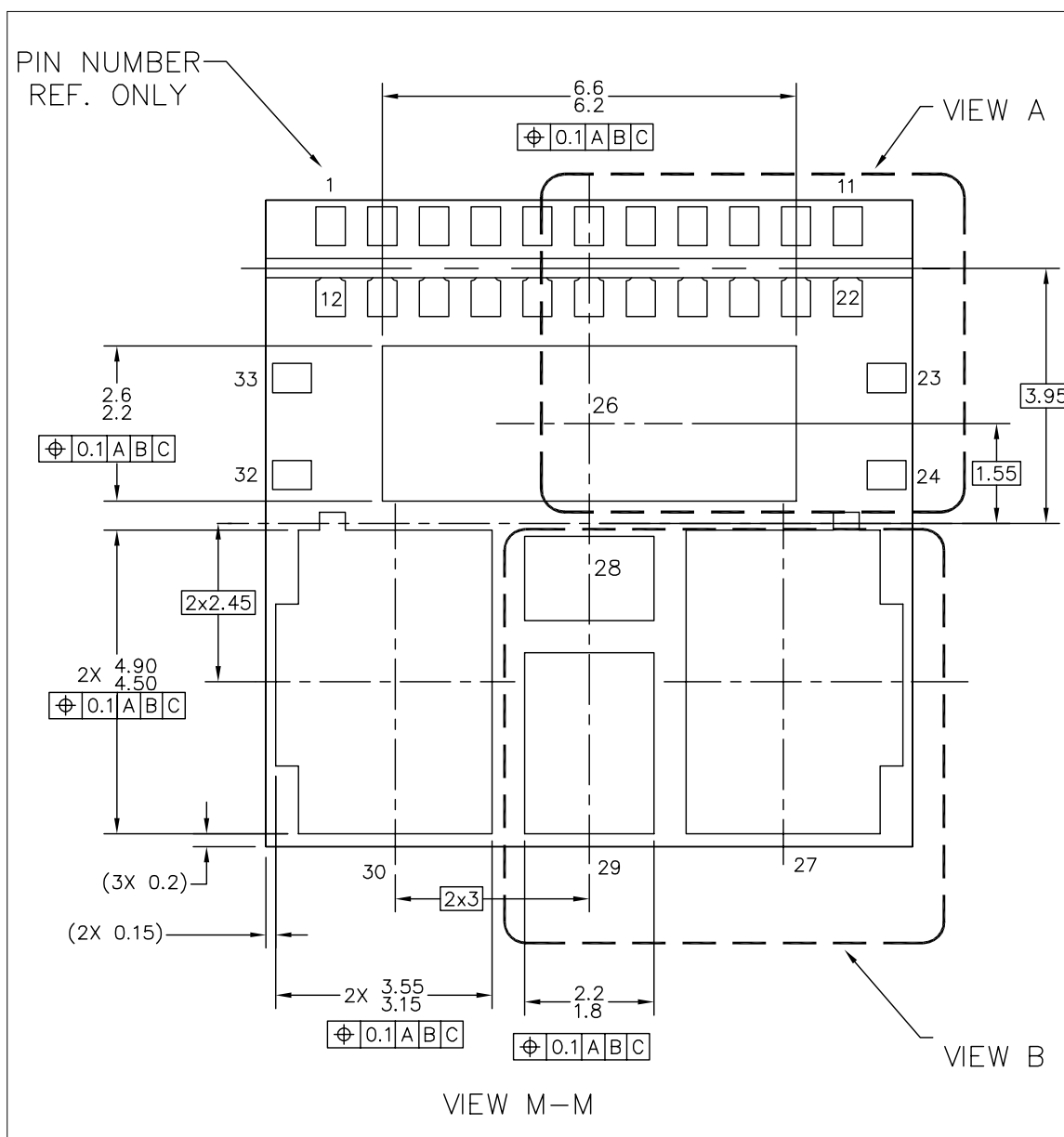


Figure 47. Load Transient Response  
(Step-Down  $I_o = 5\text{ A} - 0.1\text{ A}$ )

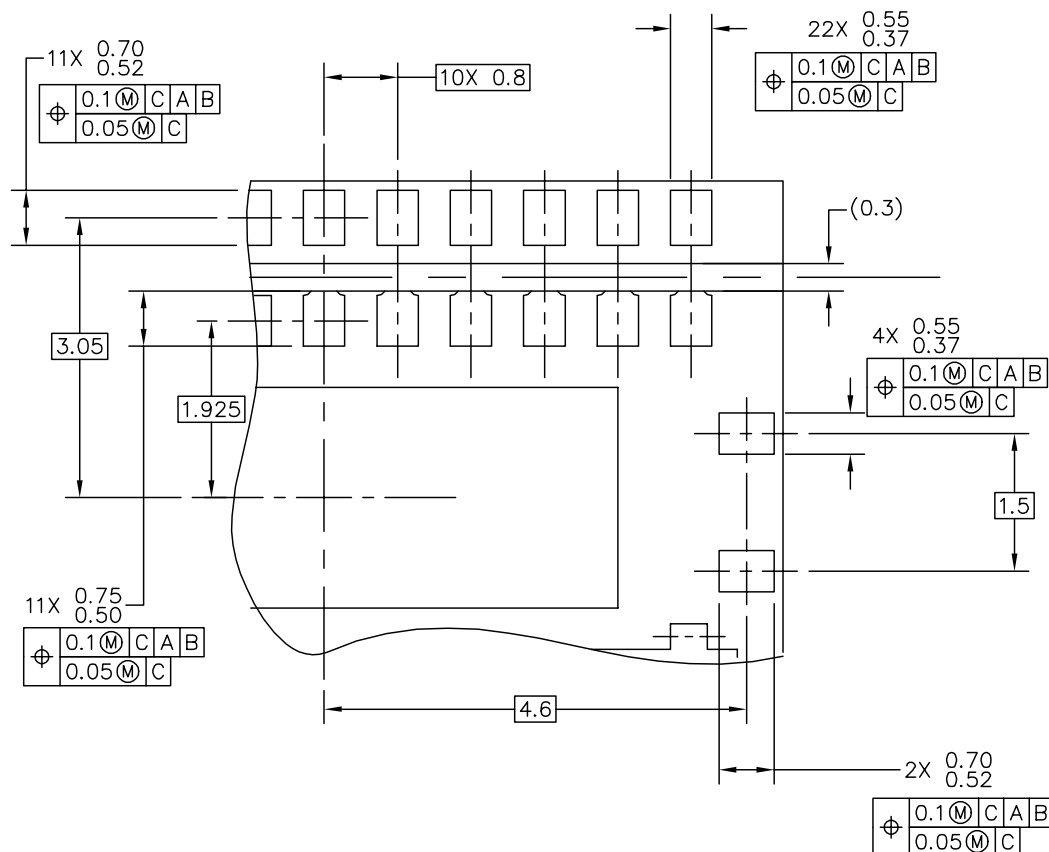




© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN) 33 TERMINAL, 0.8 PITCH(10X10X2.1)	DOCUMENT NO: 98ASA10705D		REV: 0
	CASE NUMBER: 1798-01		1 NOV 2005
	STANDARD: NON-JEDEC		

**PNB SUFFIX**  
33-PIN PQFN  
PLASTIC PACKAGE  
98ASA10705D  
ISSUE 0

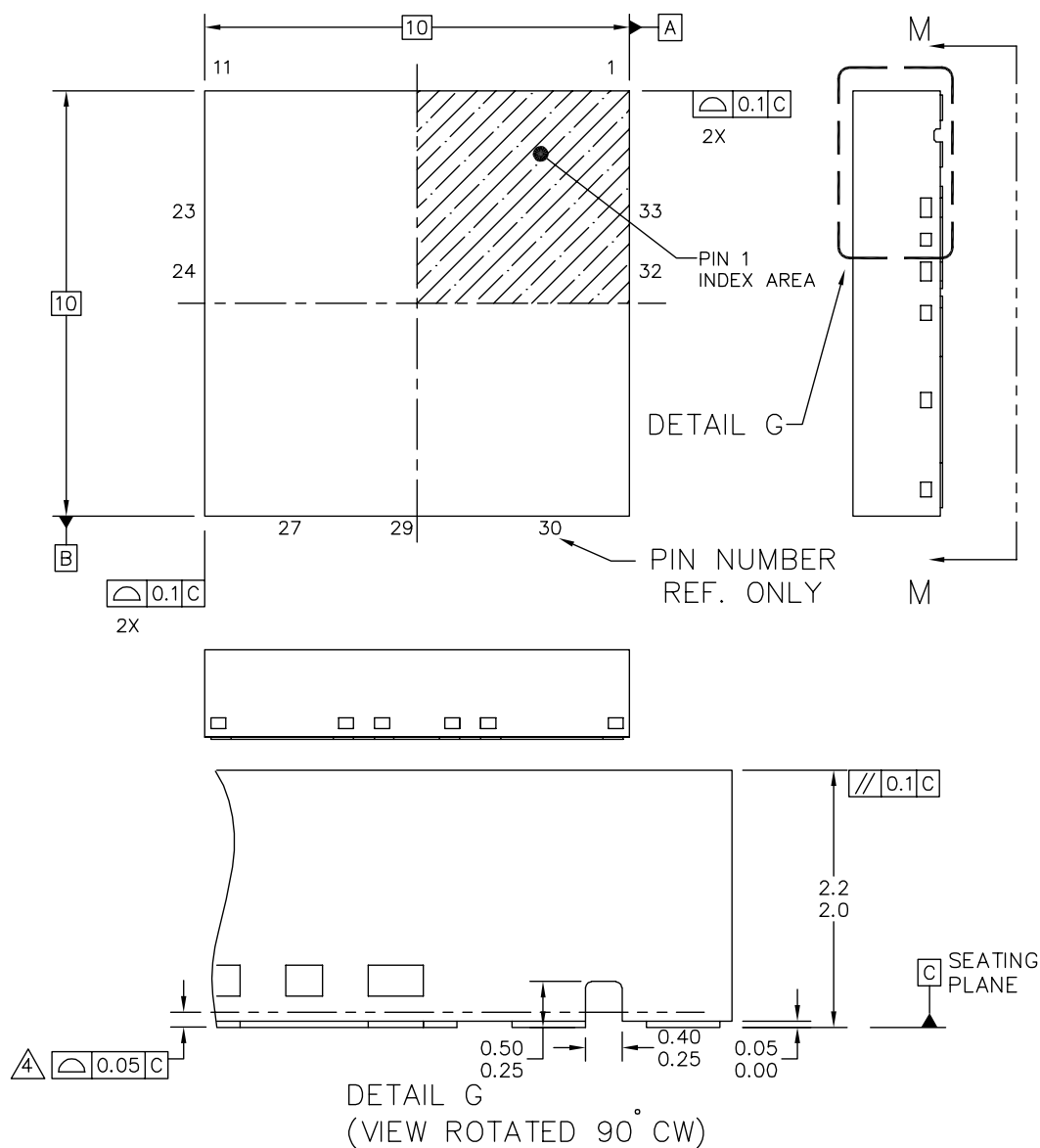




VIEW A

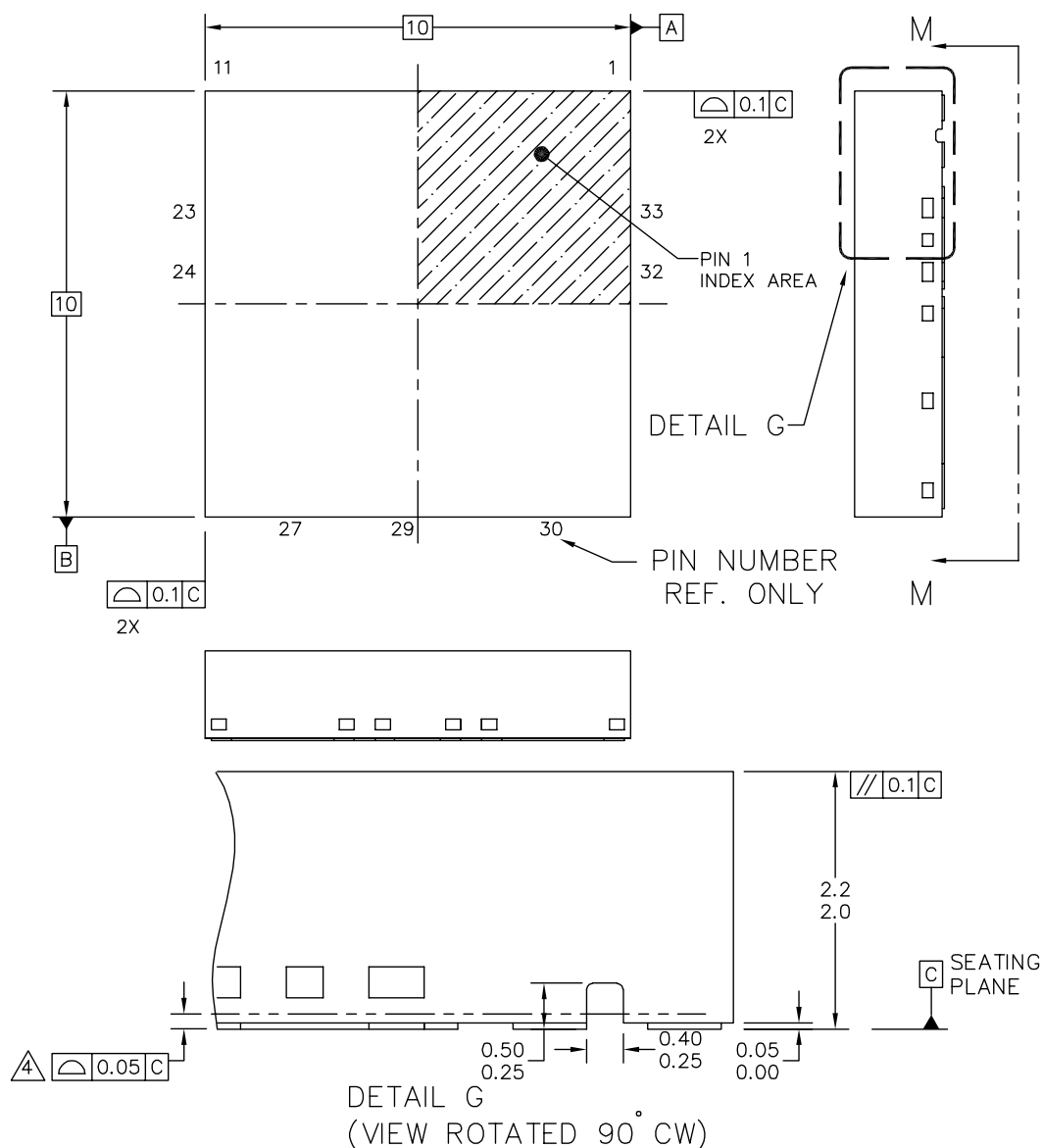
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN) 33 TERMINAL, 0.8 PITCH(10X10X2.1)	DOCUMENT NO: 98ASA10705D		REV: 0
	CASE NUMBER: 1798-01		1 NOV 2005
	STANDARD: NON-JEDEC		

**PNB SUFFIX**  
33-PIN PQFN  
PLASTIC PACKAGE  
98ASA10705D  
ISSUE 0



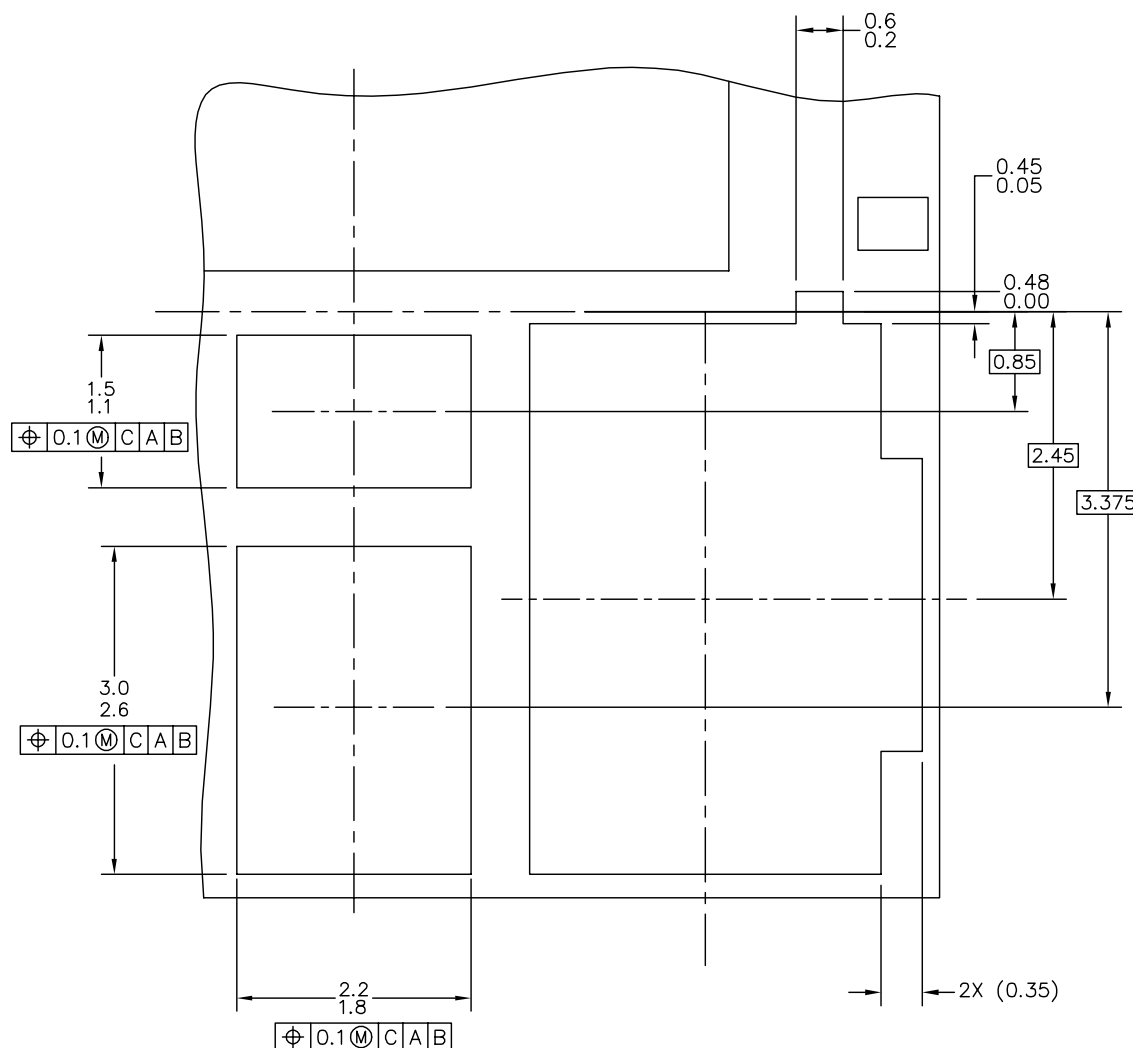
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		<b>MECHANICAL OUTLINE</b>		PRINT VERSION NOT TO SCALE	
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN) 33 TERMINAL, 0.8 PITCH(10X10X2.1)		DOCUMENT NO: 98ASA10705D		REV: 0	
		CASE NUMBER: 1798-01		1 NOV 2005	
		STANDARD: NON-JEDEC			

**PNB SUFFIX**  
33-PIN PQFN  
PLASTIC PACKAGE  
98ASA10705D  
ISSUE 0



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN) 33 TERMINAL, 0.8 PITCH(10X10X2.1)		DOCUMENT NO: 98ASA10705D		REV: 0	
		CASE NUMBER: 1798-01		1 NOV 2005	
		STANDARD: NON-JEDEC			

**PNB SUFFIX**  
33-PIN PQFN  
PLASTIC PACKAGE  
98ASA10705D  
ISSUE 0



VIEW B

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN) 33 TERMINAL, 0.8 PITCH(10X10X2.1)	DOCUMENT NO: 98ASA10705D		REV: 0
	CASE NUMBER: 1789-01		1 NOV 2005
	STANDARD: NON-JEDEC		

**PNB SUFFIX**  
33-PIN PQFN  
PLASTIC PACKAGE  
98ASA10705D  
ISSUE 0

## REVISION HISTORY

Revision	Date	Description of Changes
0.0		Initial Release
2.0	8/2005	<ul style="list-style-type: none"> <li>Implemented Revision History page</li> <li>Incorporated engineering comments</li> <li>Converted to Freescale format</li> </ul>
3.0	11/2005	<ul style="list-style-type: none"> <li>Added new 98ASA10705D Drawing</li> <li>Updated ISO drawing</li> </ul>
4.0	2/2006	<ul style="list-style-type: none"> <li>Updated Introduction / Features</li> <li>Revised Figure 1, Simplified Application Diagram</li> <li>Revised Table 1, Pin Definitions</li> <li>Revised Typical Application Section</li> <li>Changed Table 3, Static Buck Converter Peak Current Limit (High Level) Max rating from 18 to 19 and LDO Internal Pull-Down MOSFET <math>R_{DS(ON)}</math>, <math>I_D = 1.0\text{ A}</math>, <math>T_A = 25^\circ\text{C}</math>, <math>V_{BST} = 8.0\text{ V}</math> Max rating from 3.0 to 3.2</li> <li>Condensed Bill of Material.</li> <li>Corrected pin definitions on <math>V_{BST}</math>, <math>\overline{\text{RESET}}</math>, <math>\text{CLKSYN}</math>, and GND (pin 26)</li> <li>Corrected images for Internal Block Diagram, Pin Connections, and Typical Applications to reflect changes made to <math>\overline{\text{RESET}}</math> and GND pins.</li> <li>Clarified description of the Buck Converter in the Functional Internal Block Description.</li> <li>Changed Output Current Slew Rate from TBD to <math>2.5\text{ A}/\mu\text{s}</math>.</li> </ul>
5.0	8/2006	<ul style="list-style-type: none"> <li>Minor corrections to typical application graphics</li> <li>Updated to the prevailing Freescale form and style</li> </ul>

## ***How to Reach Us:***

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **E-mail:**

[support@freescale.com](mailto:support@freescale.com)

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should a Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, the Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.  
I<sup>2</sup>C is a Trademark of Koninklijke Philips Electronics N.V.

© Freescale Semiconductor, Inc., 2006. All rights reserved.