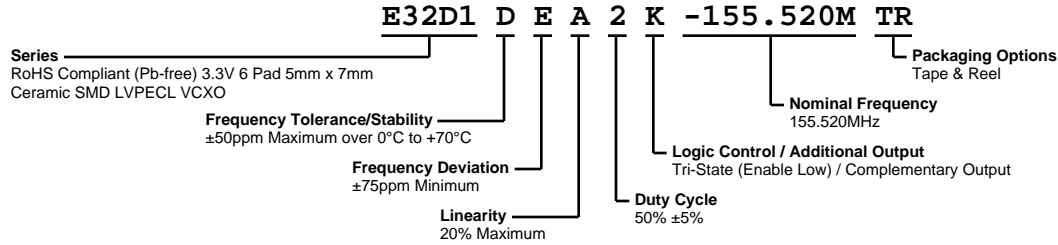


# E32D1DEA2K-155.520M TR



## ELECTRICAL SPECIFICATIONS

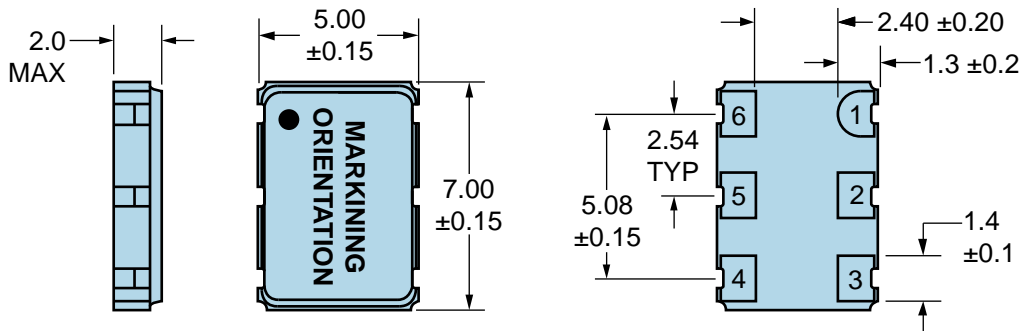
<b>Nominal Frequency</b>	155.520MHz
<b>Frequency Tolerance/Stability</b>	$\pm 50$ ppm Maximum over 0°C to +70°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration.)
<b>Supply Voltage</b>	3.3Vdc $\pm 5\%$
<b>Input Current</b>	100mA Maximum (with Load)
<b>Output Voltage Logic High (Voh)</b>	Vcc-1.025Vdc Minimum
<b>Output Voltage Logic Low (Vol)</b>	Vcc-1.620Vdc Maximum
<b>Rise/Fall Time</b>	1.5nSec Maximum (Measured over 20% to 80% of waveform)
<b>Duty Cycle</b>	50% $\pm 5\%$ (Measured at 50% of waveform)
<b>Load Drive Capability</b>	50 Ohms into Vcc-2.0Vdc
<b>Output Logic Type</b>	LVPECL
<b>Control Voltage</b>	1.65Vdc $\pm 1.65$ Vdc (Test Conditions for Frequency Deviation)
<b>Control Voltage Range</b>	0.0Vdc to Vcc +0.5Vdc
<b>Frequency Deviation</b>	$\pm 75$ ppm Minimum (Inclusive of Operating Temperature Range, Supply Voltage, and Load)
<b>Linearity</b>	20% Maximum
<b>Transfer Function</b>	Positive Transfer Characteristic
<b>Modulation Bandwidth</b>	10kHz Minimum (Measured at -3dB with a control voltage of +1.65Vdc)
<b>Input Impedance</b>	50kOhms Typical
<b>Phase Noise</b>	-55dBc/Hz at 10Hz offset, -90dBc/Hz at 100Hz offset, -120dBc/Hz at 1kHz offset, -140dBc/Hz at 10kHz offset, -145dBc/Hz at 100kHz offset, -148dBc/Hz at 1MHz (Typical Values, Fo=155.520MHz)
<b>Logic Control / Additional Output</b>	Tri-State (Enable Low) / Complementary Output
<b>Tri-State Input Voltage (Vih and Vil)</b>	Vih of 70% of Vcc Minimum to Disable Outputs (High Impedance), Vil of 30% of Vcc Maximum or No Connect to Enable Outputs
<b>RMS Phase Jitter</b>	0.4pSec Typical, 1pSec Maximum (Fj=12kHz to 20MHz)
<b>Accumulated Period Jitter (tacc)</b>	4pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution
<b>Period Jitter (trj)</b>	3pSec Typical, 5pSec Maximum Sigma of Random Jitter
<b>Period Jitter (trms)</b>	3pSec Typical, 5pSec Maximum Sigma of Total Jitter Distribution
<b>Period Jitter (tdj)</b>	4pSec Typical, 10pSec Maximum Deterministic Jitter
<b>Period Jitter (tp-p)</b>	27pSec Typical, 40pSec Maximum Peak to Peak of Jitter Distribution
<b>Start Up Time</b>	10mSec Maximum
<b>Storage Temperature Range</b>	-55°C to +125°C

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

<b>Fine Leak Test</b>	MIL-STD-883, Method 1014 Condition A
<b>Gross Leak Test</b>	MIL-STD-883, Method 1014 Condition C
<b>Mechanical Shock</b>	MIL-STD-202, Method 213 Condition C
<b>Resistance to Soldering Heat</b>	MIL-STD-202, Method 210
<b>Resistance to Solvents</b>	MIL-STD-202, Method 215
<b>Solderability</b>	MIL-STD-883, Method 2003
<b>Temperature Cycling</b>	MIL-STD-883, Method 1010
<b>Vibration</b>	MIL-STD-883, Method 2007 Condition A

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## MECHANICAL DIMENSIONS (all dimensions in millimeters)

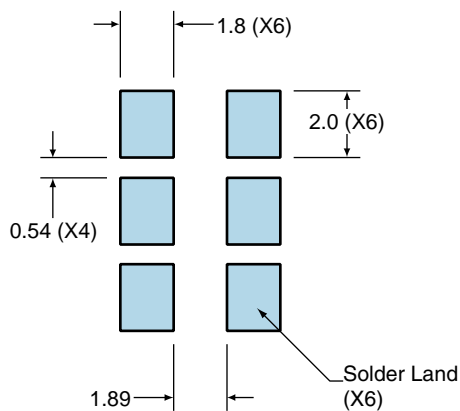


PIN	CONNECTION
1	Voltage Control
2	Tri-State
3	Case/Ground
4	Output
5	Complementary Output
6	Supply Voltage

LINE	MARKING
1	<b>ECLIPTEK</b>
2	<b>155.52M</b>
3	<b>XXYZZ</b> XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year

## Suggested Solder Pad Layout

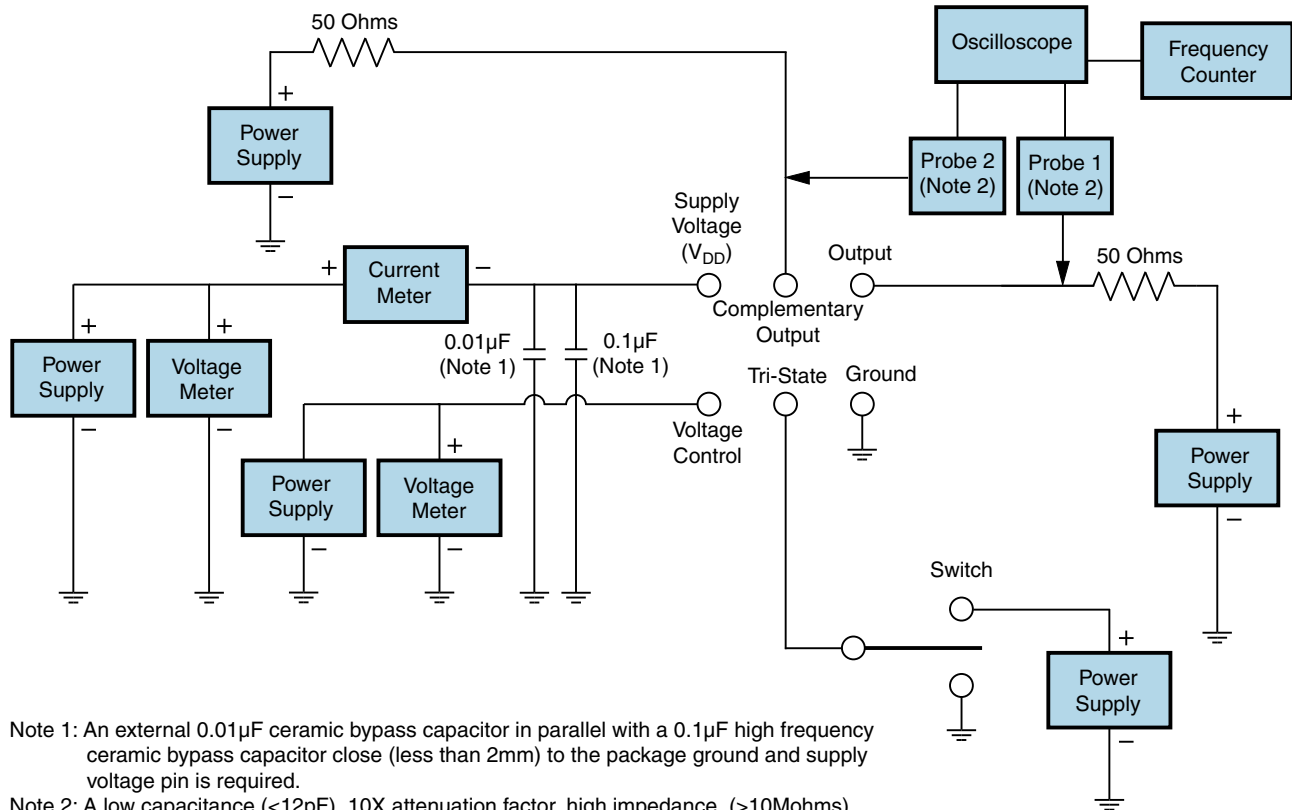
All Dimensions in Millimeters



All Tolerances are ±0.1

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## Test Circuit for Tri-State and Complementary Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

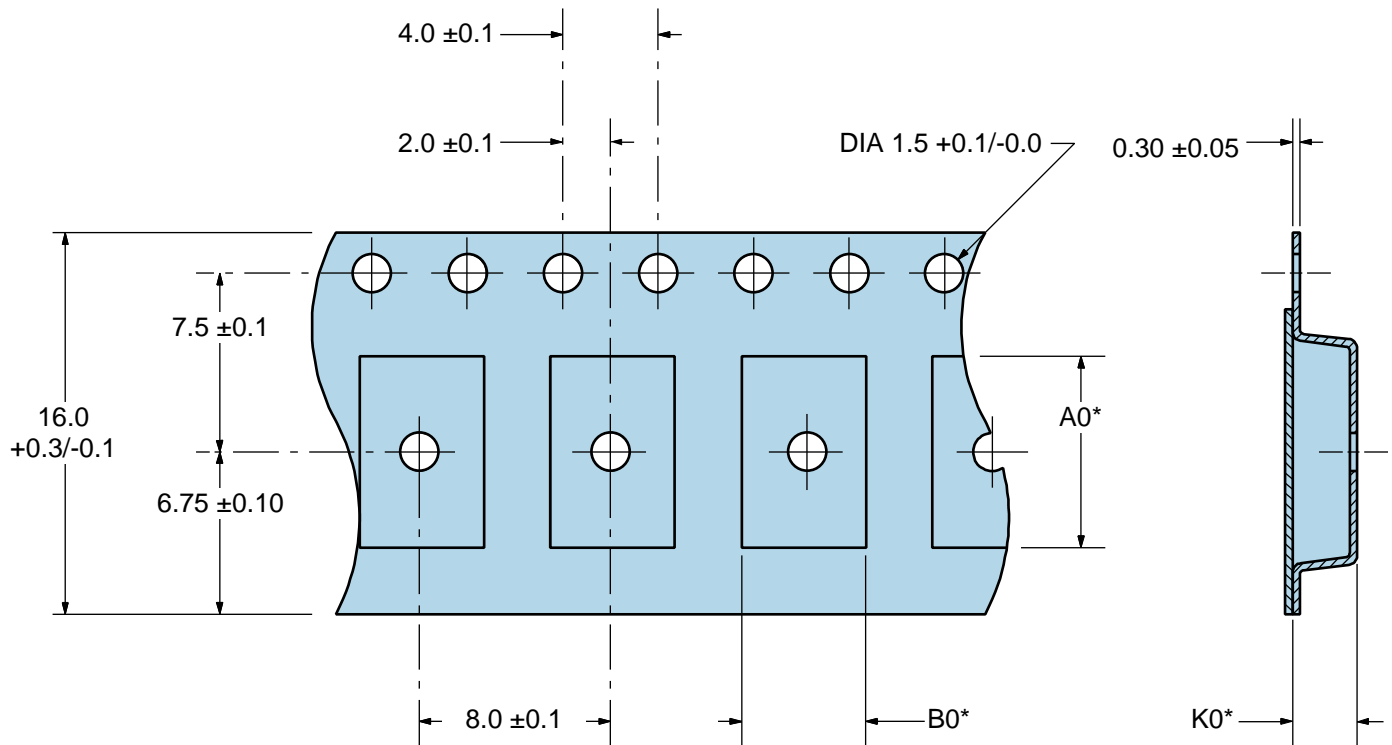
Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>500MHz) passive probe is recommended.

Note 3: Test circuit PCB traces need to be designed for a characteristic line impedance of 50 ohms.

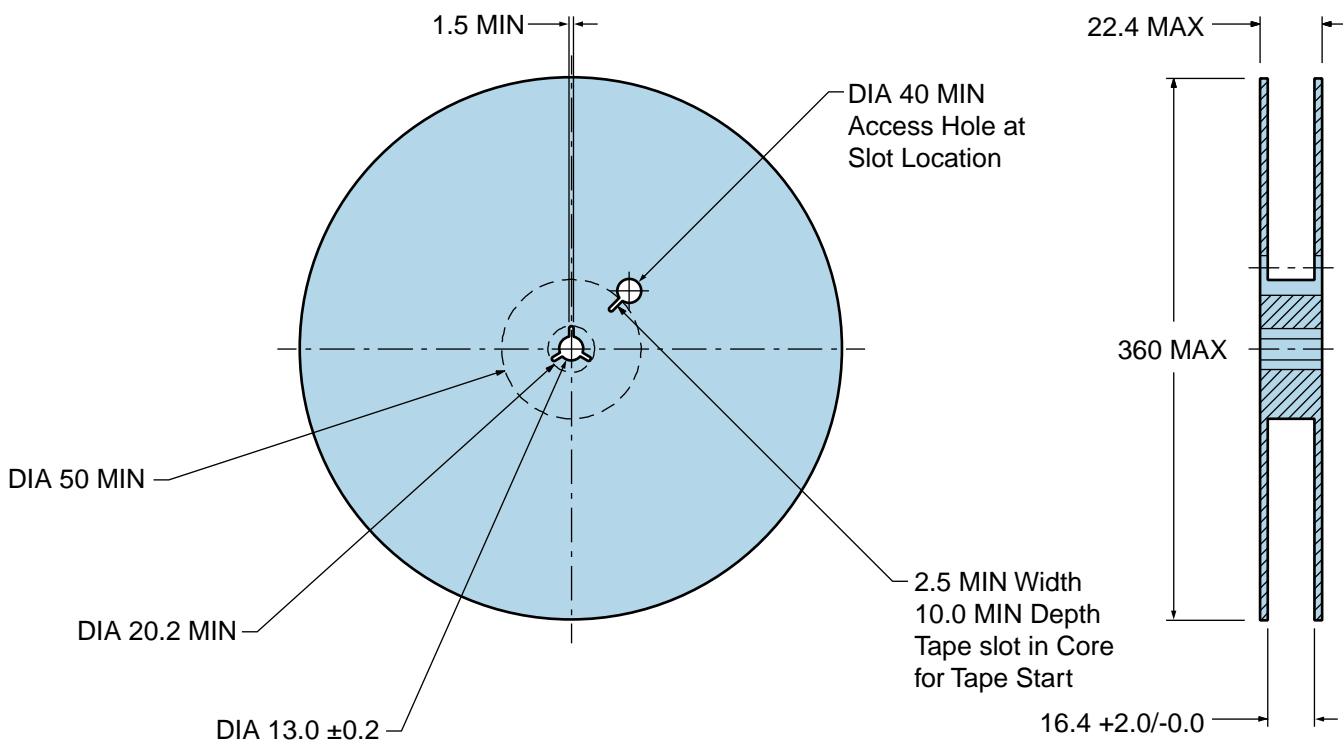
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## Tape & Reel Dimensions

Quantity Per Reel: 1,000 units



\*Compliant to EIA 481A



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## Recommended Solder Reflow Methods



### High Temperature Infrared/Convection

<b><math>T_s</math> MAX to <math>T_L</math> (Ramp-up Rate)</b>	3°C/second Maximum
<b>Preheat</b>	
- Temperature Minimum ( $T_s$ MIN)	150°C
- Temperature Typical ( $T_s$ TYP)	175°C
- Temperature Maximum ( $T_s$ MAX)	200°C
- Time ( $t_s$ MIN)	60 - 180 Seconds
<b>Ramp-up Rate (<math>T_L</math> to <math>T_p</math>)</b>	3°C/second Maximum
<b>Time Maintained Above:</b>	
- Temperature ( $T_L$ )	217°C
- Time ( $t_L$ )	60 - 150 Seconds
<b>Peak Temperature (<math>T_p</math>)</b>	260°C Maximum for 10 Seconds Maximum
<b>Target Peak Temperature (<math>T_p</math> Target)</b>	250°C +0/-5°C
<b>Time within 5°C of actual peak (<math>t_p</math>)</b>	20 - 40 seconds
<b>Ramp-down Rate</b>	6°C/second Maximum
<b>Time 25°C to Peak Temperature (t)</b>	8 minutes Maximum
<b>Moisture Sensitivity Level</b>	Level 1

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## Recommended Solder Reflow Methods



### Low Temperature Infrared/Convection 240°C

<b>T<sub>s</sub> MAX to T<sub>L</sub> (Ramp-up Rate)</b>	5°C/second Maximum
<b>Preheat</b>	
- Temperature Minimum (T <sub>s</sub> MIN)	N/A
- Temperature Typical (T <sub>s</sub> TYP)	150°C
- Temperature Maximum (T <sub>s</sub> MAX)	N/A
- Time (t <sub>s</sub> MIN)	60 - 120 Seconds
<b>Ramp-up Rate (T<sub>L</sub> to T<sub>P</sub>)</b>	5°C/second Maximum
<b>Time Maintained Above:</b>	
- Temperature (T <sub>L</sub> )	150°C
- Time (t <sub>L</sub> )	200 Seconds Maximum
<b>Peak Temperature (T<sub>P</sub>)</b>	240°C Maximum
<b>Target Peak Temperature (T<sub>P</sub> Target)</b>	240°C Maximum 1 Time / 230°C Maximum 2 Times
<b>Time within 5°C of actual peak (t<sub>p</sub>)</b>	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
<b>Ramp-down Rate</b>	5°C/second Maximum
<b>Time 25°C to Peak Temperature (t)</b>	N/A
<b>Moisture Sensitivity Level</b>	Level 1

### Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

### High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.