

AS5011

Data Sheet

Low Power Integrated Hall IC for Human Interface Applications

1 General Description

The AS5011 is a complete Hall Sensor IC for smart navigation key applications to meet the low power requirements and host SW integration challenges for products such as cell phones and smart handheld devices.

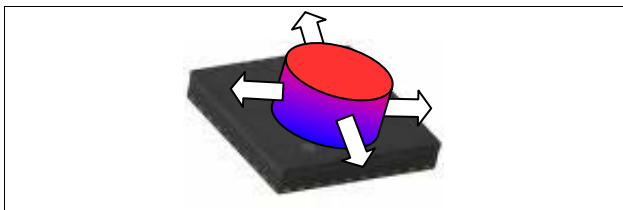
Due to the on chip processing engine, system designers are not tasked with integrating complex SW algorithms on their host processor thus leading to rapid development cycles.

The AS5011 single-chip IC includes 4 integrated Hall sensing elements for detecting up to $\pm 2\text{mm}$ lateral displacement, high resolution ADC, XY coordinate and motion detection engine combined with a smart power management controller.

The X and Y positions coordinates and magnetic field information for each Hall sensor element is transmitted over a 2-wire I²C compatible interface to the host processor.

The AS5011 is available in a small 16-pin 5x5x0.55mm QFN package and specified over an operating temperature of -20 to +80°C.

Figure 1 Typical Arrangement of AS5011 and Axial Magnet



2 Benefits

- Complete system-on-chip
- High reliability due to non-contact sensing
- Low power consumption

3 Key Features

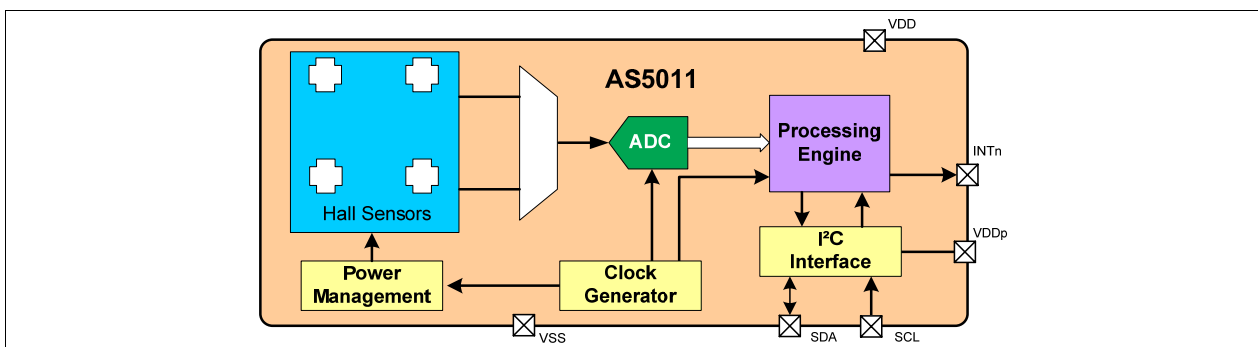
- 2.7 to 3.6V operating voltage
- Down to 1.8V peripheral supply voltage
- Less than 200µA current consumption in Low Power mode
- Less than 50µA current consumption in Shutdown mode
- Lateral magnet movement radius up to 2mm
- I²C interface up to 4MHz
- Configurable interrupt output for motion detection
- Three operating modes:
 - Shutdown mode
 - Low Power mode
 - Full Power mode

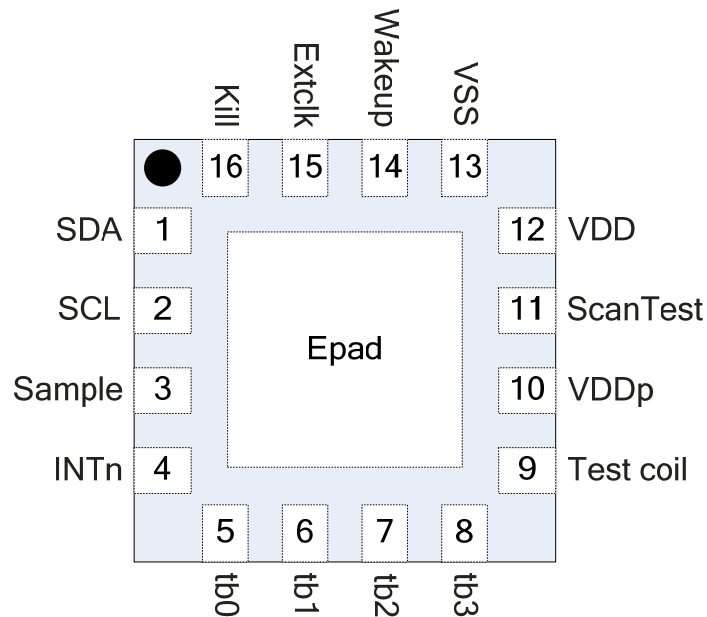
4 Applications

The AS5011 is ideal for small factor manual input devices in battery operated equipment, such as

- Mobile phones
- MP3 players
- PDA's
- GPS receivers
- Gaming consoles

Figure 2 AS5011 Block Diagram





Pin# QFN16	Symbol	Type	Description
1	SDA	DIO_OD	I ² C bus data
2	SCL	DI	I ² C bus clock
3	Sample	DI	Test pin. Connect to VSS
4	INTn	DO_OD	Interrupt output. Active LOW
5	tb0	AIO	Test pin. Leave unconnected
6	tb1	AIO	Test pin. Leave unconnected
7	tb2	AIO	Test pin. Leave unconnected
8	tb3	AIO	Test pin. Leave unconnected
9	Test coil	-	Test pin. Connect to VSS
10	VDDp	S	Peripheral power supply, 1.8 ~ 3.6V
11	ScanTest	DI	Test pin. Connect to VSS
12	VDD	S	Core power supply, 2.7 ~ 3.6V
13	VSS	S	Supply ground
14	Wakeup	DIO	Test pin. Leave unconnected
15	Extclk	DIO	Test pin. Leave unconnected
16	Kill	DIO	Test pin. Leave unconnected
Epad	-	-	Center pad not connected

PIN Types:	S	...	supply pad	AIO	...	analog I/O
	DI	...	digital input	DIO_OD	...	digital input / output open drain
	DO_OD	...	digital output open drain	DIO	...	digital input / output

6 Operating the AS5011

6.1 Typical application

The AS5011 requires only a few external components in order to operate immediately when connected to the host microcontroller.

Only 4 wires are needed for a simple application using a single power supply: two wires for power and two wires for the I²C communication. A fifth connection can be added in order to send an interrupt to the host CPU when the magnet is moving away from the center and to inform that a new valid coordinate can be read.

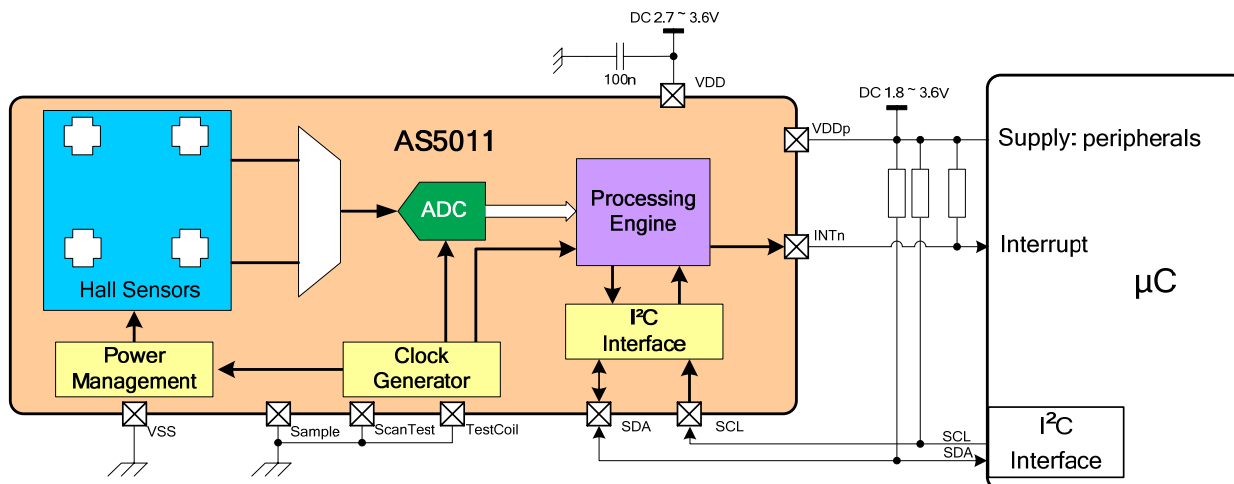
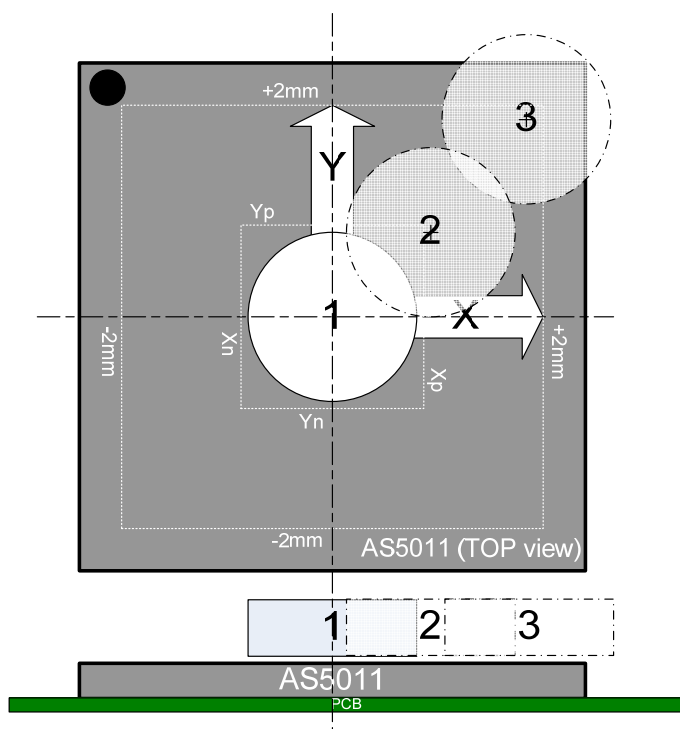


Figure 4: Electrical connection of AS5011 with microcontroller

6.2 XY coordinates interpretation

On Figure 5 the top view of the AS5011 is represented, with a round magnet (scaled) gliding over its surface. The magnet can be placed under the sensor too, with the PCB between them.



- Magnet on position 1:

The magnet is in its initial position, centered on the sensor. The AS5011 is in Shutdown mode. X and Y register values are (0,0)

- Magnet on position 2:

The center of the magnet has been moved upon the horizontal wakeup threshold Xp. An interrupt is sent to the host microcontroller which sets the AS5011 to Low Power mode. Wakeup thresholds are programmable independently for the four directions.

- Magnet on position 3:

The magnet is at the X and Y limit over the sensor surface (2mm, 2mm) but still in range.

Figure 5: Position range of the magnet

6.3 Magnet-chip surface airgap range

The relation between the magnet physical position and the resulting XY registers depends on the magnet type/size/shape, and the airgap between the magnet and the top (or bottom) surface of the AS5011.

The measurements on Figure 6, Figure 6 Figure 8 have been processed with the AS5000-MA2H-1 d2x0.8mm cylinder magnet, available on austriamicrosystems website. For those magnets, used in EasyPoint modules EP40 and EP50, the airgap range is typically 0~3mm.

The following diagrams show the relation between the X register value and the physical X coordinate ($\pm 2\text{mm}$ horizontal displacement, 0mm is the center of the chip package) of the magnet at different airgaps. The resulting X value range decreases when the airgap increases

The Y axis measurements are the same as the X axis ones.

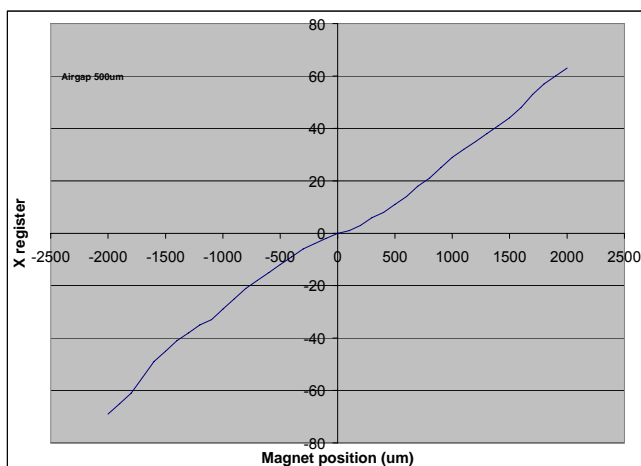


Figure 6: X register / X displacement (500um airgap)

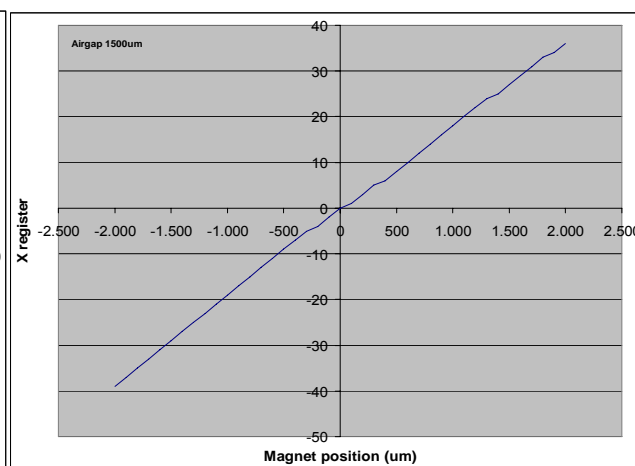


Figure 7: X register / X displacement (1500um airgap)

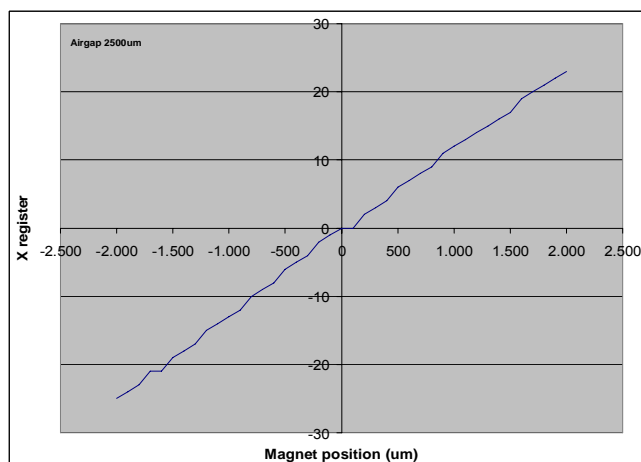


Figure 8: X register / X displacement (2500um airgap)

6.4 Power modes

The AS5011 can operate in three different power modes, depending on the power consumption requirements of the whole system.

Power Mode	[0x76] Register	Description
Sleep phase		Power state between wakeups in Shutdown and Low Power modes RC clock and analog part OFF Digital part in static mode
Shutdown mode	1001_x00x LP_Pulsed = 1 LP_Active = 0 LP_Continue = 0 INT_wup_en = 1	Default mode after power on <50µA current consumption Wake up every 80ms from Sleep phase Hall elements in reduced power during wake up RC clock ON Interrupt LOW on INTn if the magnet is away from the center above the Xp Xn Yp Yn threshold values (1)
Low Power mode	110x_100x LP_Pulsed = 1 LP_Active = 1 LP_Continue = 0 INT_act_en = 1	<200µA current consumption Wake up every 20ms from Sleep phase Hall elements in high power during wake up for better accuracy RC clock ON Interrupt LOW on INTn when XY coordinates are ready to be read (1)
Full Power mode	010x_y00x LP_Pulsed = 0 LP_Active = 1 LP_Continue = 0 INT_act_en = y	<8mA current consumption Continuous read Hall elements in high power permanently RC clock ON Interrupt LOW on INTn when XY coordinates are ready to be read (1) If <i>INT_act_en</i> = 1, after reading the XY coordinate, the next sample is stored and won't be updated until the next read of XY with interrupt release. If <i>INT_act_int_en</i> = 0, the last converted XY coordinate is read in real time.

(1) The interrupt will be released to HIGH by reading the X_res_int or Y_res_int registers, or by switching the device into a different power mode.

Table 2: Overview of typical power modes

6.4.1 Shutdown mode

$LP_Pulsed = 1, LP_Active = 0, LP_Continue = 0, INT_wup_en = 1 \rightarrow [0x76] = 1001_x00x$

This is the default operating mode when powering up the device, giving the lowest power consumption when the whole system is in idle mode.

The analog part of the AS5011 is powered off (sleep mode). It is waked up every 80ms by an internal low power logic, the hall sensors are read and the XY coordinate of the magnet is computed.

If the magnet position is above the threshold limits X_p, X_n, Y_p, Y_n , an interrupt will be generated on the INTn pin and the device returns to sleep mode waiting for the next wake up after 80ms. As the host microcontroller receives the interrupt, it can read the X and Y positions or configure the AS5011 to Low Power mode (see 6.4.2 below) in order to track the magnet position until it returns to its initial position on the center.

INT_n remains LOW until X_int/Y_int have been read, or after a power mode change. The typical coordinates read application after an interrupt is to read X first then Y_int.

6.4.2 Low Power mode

$LP_Pulsed = 1, LP_Active = 1, LP_Continue = 0, INT_act_en = 1 \rightarrow [0x76] = 110x_100x$

The Low Power mode is used to track the magnet coordinates when it has been moved from its initial center position.

The AS5011 is in sleep mode and is waked up every 20ms. As soon as the XY position of the magnet is computed, an interrupt is sent on the INTn pin to the microcontroller indicating that a valid coordinate is available, then the sensor returns to sleep mode waiting for the next wake up after 20ms. INT_n remains LOW until X_int/Y_int have been read, or after a power mode change. The typical coordinates read application after an interrupt is to read X first then Y_int.

This mode generates a higher power consumption than the Shutdown mode because of the faster sampling rate and the higher hall sensor current to provide an optimal accuracy of the coordinates.

When the microcontroller detects that the magnet has returned to the initial center position, it has to configure the AS5011 back to Shutdown mode (see 6.4.1).

6.4.3 Full Power mode

$LP_Pulsed = 0, LP_Active = 1, LP_Continue = 0 \rightarrow [0x76] = 010x_y00x$

This mode allows the fastest coordinates reading. The sensor stays at its full capability, and never enters in sleep mode.

The interrupt output goes LOW each time a new X and Y result has been computed and the valid data are ready to be read by the host microcontroller. INT_n remains LOW until X_int/Y_int have been read, or after a power mode change. The typical coordinates read application after an interrupt is to read X first then Y_int.

The INT_act_en bit (y):

- If $INT_act_en = 1$, after reading the X_int or Y_int register, the next sampled XY coordinate is stored and won't be updated until the next read of X_int or Y_int.
- If $INT_act_en = 0$, the last converted XY coordinate is read in real time.

6.4.4 Switching the power modes

The following sequence example would be used for a typical mobile application (mobile phone, PDA, MP3 player):

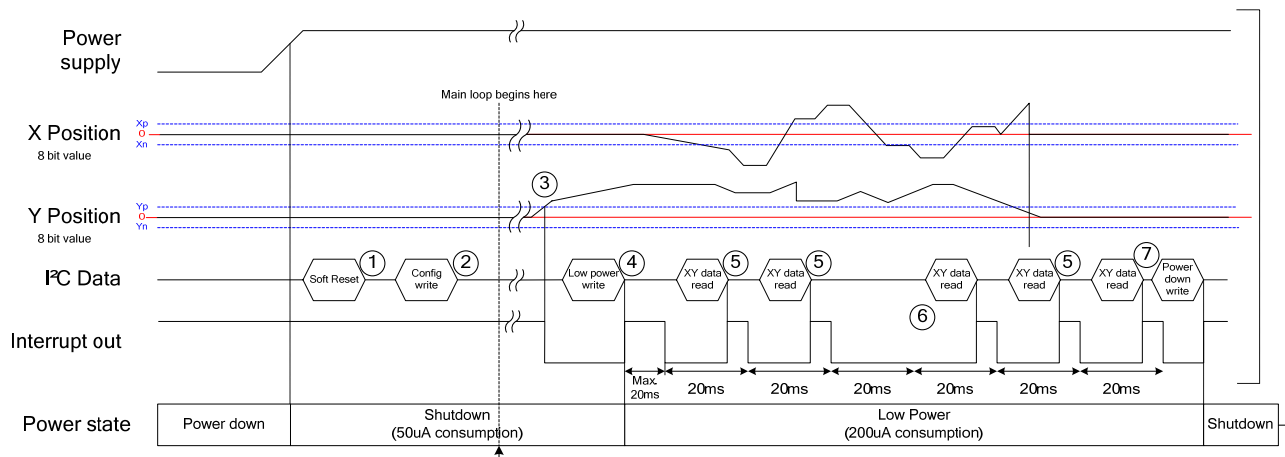


Figure 9: Typical application sequence for mobile device

- ① After a complete system power up, a soft reset should be applied by sending the I²C commands $[0x76] = 0x9A$ then $[0x76] = 0x98$.
- ② If needed the host microcontroller writes the configuration once to the AS5011, for example the *inv_spinning* register if the magnet is inverted (see 7.2) or the *Xp Xn Yp Yn* wakeup threshold values. The cursor is normally centered $X,Y = (0,0)$ as the magnet position 1 on Figure 5. The AS5011 is in *Shutdown mode* by default.
- ③ The cursor is moved by the user above the Y_p threshold. An interrupt is generated and remains LOW until an X_int/Y_int read or a power mode changing.
- ④ The microcontroller configures the AS5011 in *Low Power mode* ($[0x76] = 110x_100x$) for faster reading. The interrupt is released to HIGH automatically by the power mode change.
- ⑤ Interrupts are generated automatically every 20ms when the XY coordinates are ready for reading. The microcontroller reads the X register $[0x41]$ then Y_int register $[0x52]$ which releases $INTn$ to HIGH. During this phase, the cursor is still moving and stays out of the wakeup thresholds range.
- ⑥ If the microcontroller doesn't read X_int or Y_int immediately after an interrupt, the $INTn$ pin remains LOW until the next read of X_int or Y_int . The last new converted (a new sample every 20ms) coordinate will be transferred.
- ⑦ The cursor has been released by the user, and returns to the center of the AS5011 (magnet position 1 on Figure 5). The microcontroller will read $X,Y = (0,0)$, and will configure the sensor to *Shutdown mode* ($[0x76] = 1001_x00x$).

Note:

Firmware application notes with source code example for AS5011 and EasyPoint modules are available on www.austriamicrosystems.com website.

7 I²C interface

The AS5011 supports the 2-wire I²C protocol without “repeat start” as a slave device, the host CPU (master) has to initiate the data transfers. The 7-bit device address of the AS5011 is ‘1000 000’.

The SDA signal is bidirectional and is used to read and write the serial data. The SCL signal is the clock generated by the host CPU, to synchronize the SDA data in read and write mode. The maximum I²C clock frequency is 4MHz, data are triggered on the rising edge of SCL.

7.1 Interface operation

For both read and write data transfers consist of three phases:

1. The master sends a START command by pulling down SDA while SCL remains high. Then the 7-bit device address is sent followed by a read/write bit indicator. In READ mode (r/w = ‘1’), the slave has to send the data from its selected register. In WRITE mode (r/w = ‘0’), the master writes the data in the selected register. The slave has to acknowledge by sending ‘0’ after the r/w bit from the master.
2. The slave register is selected by the second data sent by the master. The address has an 8-bit format. The slave has to acknowledge by sending ‘0’ after the bit R0.
3. The 8-bit data is transferred from/to the slave selected register, depending on the r/w bit. At the end of the 8-bit data transfer, the master (read mode) or the slave (write mode) acknowledges by sending ‘1’. The transfer ends when the master sends a STOP command by sending a low to high transition while SCL remains high.

The AS5011 does not send any acknowledge after the device address or register address (ACK remains High) in the following cases:

- Wrong address
- Write access to a read-only register

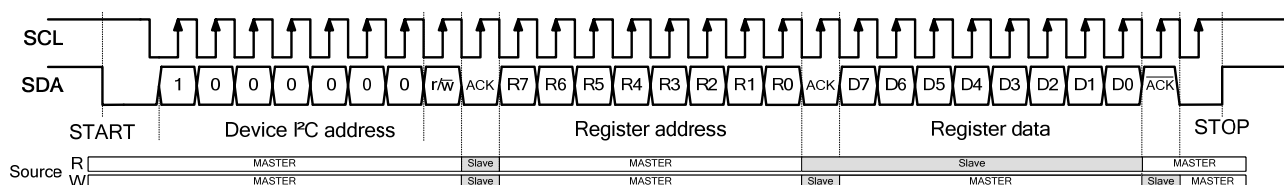


Figure 10: I²C bus Read and Write operation

7.2 I²C Registers

The following registers / functions are accessible over the serial I²C interface.

Register	size	Access	Address	Format	Reset Value	Bit	Description
Control Register 1							
LP_pulsed	1	R/W	0x76		1	<7>	Low Power control register. See Table 2.
LP_active	1	R/W	0x76		0	<6>	Low Power control register. See Table 2.
LP_continue	1	R/W	0x76		0	<5>	For test only. Must be 0.
INT_wup_en	1	R/W	0x76		1	<4>	Interrupt control register. If set, the interrupt pin goes low in Shutdown mode when the magnet has moved away from the center, above the xp, xn, yp yn threshold values.
INT_act_en	1	R/W	0x76		1	<3>	Interrupt control register. If set, the interrupt pin goes LOW in Low Power mode when a new XY value is ready for reading. Stores coordinate until next read in full power mode,
ext_clk_en	1	R/W	0x76		0	<2>	For test only. Must be 0.
soft_rst	1	R/W	0x76		0	<1>	Soft Reset. soft_rst = 0: normal mode soft_rst = 1: all registers return to their respective reset value
data_valid	1	R	0x76		0	<0>	Data valid. data_valid = 0: no valid XY coordinates data_valid = 1: valid data are ready to be read
Control Register 2							
Test 7	1	R/W	0x75		0	<7>	For test only. Must be 0.
Test 6	1	R/W	0x75		1	<6>	For test only. Must be 1.
Test 5	1	R/W	0x75		0	<5>	For test only. Must be 0.
Test 4	1	R/W	0x75		0	<4>	For test only. Must be 0.
ext_sample_en	1	R/W	0x75		0	<3>	For test only. Must be 0.
rc_bias_on	1	R/W	0x75		0	<2>	For test only. Must be 0.
inv_spinning	1	R/W	0x75		0	<1>	Invert the channel voltage. Set if the magnet polarity is reversed.
pptrim_en	1	R/W	0x75		0	<0>	For test only. Must be 0.
Range and position values							
Xp	8	R/W	0x43	2' comp	0x28 (40d)		Wakeup threshold on the positive X direction.
Xn	8	R/W	0x44	2' comp	0xD8 (-40d)		Wakeup threshold on the negative X direction.
Yp	8	R/W	0x53	2' comp	0x28 (40d)		Wakeup threshold on the positive Y direction.
Yn	8	R/W	0x54	2' comp	0xD8 (-40d)		Wakeup threshold on the negative Y direction.
X	8	R	0x41	2' comp	0x00		X position. The zero value means the horizontal center position on the AS5011.
Y	8	R	0x42	2' comp	0x00		Y position. The zero value means the vertical center position on the AS5011.
X_res_int	8	R	0x51	2' comp	0x00		X position. Releases INT_n to '1'
Y_res_int	8	R	0x52	2' comp	0x00		Y position. Releases INT_n to '1'

Table 3: I²C Registers

8 Device specifications

8.1 Absolute maximum ratings (non operating)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage	VDD	-0.3	5	V	
Peripheral supply voltage	VDDp	-0.3	5 VDD +0.3	V	
Input pin voltage	V _{in}	-0.3	VDDp +0.3	V	
Input pin voltage	V _{in}	-	3.6	V	
Input current (latchup immunity)	I _{scr}	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge	ESD	-	±1	kV	Norm: MIL 883 E method 3015
Package Thermal Resistance	Θ _{JA}	-	30	°C/W	Velocity=0, Multi Layer PCB; JEDEC Standard Testboard
Total power dissipation	P _t		36	mW	
Storage temperature	T _{strg}	-55	125	°C	
Package body temperature	T _{body}		260	°C	Norm: IPC/JEDEC J-STD-020C
Humidity non-condensing		5	85	%	

8.2 Operating conditions

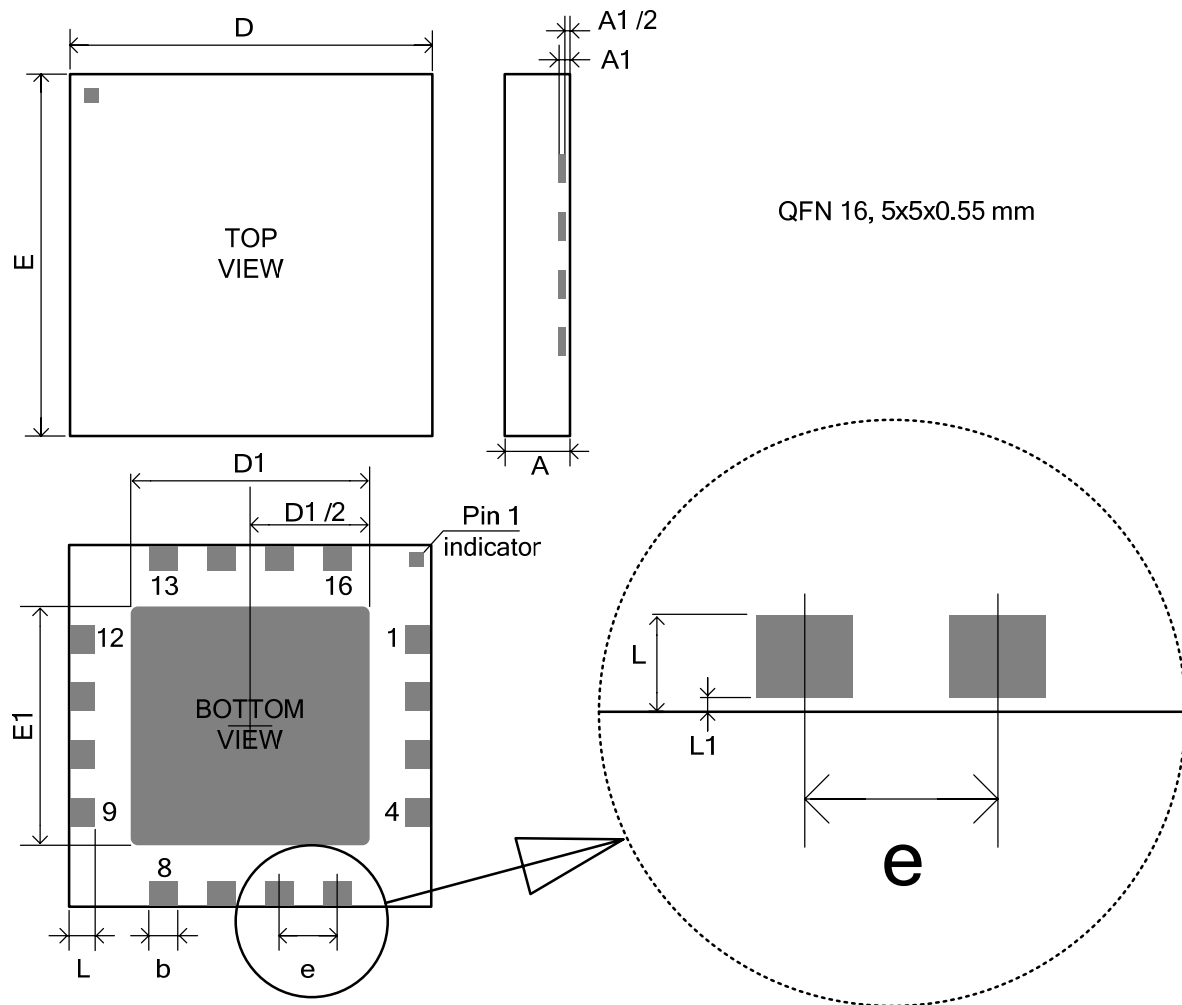
(operating conditions: $T_{amb} = -20$ to $+80^{\circ}\text{C}$, $VDD = 3.3\text{V}$)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Supply voltage	VDD	2.7		3.6	V	
Peripheral Supply voltage	VDDp	1.8		VDD +0.3	V	open drain outputs : SCL, SDA, INT/
Current consumption on core supply, Shutdown mode	IDD _s			50	μA	average current pin VDD pulsed current IDD _f during t_{conv} with period $t_{p,W}$
Current consumption on core supply, Low Power mode	IDD _l			200	μA	average current pin VDD pulsed current IDD _f during t_{conv} with period $t_{p,A}$
Current consumption on core supply, Full Power mode	IDD _f			8	mA	continuous current pin VDD
Current consumption on IO supply	IDDp		1		μA	average current pin VDDp, 20ms i ² C polling, 47k pullup resistor on SDA
Polling clock rate, Shutdown mode	$t_{p,W}$	65.6	80	94.4	ms	internal
Polling clock rate, Low Power mode	$t_{p,A}$	16.4	20	23.6	ms	internal
Coordinate conversion time	t_{conv}	330	380	455	μs	Full Power mode
lateral movement radius	$\begin{matrix} dx \\ dy \end{matrix}$	± 1.8	2	± 2.3	mm	vertical magnetic field at magnet centre, measured at the chip surface
type of magnet	d	2		3	mm	cylindrical; axial magnetized
Hall array diameter	RH		2.2		mm	
magnetic field strength	B _z	30		120	mT	vertical magnetic field at magnet center; measured at chip surface
Ambient temperature range	T _{amb}	-20		+80	$^{\circ}\text{C}$	
Magnetic field measurement resolution			11		bit	Internal
Resolution of XY displacement			8		bit	over 2*dx and 2*dy axis
IC package		QFN16 5x5x0.55mm				
Power supply filtering capacitors		100			nF	Ceramic capacitor VDD - VSS
		100			nF	Ceramic capacitor VDDp - VSS

8.3 Digital IO pads DC/AC characteristics

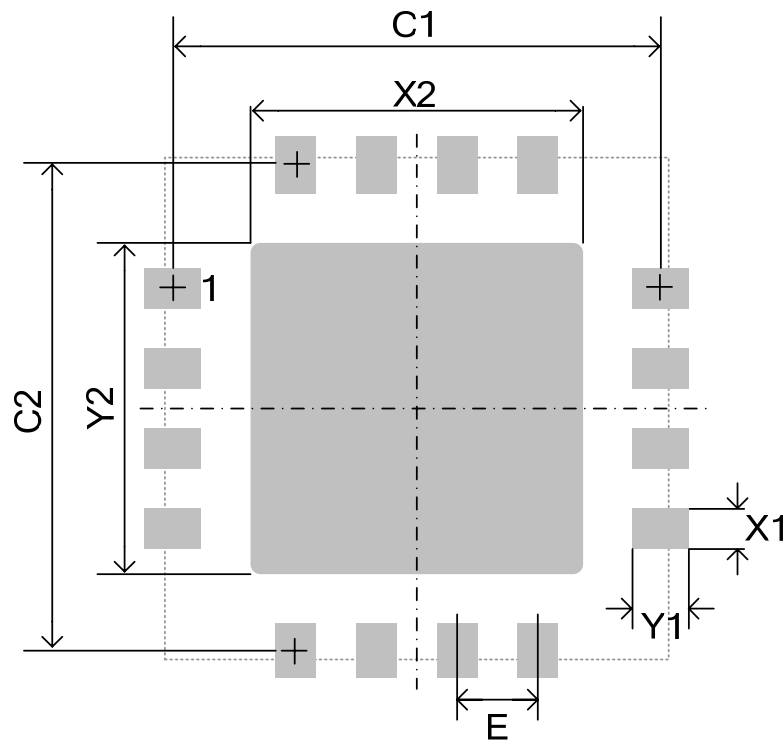
Parameter	Symbol	Min	Max	Unit	Note
Inputs: SCL, SDA (receiver)					
High level input voltage	V_{IH}	$0.7 \cdot V_{DDp}$		V	
Low level input voltage	V_{IL}		$0.3 \cdot V_{DDp}$	V	$V_{DDp} \geq 2.7V$
			$0.25 \cdot V_{DDp}$		$V_{DDp} < 2.7V$
Input leakage current	I_{LEAK}		1	μA	$V_{DDp} = 3.6V$
Capacitive load	C_L		35	pF	
Outputs: INTn, SDA (transmitter)					
High level output voltage	V_{OH}	Open drain			Leakage current 1 μA
Low level output voltage	V_{OL}		$V_{SS} + 0.4$	V	-2mA

9 Package Drawings



DIM (mm)	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.152 REF		
b	0.35	0.40	0.45
D	5.00 BSC		
E	5.00 BSC		
D1	3.5	3.6	3.7
E1	3.15	3.25	3.35
e	0.80 BSC		
L	0.35	0.40	0.45
L1	0.00		0.10

10 Recommended footprint



DIM (mm)	Typ
C1	4.8
C2	4.8
E	0.8
X1	0.45
X2	3.7
Y1	0.9
Y2	3.7

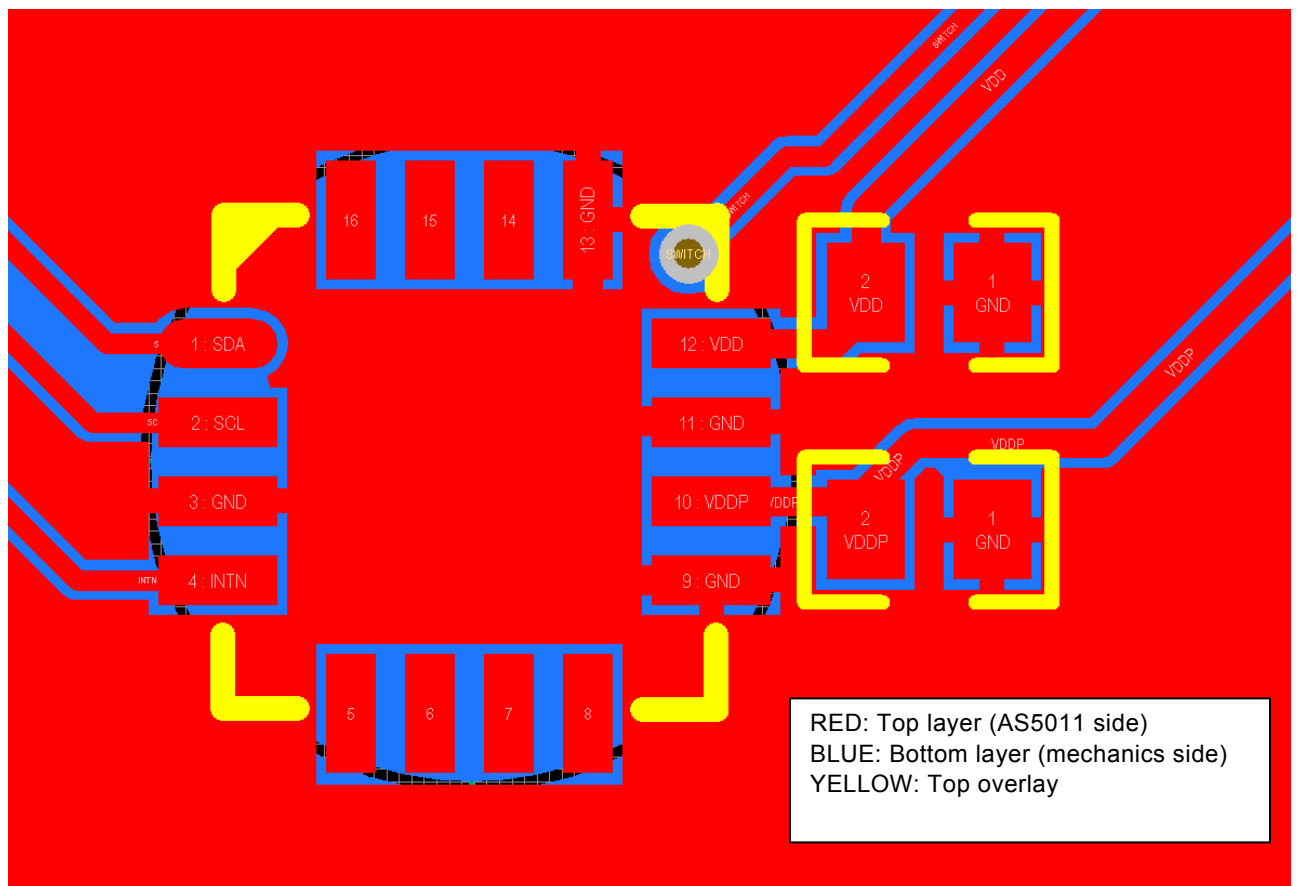


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Revision History

Revision	Date	Description
3.10	November.3.2009	<ul style="list-style-type: none"> Added recommended footprint Added 0x75 register description
3.6	July. 3. 2009	<ul style="list-style-type: none"> Added AS5000-MA2H-1 Magnet reference
3.5	June. 8.2009	<ul style="list-style-type: none"> QFN 5x5x0.55mm package I²C @ 4MHz max.

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